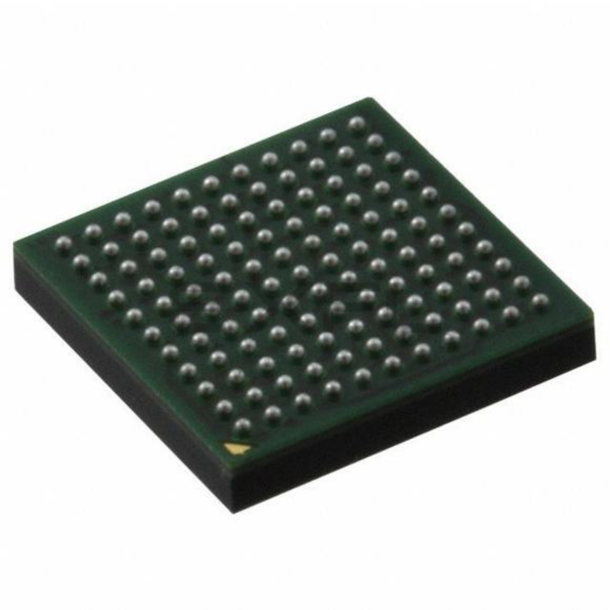

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LCD, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 37x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-LFBGA
Supplier Device Package	121-MAPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk51dn512cmc10

Table of Contents

Field	Description	Values
FFF	Program flash memory size	• 32 = 32 KB • 64 = 64 KB • 128 = 128 KB • 256 = 256 KB • 512 = 512 KB • 1M0 = 1 MB • 2M0 = 2 MB
R	Silicon revision	• Z = Initial • (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105 • C = –40 to 85
PP	Package identifier	• FM = 32 QFN (5 mm x 5 mm) • FT = 48 QFN (7 mm x 7 mm) • LF = 48 LQFP (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm) • MP = 64 MAPBGA (5 mm x 5 mm) • LK = 80 LQFP (12 mm x 12 mm) • LL = 100 LQFP (14 mm x 14 mm) • MC = 121 MAPBGA (8 mm x 8 mm) • LQ = 144 LQFP (20 mm x 20 mm) • MD = 144 MAPBGA (13 mm x 13 mm) • MJ = 256 MAPBGA (17 mm x 17 mm)
CC	Maximum CPU frequency (MHz)	• 5 = 50 MHz • 7 = 72 MHz • 10 = 100 MHz • 12 = 120 MHz • 15 = 150 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

MK51DN512ZVMD10

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

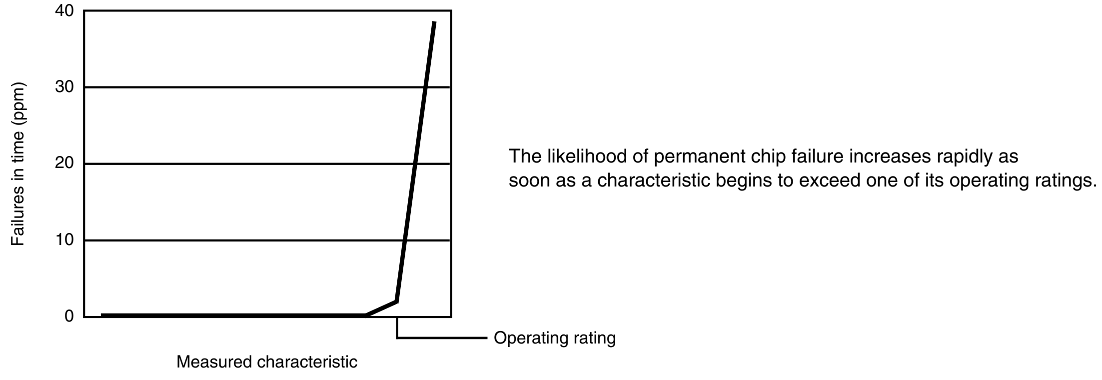
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

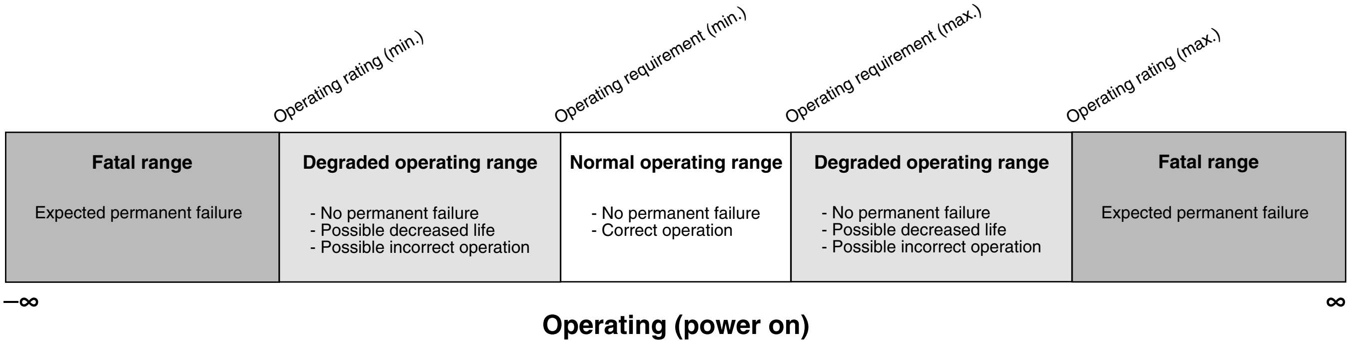
This is an example of an operating rating:

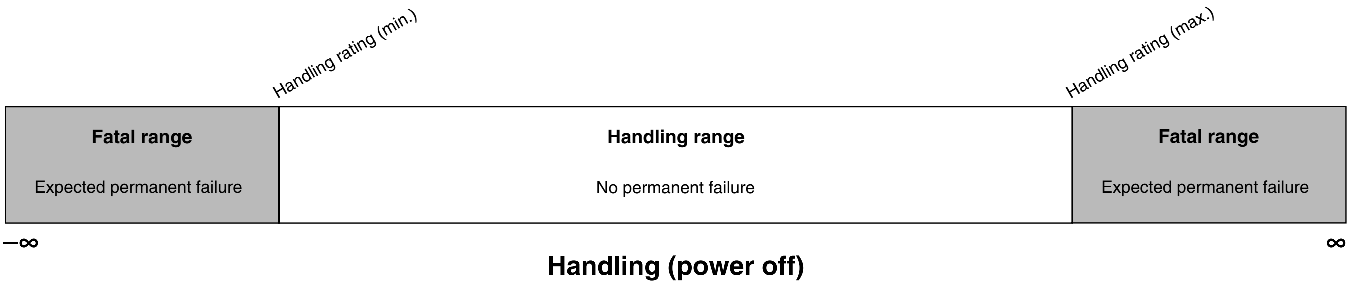
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

3.5 Result of exceeding a rating



3.6 Relationship between ratings and operating requirements





3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

4.4 Voltage and current operating ratings

5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength					
	• $2.7\ V \le V_{DD} \le 3.6\ V$, $I_{OH} = -9mA$	$V_{DD} – 0.5$	—	—	V	
	• $1.71\ V \le V_{DD} \le 2.7\ V$, $I_{OH} = -3mA$	$V_{DD} – 0.5$	—	—	V	
	Output high voltage — low drive strength					
	• $2.7\ V \le V_{DD} \le 3.6\ V$, $I_{OH} = -2mA$	$V_{DD} – 0.5$	—	—	V	
	• $1.71\ V \le V_{DD} \le 2.7\ V$, $I_{OH} = -0.6mA$	$V_{DD} – 0.5$	—	—	V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	
V_{OL}	Output low voltage — high drive strength					2
	• $2.7\ V \le V_{DD} \le 3.6\ V$, $I_{OL} = 10mA$	—	—	0.5	V	
	• $1.71\ V \le V_{DD} \le 2.7\ V$, $I_{OL} = 5mA$	—	—	0.5	V	
	Output low voltage — low drive strength					
	• $2.7\ V \le V_{DD} \le 3.6\ V$, $I_{OL} = 2mA$	—	—	0.5	V	
	• $1.71\ V \le V_{DD} \le 2.7\ V$, $I_{OL} = 1mA$	—	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{INA}	Input leakage current, analog pins and digital pins configured as analog inputs					3, 4
	• $V_{SS} \le V_{IN} \le V_{DD}$					
	• All pins except EXTAL32, XTAL32, EXTAL, XTAL	—	0.002	0.5	μA	
	• EXTAL (PTA18) and XTAL (PTA19)	—	0.004	1.5	μA	
	• EXTAL32, XTAL32	—	0.075	10	μA	
I_{IND}	Input leakage current, digital pins					4, 5
	• $V_{SS} \le V_{IN} \le V_{IL}$					
	• All digital pins	—	0.002	0.5	μA	
	• $V_{IN} = V_{DD}$					
	• All digital pins except PTD7	—	0.002	0.5	μA	
	• PTD7	—	0.004	1	μA	
I_{IND}	Input leakage current, digital pins					4, 5, 6
	• $V_{IL} < V_{IN} < V_{DD}$					
	• $V_{DD} = 3.6\ V$	—	18	26	μA	
	• $V_{DD} = 3.0\ V$	—	12	49	μA	
	• $V_{DD} = 2.5\ V$	—	8	13	μA	
	• $V_{DD} = 1.7\ V$	—	3	6	μA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.71	—	mA	7
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.77	—	mA	8
I_{DD_STOP}	Stop mode current at 3.0 V					
	• @ –40 to 25°C	—	0.74	1.41	mA	
	• @ 70°C	—	2.45	11.5	mA	
	• @ 105°C	—	6.61	30	mA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• @ –40 to 25°C	—	83	435	μA	
	• @ 70°C	—	425	2000	μA	
	• @ 105°C	—	1280	4000	μA	
I_{DD_LLS}	Low leakage stop mode current at 3.0 V					9
	• @ –40 to 25°C	—	4.58	19.9	μA	
	• @ 70°C	—	30.6	105	μA	
	• @ 105°C	—	137	500	μA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					9
	• @ –40 to 25°C	—	3.0	23	μA	
	• @ 70°C	—	18.6	43	μA	
	• @ 105°C	—	84.9	230	μA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	• @ –40 to 25°C	—	2.2	5.4	μA	
	• @ 70°C	—	9.3	35	μA	
	• @ 105°C	—	41.4	128	μA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• @ –40 to 25°C	—	2.1	9	μA	
	• @ 70°C	—	7.6	28	μA	
	• @ 105°C	—	33.5	95.5	μA	
I_{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V					
	• @ –40 to 25°C	—	0.19	0.22	μA	
	• @ 70°C	—	0.49	0.64	μA	
	• @ 105°C	—	2.2	3.2	μA	

Table continues on the next page...

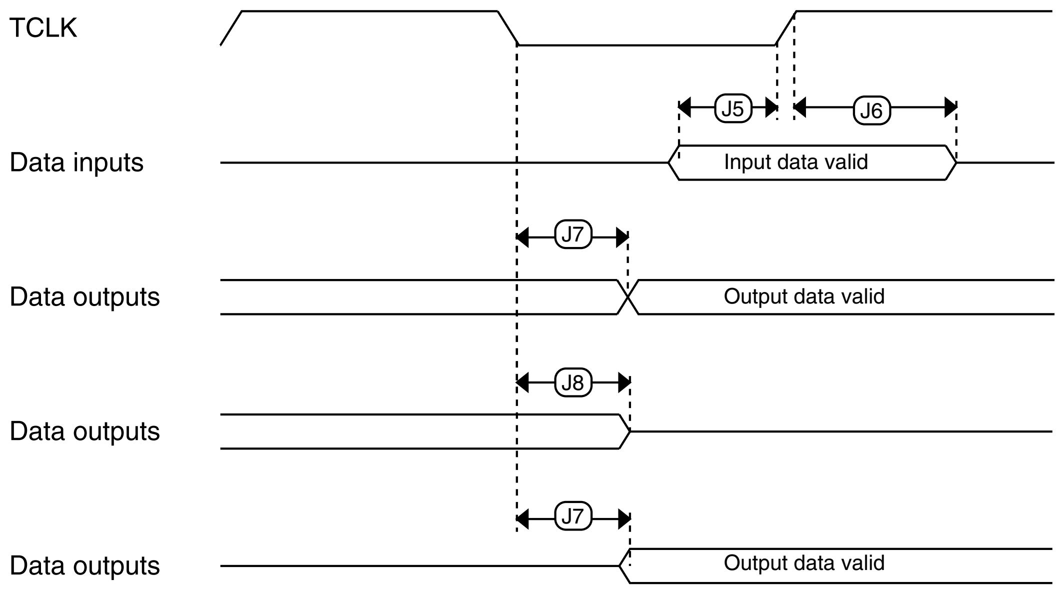


Figure 6. Boundary scan (JTAG) timing

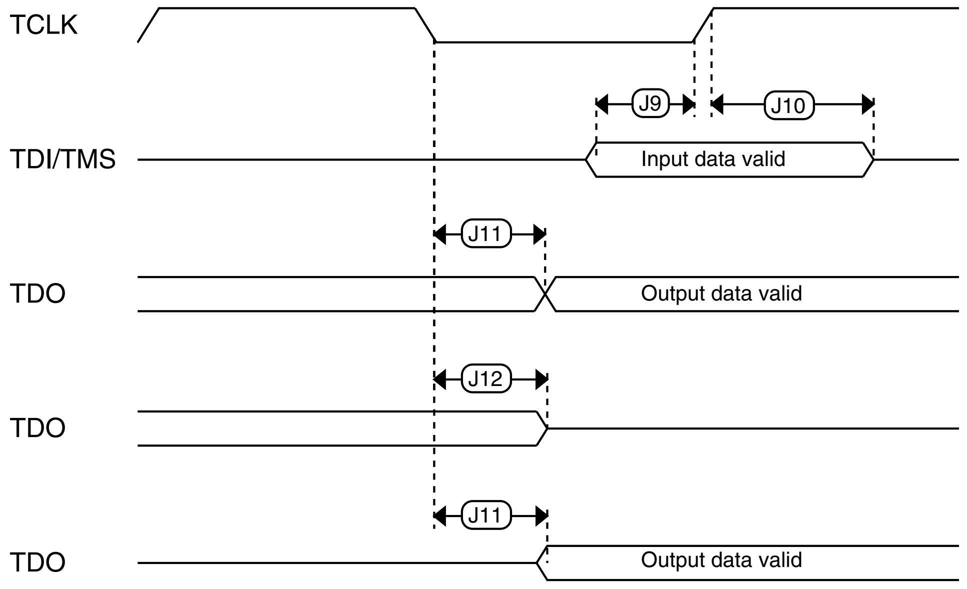


Figure 7. Test Access Port timing

Table 15. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS=00) $640 \times f_{fll\_ref}$	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) $1280 \times f_{fll\_ref}$	40	41.94	50	MHz	
		Mid-high range (DRS=10) $1920 \times f_{fll\_ref}$	60	62.91	75	MHz	
		High range (DRS=11) $2560 \times f_{fll\_ref}$	80	83.89	100	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) $732 \times f_{fll\_ref}$	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) $1464 \times f_{fll\_ref}$	—	47.97	—	MHz	
		Mid-high range (DRS=10) $2197 \times f_{fll\_ref}$	—	71.99	—	MHz	
		High range (DRS=11) $2929 \times f_{fll\_ref}$	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{DCO} = 48 MHz • f_{DCO} = 98 MHz		— —	180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	6
PLL							
f_{vco}	VCO operating frequency		48.0	—	100	MHz	
I_{pll}	PLL operating current • PLL @ 96 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 48)		—	1060	—	µA	7
I_{pll}	PLL operating current • PLL @ 48 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 24)		—	600	—	µA	7
f_{pll_ref}	PLL reference frequency range		2.0	—	4.0	MHz	
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 48 MHz • f_{vco} = 100 MHz		— —	120 50	— —	ps ps	8
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS) • f_{vco} = 48 MHz • f_{vco} = 100 MHz		— —	1350 600	— —	ps ps	8
D_{lock}	Lock entry frequency tolerance		± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance		± 4.47	—	± 5.97	%	

Table continues on the next page...

Table 16. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	—	μA	
	• 4 MHz	—	400	—	μA	
	• 8 MHz (RANGE=01)	—	500	—	μA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x,C_y can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

$$\text{Writes\_subsystem} = \frac{\text{EEPROM} - 2 \times \text{EEESPLIT} \times \text{EEESIZE}}{\text{EEESPLIT} \times \text{EEESIZE}} \times \text{Write\_efficiency} \times n_{nvmcycd}$$

where

- Writes_subsystem — minimum number of writes to each FlexRAM location for subsystem (each subsystem can have different endurance)
- EEPROM — allocated FlexNVM for each EEPROM subsystem based on DEPART; entered with the Program Partition command
- EEESPLIT — FlexRAM split factor for subsystem; entered with the Program Partition command
- EEESIZE — allocated FlexRAM based on DEPART; entered with the Program Partition command
- Write_efficiency —
  - 0.25 for 8-bit writes to FlexRAM
  - 0.50 for 16-bit or 32-bit writes to FlexRAM
- $n_{nvmcycd}$ — data flash cycling endurance (the following graph assumes 10,000 cycles)

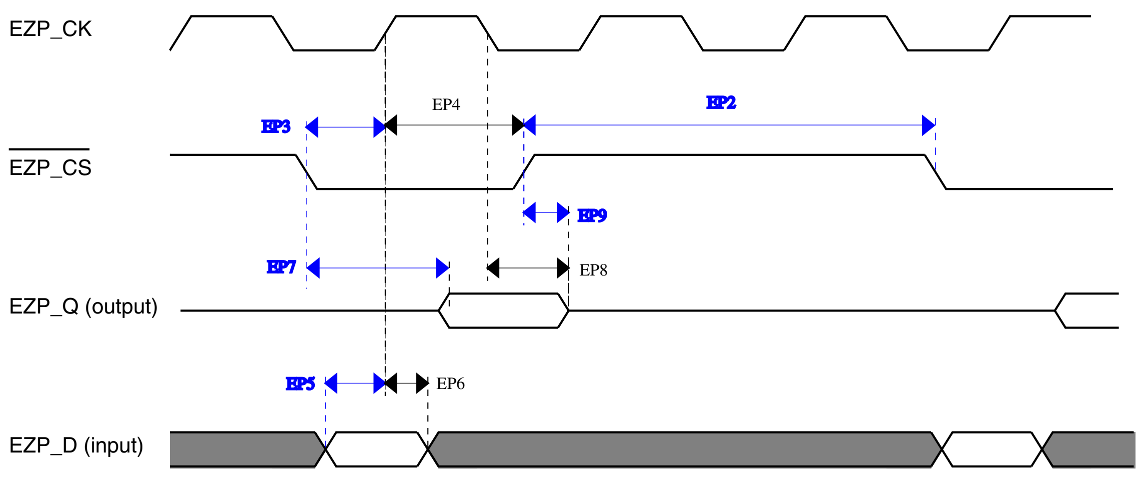


Figure 10. EzPort Timing Diagram

6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

6.6 Analog

6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 25 and Table 26 are achievable on the differential pins ADCx_DP0, ADCx_DM0, ADCx_DP1, ADCx_DM1, ADCx_DP3, and ADCx_DM3.

The ADCx_DP2 and ADCx_DM2 ADC inputs are connected to the PGA outputs and are not direct device pins. Accuracy specifications for these pins are defined in Table 27 and Table 28.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

Table 28. 16-bit ADC with PGA characteristics (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
$V_{PP,DIFF}$	Maximum differential input signal swing		$\left(\frac{(\min(V_x, V_{DDA}-V_x)-0.2)\times 4}{\text{Gain}}\right)$ where $V_X = V_{REFPGA} \times 0.583$			V	6
SNR	Signal-to-noise ratio	• Gain=1 • Gain=64	80 52	90 66	— —	dB dB	16-bit differential mode, Average=32
THD	Total harmonic distortion	• Gain=1 • Gain=64	85 49	100 95	— —	dB dB	16-bit differential mode, Average=32, f_{in}=100Hz
SFDR	Spurious free dynamic range	• Gain=1 • Gain=64	85 53	105 88	— —	dB dB	16-bit differential mode, Average=32, f_{in}=100Hz
ENOB	Effective number of bits	• Gain=1, Average=4 • Gain=1, Average=8 • Gain=64, Average=4 • Gain=64, Average=8 • Gain=1, Average=32 • Gain=2, Average=32 • Gain=4, Average=32 • Gain=8, Average=32 • Gain=16, Average=32 • Gain=32, Average=32 • Gain=64, Average=32	11.6 8.0 7.2 6.3 12.8 11.0 7.9 7.3 6.8 6.8 7.5	13.4 13.6 9.6 9.6 14.5 14.3 13.8 13.1 12.5 11.5 10.6	— — — — — — — — — — —	bits bits bits bits bits bits bits bits bits bits bits	16-bit differential mode,f_{in}=100Hz
SINAD	Signal-to-noise plus distortion ratio	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	

1. Typical values assume V_{DDA} =3.0V, Temp=25°C, f_{ADCK}=6MHz unless otherwise stated.
2. This current is a PGA module adder, in addition to ADC conversion currents.
3. Between IN+ and IN-. The PGA draws a DC current from the input terminals. The magnitude of the DC current is a strong function of input common mode voltage (V_{CM}) and the PGA gain.
4. Gain = 2^{PGAG}
5. After changing the PGA gain setting, a minimum of 2 ADC+PGA conversions should be ignored.
6. Limit the input signal swing so that the PGA does not saturate during operation. Input signal swing is dependent on the PGA reference voltage and gain setting.

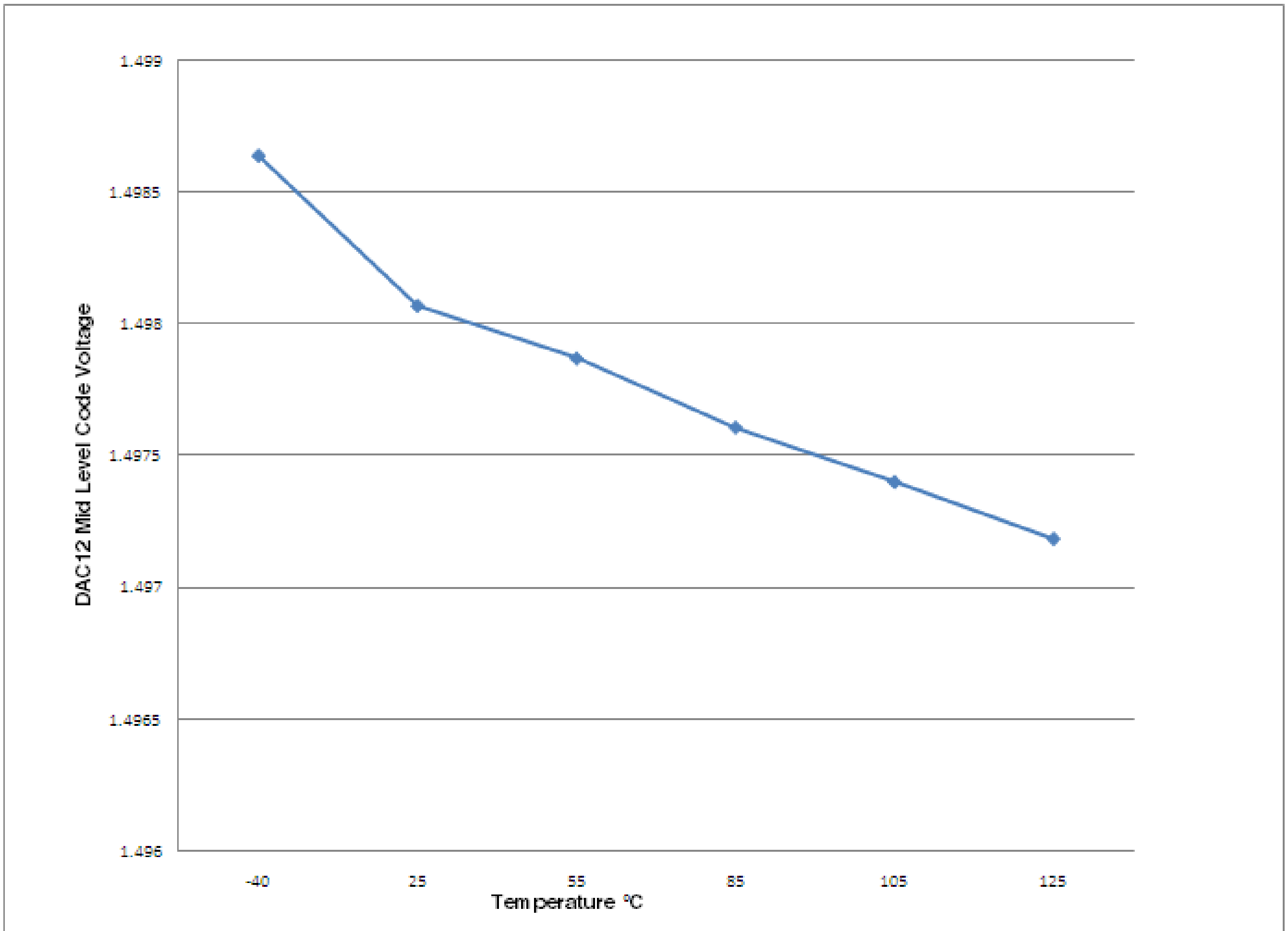


Figure 17. Offset at half scale vs. temperature

6.6.4 Op-amp electrical specifications

Table 32. Op-amp electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	1.71	—	3.6	V
I_{SUPPLY}	Supply current (I_{OUT}=0mA, CL=0), low-power mode	—	92	195	µA
I_{SUPPLY}	Supply current (I_{OUT}=0mA, CL=0), high-speed mode	—	465	865	µA
V_{OS}	Input offset voltage	—	±3	±10	mV
α_{VOS}	Input offset voltage temperature coefficient	—	10	—	µV/C
I_{OS}	Typical input offset current across the following temp range (0–50°C)	—	±500	—	pA
I_{OS}	Typical input offset current across the following temp range (-40–105°C)	—	4	—	nA

Table continues on the next page...

Table 38. VREF full-range operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{tdrift}	Temperature drift (Vmax -Vmin across the full temperature range)	—	—	80	mV	
I_{bg}	Bandgap only current	—	—	80	μA	1
I_{lp}	Low-power buffer current	—	—	360	uA	1
I_{hp}	High-power buffer current	—	—	1	mA	1
ΔV_{LOAD}	Load regulation • current = ± 1.0 mA	—	200	—	μV	1, 2
T_{stup}	Buffer startup time	—	—	100	μs	
V_{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 39. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	°C	

Table 40. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	1.173	1.225	V	

6.7 Timers

See General switching specifications.

6.8 Communication interfaces

6.8.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit **usb.org**.

6.8.2 USB DCD electrical specifications

Table 41. USB DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DP_SRC}	USB_DP source voltage (up to 250 μA)	0.5	—	0.7	V
V_{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I_{DP_SRC}	USB_DP source current	7	10	13	μA
I_{DM_SINK}	USB_DM sink current	50	100	150	μA
R_{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	—	24.8	kΩ
V_{DAT_REF}	Data detect voltage	0.25	0.33	0.4	V

6.8.3 USB VREG electrical specifications

Table 42. USB VREG electrical specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I_{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	120	186	μA	
I_{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	10	μA	
I_{DDoff}	Quiescent current — Shutdown mode • VREGIN = 5.0 V and temperature=25 °C • Across operating voltage and temperature	 — —	 650 —	 — 4	 nA μA	
$I_{LOADrun}$	Maximum load current — Run mode	—	—	120	mA	
$I_{LOADstby}$	Maximum load current — Standby mode	—	—	1	mA	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) > 3.6 V • Run mode • Standby mode	 3 2.1	 3.3 2.8	 3.6 3.6	 V V	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C_{OUT}	External output capacitor	1.76	2.2	8.16	μF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I_{LIM}	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

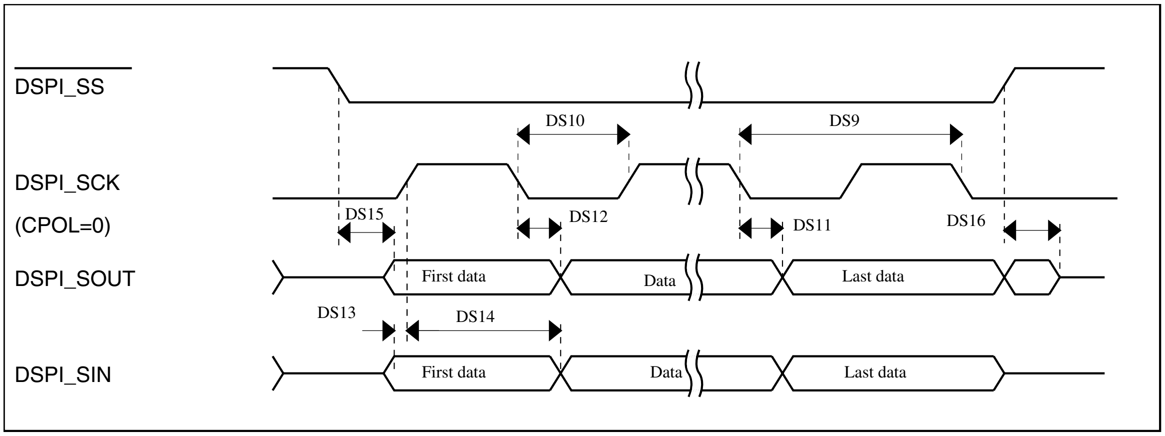


Figure 21. DSPI classic SPI timing — slave mode

6.8.6 Inter-Integrated Circuit Interface (I^2C) timing

Table 47. I^2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I_2C bus devices	t_{HD}; DAT	0[1]	3.45[2]	0[3]	0.9[1]	µs
Data set-up time	t_{SU}; DAT	250[4]	—	100[2, 5]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[6]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[5]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
3. Input signal Slew = 10 ns and Output Load = 50 pF
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode I^2C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\,DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\,DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I^2C bus specification) before the SCL line is released.

Table 49. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (limited voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	15	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

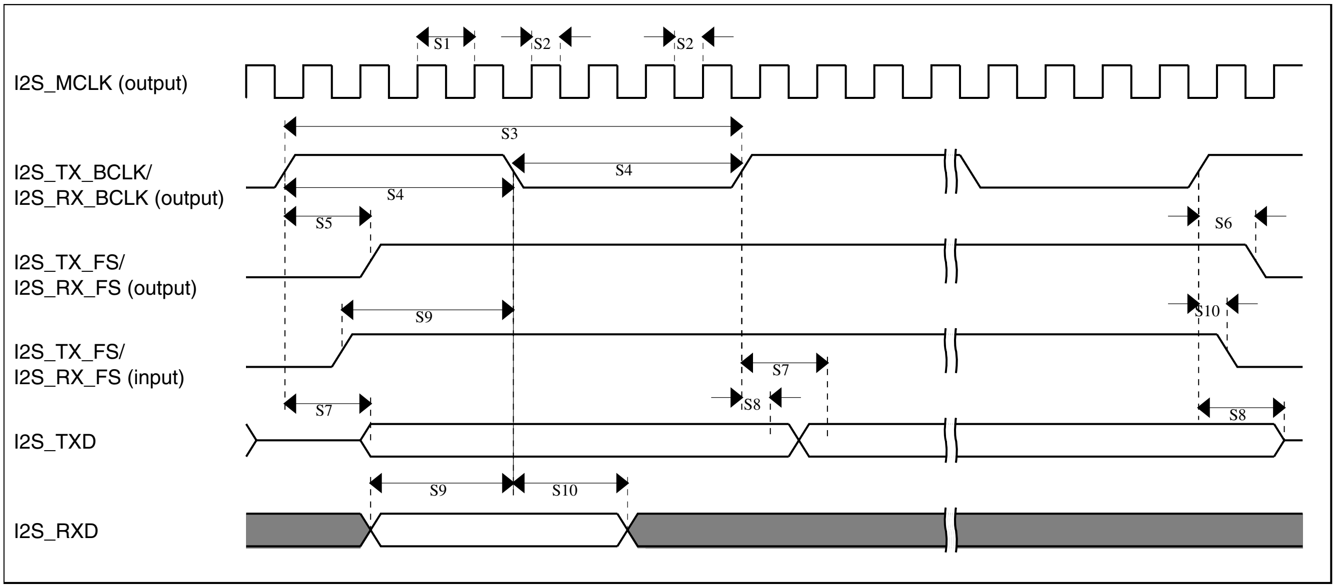


Figure 24. I2S/SAI timing — master modes

Table 50. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (limited voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	4.5	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid • Multiple SAI Synchronous mode • All other modes	 — —	 21 15	ns

Table continues on the next page...

121 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
A10	VLL2	VLL2	VLL2								
A9	VLL1	VLL1	VLL1								
B11	VCAP2	VCAP2	VCAP2								
C11	VCAP1	VCAP1	VCAP1								
A8	PTC4/ LLWU_P8	LCD_P24	LCD_P24	PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT	LCD_P24	
D7	PTC5/ LLWU_P9	LCD_P25	LCD_P25	PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0		CMP0_OUT	LCD_P25	
C7	PTC6/ LLWU_P10	LCD_P26/ CMP0_IN0	LCD_P26/ CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_BCLK		I2S0_MCLK	LCD_P26	
B7	PTC7	LCD_P27/ CMP0_IN1	LCD_P27/ CMP0_IN1	PTC7	SPI0_SIN	USB_SOF_ OUT	I2S0_RX_FS			LCD_P27	
A7	PTC8	LCD_P28/ ADC1_SE4b/ CMP0_IN2	LCD_P28/ ADC1_SE4b/ CMP0_IN2	PTC8			I2S0_MCLK			LCD_P28	
D6	PTC9	LCD_P29/ ADC1_SE5b/ CMP0_IN3	LCD_P29/ ADC1_SE5b/ CMP0_IN3	PTC9			I2S0_RX_BCLK		FTM2_FLT0	LCD_P29	
C6	PTC10	LCD_P30/ ADC1_SE6b	LCD_P30/ ADC1_SE6b	PTC10	I2C1_SCL		I2S0_RX_FS			LCD_P30	
C5	PTC11/ LLWU_P11	LCD_P31/ ADC1_SE7b	LCD_P31/ ADC1_SE7b	PTC11/ LLWU_P11	I2C1_SDA		I2S0_RXD1			LCD_P31	
B6	PTC12	LCD_P32	LCD_P32	PTC12		UART4_RTS_b				LCD_P32	
A6	PTC13	LCD_P33	LCD_P33	PTC13		UART4_CTS_b				LCD_P33	
A5	PTC14	LCD_P34	LCD_P34	PTC14		UART4_RX				LCD_P34	
B5	PTC15	LCD_P35	LCD_P35	PTC15		UART4_TX				LCD_P35	
D5	PTC16	LCD_P36	LCD_P36	PTC16		UART3_RX				LCD_P36	
C4	PTC17	LCD_P37	LCD_P37	PTC17		UART3_TX				LCD_P37	
B4	PTC18	LCD_P38	LCD_P38	PTC18		UART3_RTS_b				LCD_P38	
A4	PTC19	LCD_P39	LCD_P39	PTC19		UART3_CTS_b				LCD_P39	
D4	PTD0/ LLWU_P12	LCD_P40	LCD_P40	PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_b				LCD_P40	
D3	PTD1	LCD_P41/ ADC0_SE5b	LCD_P41/ ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_b				LCD_P41	
C3	PTD2/ LLWU_P13	LCD_P42	LCD_P42	PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX				LCD_P42	
B3	PTD3	LCD_P43	LCD_P43	PTD3	SPI0_SIN	UART2_TX				LCD_P43	
A3	PTD4/ LLWU_P14	LCD_P44	LCD_P44	PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4		EWM_IN	LCD_P44	
A2	PTD5	LCD_P45/ ADC0_SE6b	LCD_P45/ ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_ b/ UART0_COL_b	FTM0_CH5		EWM_OUT_b	LCD_P45	
B2	PTD6/ LLWU_P15	LCD_P46/ ADC0_SE7b	LCD_P46/ ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6		FTM0_FLT0	LCD_P46	
A1	PTD7	LCD_P47	LCD_P47	PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1	LCD_P47	

	1	2	3	4	5	6	7	8	9	10	11	
A	PTD7	PTD5	PTD4/ LLWU_P14	PTC19	PTC14	PTC13	PTC8	PTC4/ LLWU_P8	VLL1	VLL2	VLL3	A
B	PTD10	PTD6/ LLWU_P15	PTD3	PTC18	PTC15	PTC12	PTC7	PTC3/ LLWU_P7	PTC0	PTB16	VCAP2	B
C	PTD12	PTD11	PTD2/ LLWU_P13	PTC17	PTC11/ LLWU_P11	PTC10	PTC6/ LLWU_P10	PTC2	PTB19	PTB11	VCAP1	C
D	PTD14	PTD13	PTD1	PTD0/ LLWU_P12	PTC16	PTC9	PTC5/ LLWU_P9	PTC1/ LLWU_P6	PTB18	PTB10	PTB8	D
E	PTD15	PTE2/ LLWU_P1	PTE1/ LLWU_P0	PTE0	VDD	VDD	VDD	PTB23	PTB17	PTB9	PTB7	E
F	USB0_DP	USB0_DM	PTE6	PTE3	VDDA	VSSA	VSS	PTB22	PTB21	PTB20	PTB6	F
G	VOUT33	VREGIN	VSS	PTE5	VREFH	VREFL	VSS	PTB3	PTB2	PTB1	PTB0/ LLWU_P5	G
H	ADC0_DP1/ OP0_DP0	ADC0_DM1/ OP0_DM0	ADC0_SE16/ OP0_OUT/ CMP1_IN2/ ADC0_SE21/ OP0_DP1/ OP1_DP1	TRI0_DM	TRI1_DM	TRI1_OUT CMP2_IN5/ ADC1_SE22	PTE4/ LLWU_P2	PTA1	PTA3	PTA17	PTA29	H
J	ADC1_DP1/ OP1_DP0/ OP1_DM1	ADC1_DM1/ OP1_DM0	ADC1_SE16/ OP1_OUT/ CMP2_IN2/ ADC0_SE22/ OP0_DP2/ OP1_DP2	TRI0_DP	TRI1_DP	PTA0	PTA2	PTA4/ LLWU_P3	PTA10	PTA16	RESET_b	J
K	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	TRI0_OUT/ OP1_DM2	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23/ OP0_DP5/ OP1_DP5	DAC0_OUT/ CMP1_IN3/ ADC0_SE23/ OP0_DP4/ OP1_DP4	VBAT	PTA5	PTA12	PTA14	VSS	PTA19	K
L	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	XTAL32	EXTAL32	VSS	RTC_ WAKEUP_B	PTA13/ LLWU_P4	PTA15	VDD	PTA18	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 30. K51 121 MAPBGA Pinout Diagram

9 Revision history

The following table provides a revision history for this document.

Table 57. Revision history

Rev. No.	Date	Substantial Changes
1	6/2012	Initial public revision
2	12/2012	Replaced TBDs throughout.

Table continues on the next page...