Cypress Semiconductor Corp - MB9BF122LPMC1-G-JNE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CSIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 23x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/rochester-electronics/mb9bf122lpmc1-g-jne2

Multi-Function Timer
The multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3ch./unit
- Input capture × 4ch./unit
- Output compare × 6ch./unit
- A/D activation compare × 2ch./unit
- Waveform generator × 3ch./unit
- 16-bit PPG timer × 3ch./unit

The following functions can be used to achieve motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D converter activate function
- DTIF (motor emergency stop) interrupt function

Real-Time Clock (RTC)
The real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 01 to 99.

- The interrupt function with specifying date and time (Year/Month/Day/Hour/Minute/Second/A day of the week.) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

Watch Counter
The watch counter is used for wake up from the Sleep and Timer mode.

Interval timer: up to 64s (Max) @ Sub Clock: 32.768 kHz

External Interrupt Controller Unit

- Up to 23 external interrupt input pins @ 80 pin Package
- Include one non-maskable interrupt (NMI) input pin

Watchdog Timer (Two channels)
A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a “Hardware” watchdog and a “Software” watchdog.

The “Hardware” watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the “Hardware” watchdog is active in any low-power consumption modes except RTC, Stop, Deep Standby RTC, Deep Standby Stop modes.

CRC (Cyclic Redundancy Check) Accelerator
The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

Clock and Reset

[Clocks]
Selectable from five clock sources (2 external oscillators, 2 built-in CR oscillator, and Main PLL).

- Main Clock : 4 MHz to 48 MHz
- Sub Clock : 32.768 kHz
- Built-in High-speed CR Clock : 4 MHz
- Built-in Low-speed CR Clock : 100 kHz
- Main PLL Clock

[Resets]

- Reset requests from INITX pin
- Power-on reset
- Software reset
- Watchdog timers reset
- Low-voltage detection reset
- Clock Super Visor reset

Clock Super Visor (CSV)
Clocks generated by built-in CR oscillators are used to supervise abnormality of the external clocks.

- If external clock failure (clock stop) is detected, reset is asserted.
- If external frequency anomaly is detected, interrupt or reset is asserted.

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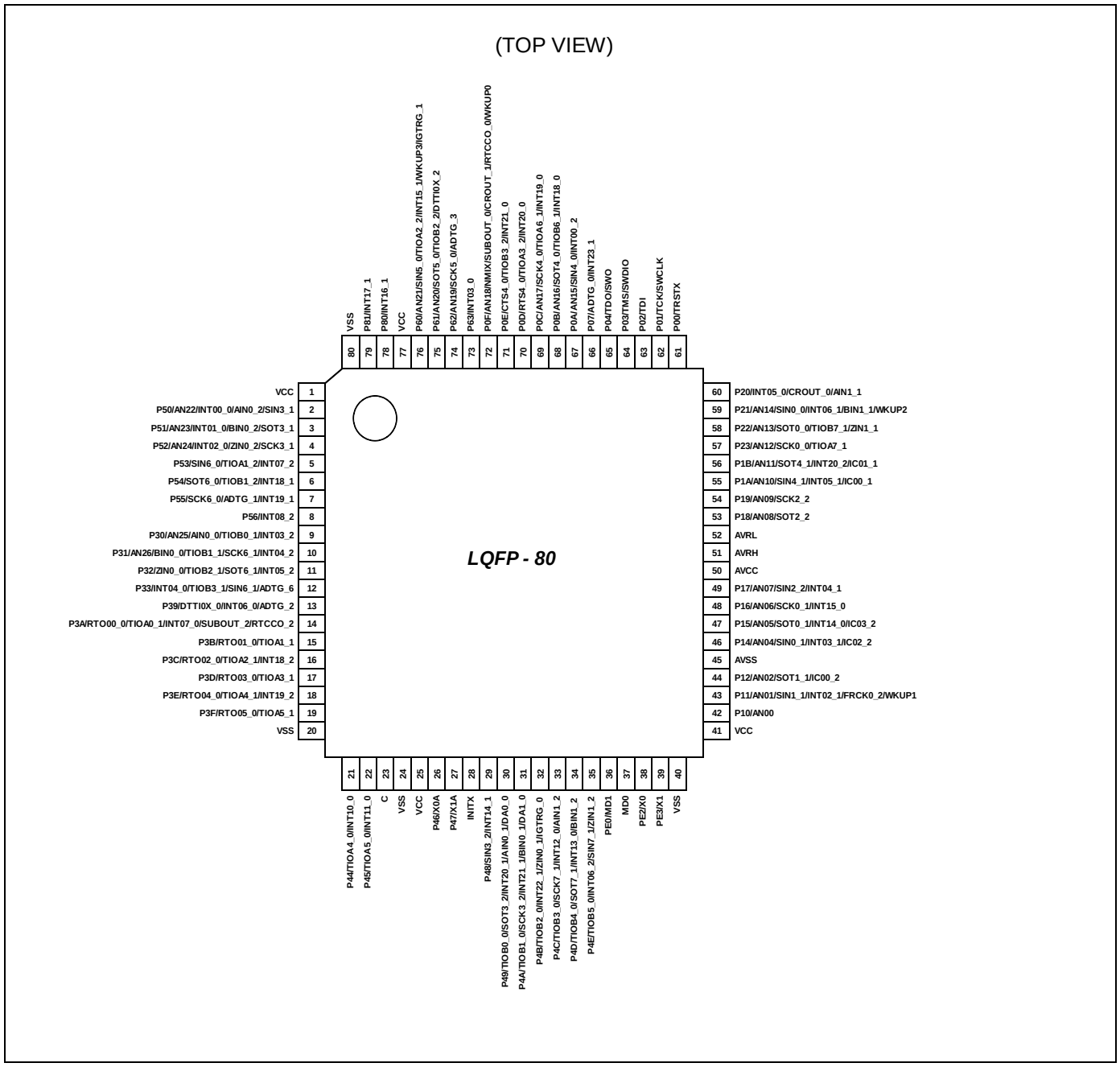
3. Pin Assignment

FPT-80-M37/M40



Note:

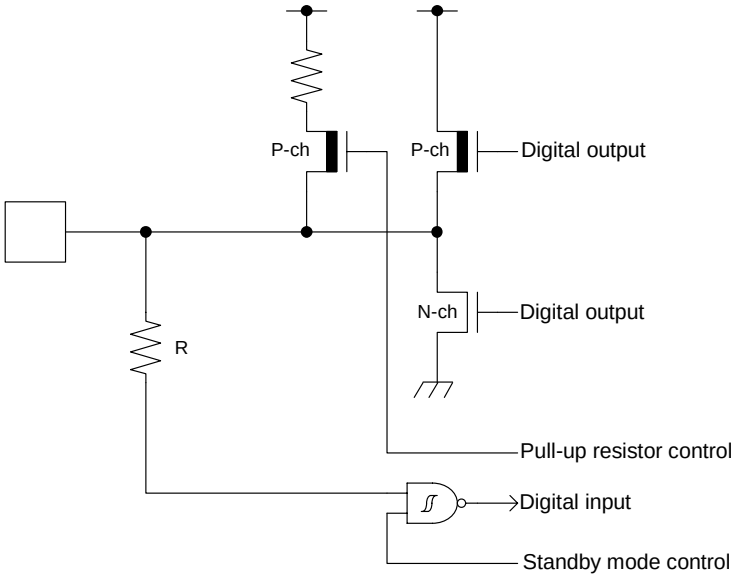
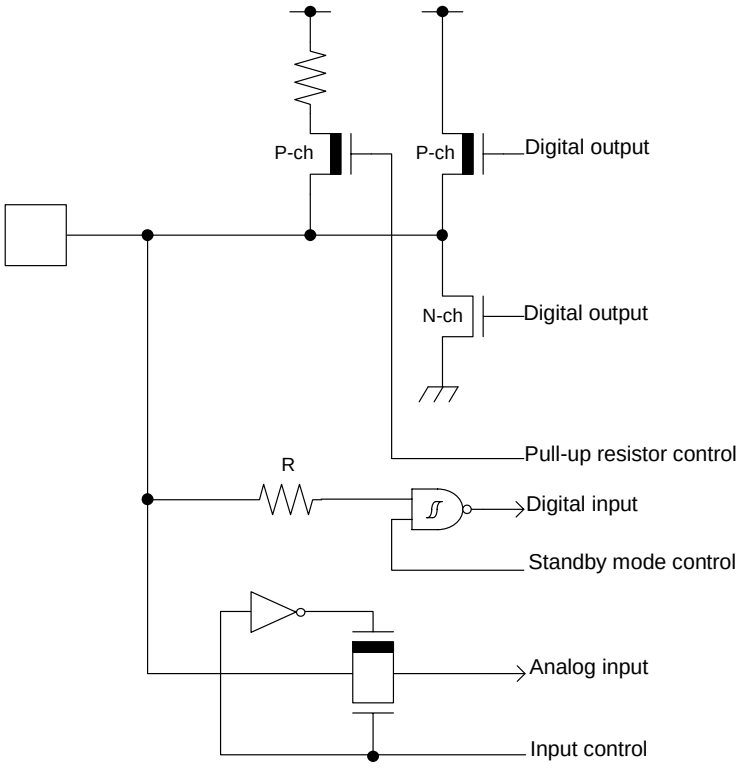
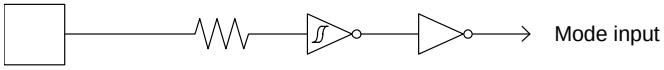
The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
55	E10	-	-	P1A AN10 SIN4_1 INT05_1 IC00_1	F	N
56	E9	-	-	P1B AN11 SOT4_1 (SDA4_1) IC01_1 INT20_2	F	N
57	D10	46	34	P23 SCK0_0 (SCL0_0) TIOA7_1 AN12	F	M
58	D9	47	35	P22 SOT0_0 (SDA0_0) TIOB7_1 AN13	F	M
		-	-	ZIN1_1		
59	C11	48	36	P21 SIN0_0 INT06_1 WKUP2 BIN1_1 AN14	F	N
60	C10	-	-	P20 INT05_0 CROUT_0 AIN1_1	E	N
61	A10	49	37	P00 TRSTX	E	J
62	B9	50	38	P01 TCK SWCLK	E	J
63	B11	51	39	P02 TDI	E	J
64	A9	52	40	P03 TMS SWDIO	E	J
65	B8	53	41	P04 TDO SWO	E	J
66	A8	-	-	P07 ADTG_0 INT23_1	E	L
67	C8	54	-	P0A SIN4_0 INT00_2 AN15	J*	N

List of functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin function	Pin name	Function description	Pin No			
			LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48
ADC	ADTG_0	A/D converter external trigger input pin	66	A8	-	-
	ADTG_1		7	D3	-	-
	ADTG_2		13	G3	9	5
	ADTG_3		74	C5	58	-
	ADTG_6		12	G2	8	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	42	J11	34	25
	AN01		43	J10	35	26
	AN02		44	J8	36	27
	AN04		46	H9	38	29
	AN05		47	G10	39	30
	AN06		48	G9	-	-
	AN07		49	F10	40	-
	AN08		53	F9	44	-
	AN09		54	E11	45	-
	AN10		55	E10	-	-
	AN11		56	E9	-	-
	AN12		57	D10	46	34
	AN13		58	D9	47	35
	AN14		59	C11	48	36
	AN15		67	C8	54	-
	AN16		68	C7	55	-
	AN17		69	B7	56	-
	AN18		72	A6	57	42
	AN19		74	C5	58	-
	AN20		75	B4	59	43
	AN21		76	C4	60	44
	AN22		2	C1	2	2
	AN23		3	C2	3	3
	AN24		4	B3	4	4
	AN25		9	E2	5	-
	AN26		10	E3	6	-
Base Timer 0	TIOA0_1	Base timer ch.0 TIOA pin	14	H1	10	6
	TIOB0_0	Base timer ch.0 TIOB pin	30	K6	22	18
	TIOB0_1		9	E2	5	-
Base Timer 1	TIOA1_1	Base timer ch.1 TIOA pin	15	H2	11	7
	TIOA1_2		5	D1	-	-
	TIOB1_0	Base timer ch.1 TIOB pin	31	J6	23	19
	TIOB1_1		10	E3	6	-
	TIOB1_2		6	D2	-	-
Base Timer 2	TIOA2_1	Base timer ch.2 TIOA pin	16	H3	12	8
	TIOA2_2		76	C4	60	44
	TIOB2_0	Base timer ch.2 TIOB pin	32	L7	24	-
	TIOB2_1		11	G1	7	-
	TIOB2_2		75	B4	59	43
Base Timer 3	TIOA3_1	Base timer ch.3 TIOA pin	17	J1	13	9
	TIOA3_2		70	B6	-	-
	TIOB3_0	Base timer ch.3 TIOB pin	33	K7	25	-
	TIOB3_1		12	G2	8	-
	TIOB3_2		71	C6	-	-
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	21	L5	-	-
	TIOA4_1		18	J2	14	10
	TIOB4_0	Base timer ch.4 TIOB pin	34	J7	26	-

Type	Circuit	Remarks
I		• CMOS level output • CMOS level hysteresis input • 5 V tolerant • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA • Available to control PZR registers. • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
J		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • 5 V tolerant • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA • Available to control PZR registers. • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
K		• CMOS level hysteresis input

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Input enabled	GPIO selected	Hi-Z / Input enabled	GPIO selected
F	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Sub crystal oscillator input pin / External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
G	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	External sub clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at "0"/ or Input enable	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state	Maintain previous state/ When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state/ When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state/ When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state/ When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state/ When oscillation stops*2, Hi-Z / Internal input fixed at "0"
H	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage *1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage *1, *3	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage *1, *3	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage *1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5V tolerant
Analog pin input voltage *1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5V)	V	
Output voltage *1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5V)	V	
Clamp maximum current	I_{CLAMP}	-2	+2	mA	*7
Clamp total maximum current	$\sum [I_{CLAMP}]$		+20	mA	*7
"L" level maximum output current *4	I_{OL}	-	10	mA	4mA type
			20	mA	12mA type
			39	mA	P80/P81 pin
"L" level average output current *5	I_{OLAV}	-	4	mA	4mA type
			12	mA	12mA type
			16.5	mA	P80/P81 pin
"L" level total maximum output current	$\sum I_{OL}$	-	100	mA	
"L" level total maximum output current *8	$\sum I_{OLAV}$	-	50	mA	
"H" level maximum output current *6	I_{OH}	-	- 10	mA	4mA type
			- 20	mA	12mA type
			- 39	mA	P80/P81 pin
"H" level average output current *7	I_{OHAV}	-	- 4	mA	4mA type
			- 12	mA	12mA type
			- 18	mA	P80/P81 pin
"H" level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
"H" level total average output current *8	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	300	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0$ V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: Ensure that the voltage does not exceed V_{CC} + 0.5 V, for example, when the power is turned on.

*4: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*5: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100 ms period.

*6: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100 ms period.

12.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = AVRL = 0.0V)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply voltage	V_{CC}	-	2.7*2	5.5	V	
Analog power supply voltage	AV_{CC}	-	2.7	5.5	V	AV_{CC}=V_{CC}
Analog reference voltage	AVRH	-	2.7	AV_{CC}	V	
	AVRL		AV_{SS}	AV_{SS}	V	
Smoothing capacitor	C_S	-	1	10	µF	For Regulator*1
Operating temperature	T_A	-	- 40	+ 105	°C	

*1: See "C Pin" in "Handling Devices" for the connection of the smoothing capacitor.

*2: In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR (including Main PLL is used) or built-in Low-speed CR is possible to operate only.

WARNING

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

12.3.2 Pin Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	-	V_{CC} × 0.8	-	V_{CC} + 0.3	V	
		5V tolerant input pin	-	V_{CC} × 0.8	-	V_{SS} + 5.5	V	
L level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	-	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
		5 V tolerant input pin	-	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
H level output voltage	V_{OH}	4 mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 2 mA					
		12 mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 12 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 8 mA					
		P80, P81	V_{CC} ≥ 4.5 V, I_{OH} = - 18.0 mA	V_{CC} - 0.4	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 12.0 mA					
L level output voltage	V_{OL}	4 mA type	V_{CC} ≥ 4.5 V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			V_{CC} < 4.5 V, I_{OL} = 2 mA					
		12 mA type	V_{CC} ≥ 4.5 V, I_{OL} = 12 mA	V_{SS}	-	0.4	V	
			V_{CC} < 4.5 V, I_{OL} = 8 mA					
		P80, P81	V_{CC} ≥ 4.5 V, I_{OL} = 16.5 mA	V_{SS}	-	0.4	V	
			V_{CC} < 4.5 V, I_{OL} = 10.5 mA					
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistance value	R_{PU}	Pull-up pin	V_{CC} ≥ 4.5 V	33	50	90	kΩ	
			V_{CC} < 4.5 V	-	-	180		
Input capacitance	C_{IN}	Other than VCC, VSS, AVCC, AVSS, AVRH, AVRL	-	-	5	15	pF	

12.4.9 CSIO/UART Timing

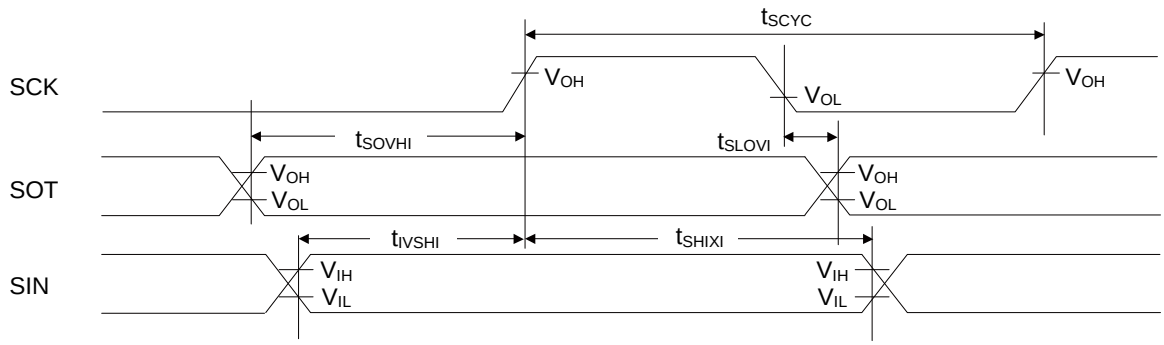
CSIO (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

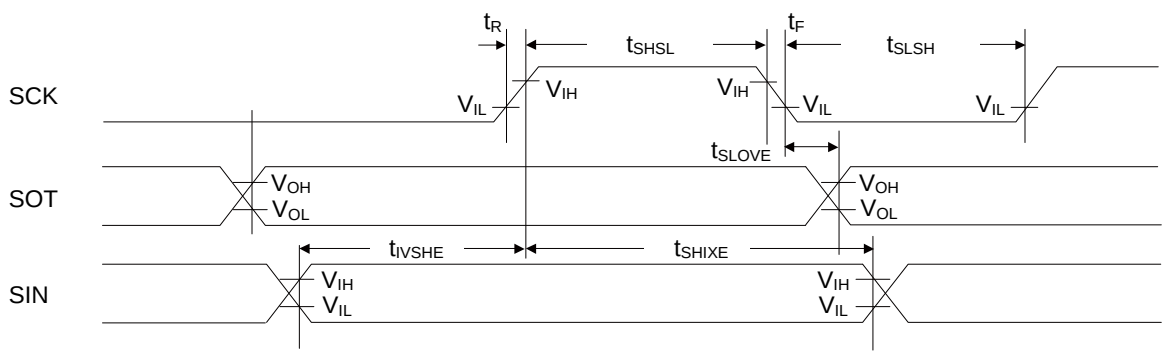
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function serial is connected to, see "Block Diagram" in this data sheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 30 pF.



Master mode

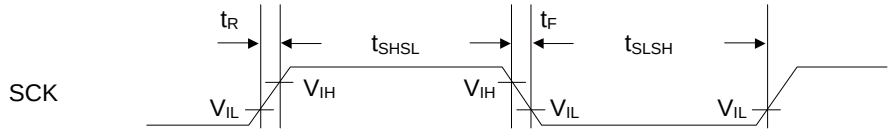


Slave mode

UART external clock input (EXT = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Min	Max	Unit	Remarks
Serial clock L pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock H pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK falling time	t_F		-	5	ns	
SCK rising time	t_R		-	5	ns	



12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-	± 1.5	± 4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential Nonlinearity	-	-	-	± 1.7	± 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	-	± 10	± 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	-	AVRH ± 5	AVRH ± 15	mV	
Conversion time	-	-	0.8*1	-	-	µs	AV_{CC} ≥ 4.5 V
			1.0*1	-	-		AV_{CC} < 4.5 V
Sampling time*2	t_S	-	0.24	-	10	µs	AV_{CC} ≥ 4.5 V
			0.3	-			AV_{CC} < 4.5 V
Compare clock cycle*3	t_{CCK}	-	40	-	1000	ns	AV_{CC} ≥ 4.5 V
			50	-			AV_{CC} < 4.5 V
State transition time to operation permission	t_{STT}	-	-	-	1.0	µs	
Analog input capacity	C_{AIN}	-	-	-	9.7	pF	
Analog input resistor	R_{AIN}	-	-	-	1.7	kΩ	AV_{CC} ≥ 4.5 V
					2.4		AV_{CC} < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AVRL	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	AV_{CC}	V	
	-	AVRL	AV_{SS}	-	AV_{SS}	V	

*1: The conversion time is the value of sampling time (t_S) + compare time (t_C).

The condition of the minimum conversion time is the following.

AV_{CC} ≥ 4.5 V, HCLK=50 MHz sampling time: 240 ns, compare time: 560 ns.

AV_{CC} < 4.5 V, HCLK=40 MHz sampling time: 300 ns, compare time: 700 ns

Ensure that it satisfies the value of the sampling time (t_S) and compare clock cycle (t_{CCK}).

For setting of the sampling time and compare clock cycle, see "Chapter 1-1: A/D Converter" in "FM3 Family Peripheral Manual Analog Macro Part".

The register settings of the A/D Converter are reflected in the operation according to the APB bus clock timing.

For the number of the APB bus to which the A/D Converter is connected, see "Block Diagram".

The base clock (HCLK) is used to generate the sampling time and the compare clock cycle.

*2: A necessary sampling time changes by external impedance.
Ensure that it sets the sampling time to satisfy (Equation 1).

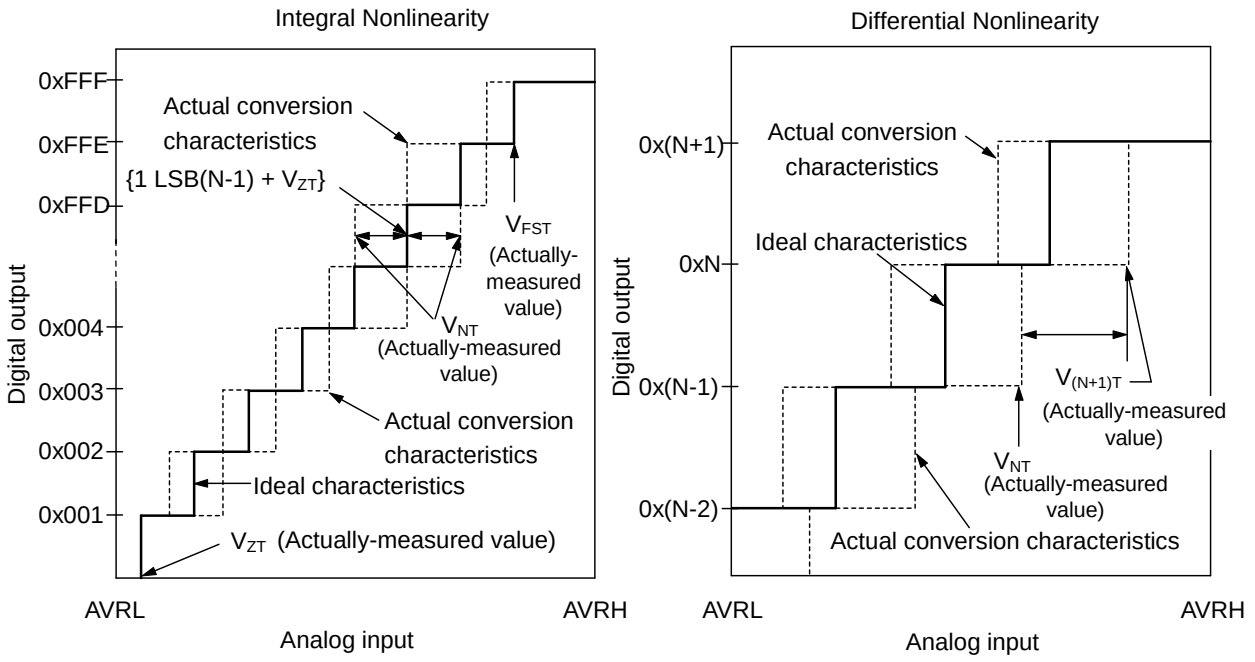
*3: The compare time (t_C) is the value of (Equation 2).

Definition of 12-bit A/D Converter Terms

■Resolution : Analog variation that is recognized by an A/D converter.

■Integral Nonlinearity : Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.

■Differential Nonlinearity : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N : A/D converter digital output value.

V_{ZT} : Voltage at which the digital output changes from 0x000 to 0x001.

V_{FST} : Voltage at which the digital output changes from 0xFFE to 0xFFF.

V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.

12.7 Low-Voltage Detection Characteristics

12.7.1 Low-Voltage Detection Reset

(T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHR*1= 00000	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH		2.30	2.50	2.70	V	When voltage rises
Detected voltage	VDL	SVHR*1= 00001	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH		2.48	2.70	2.92	V	When voltage rises
Detected voltage	VDL	SVHR*1= 00010	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH		2.58	2.80	3.02	V	When voltage rises
Detected voltage	VDL	SVHR*1= 00011	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVHR*1= 00100	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVHR*1= 00101	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		3.04	3.30	3.56	V	When voltage rises
Detected voltage	VDL	SVHR*1= 00110	3.31	3.60	3.89	V	When voltage drops
Released voltage	VDH		3.40	3.70	4.00	V	When voltage rises
Detected voltage	VDL	SVHR*1= 00111	3.40	3.70	4.00	V	When voltage drops
Released voltage	VDH		3.50	3.80	4.10	V	When voltage rises
Detected voltage	VDL	SVHR*1= 01000	3.68	4.00	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.10	4.43	V	When voltage rises
Detected voltage	VDL	SVHR*1= 01001	3.77	4.10	4.43	V	When voltage drops
Released voltage	VDH		3.86	4.20	4.54	V	When voltage rises
Detected voltage	VDL	SVHR*1= 01010	3.86	4.20	4.54	V	When voltage drops
Released voltage	VDH		3.96	4.30	4.64	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	8160 × t_{CYCP}*2	µs	
LVD detection delay time	t_{LVDDL}	-	-	-	200	µs	

*1: The SVHR bit of Low-Voltage Detection Voltage Control Register (LVD_CTL) is initialized to "00000" by Low-Voltage Detection Reset.

*2: t_{CYCP} indicates the APB2 bus clock cycle time.

12.9 Return Time from Low-Power Consumption Mode

12.9.1 Return Factor: Interrupt/WKUP

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

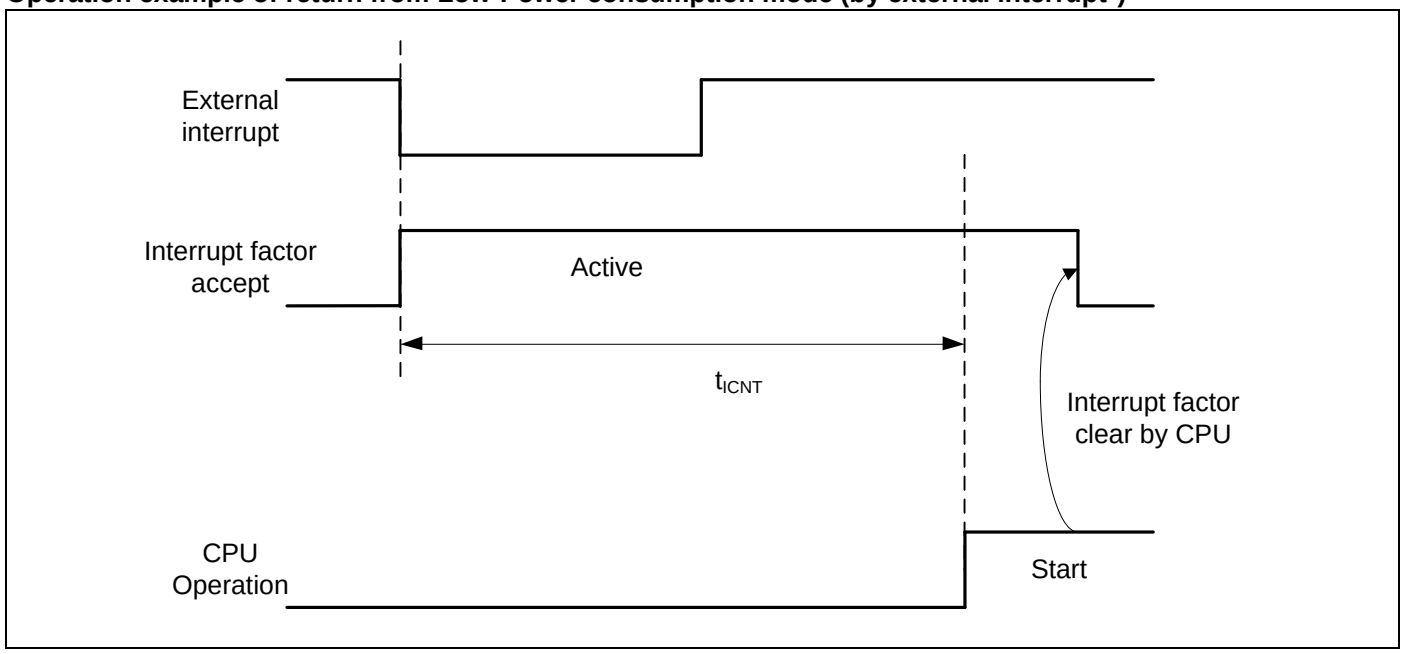
Return Count Time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 105°C)

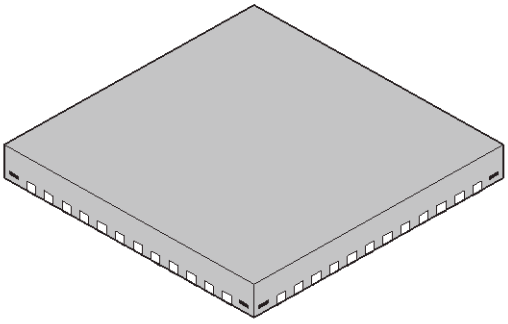
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	tICNT	t_{CYCC}		µs	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		40	80	µs	
Low-speed CR Timer mode		340	680	µs	
Sub Timer mode		680	860	µs	
RTC mode, Stop mode		268	503	µs	
Deep Standby RTC mode		308	583	µs	When RAM is off
Deep Standby Stop mode		268	503	µs	When RAM is on

*: The maximum value depends on the accuracy of built-in CR.

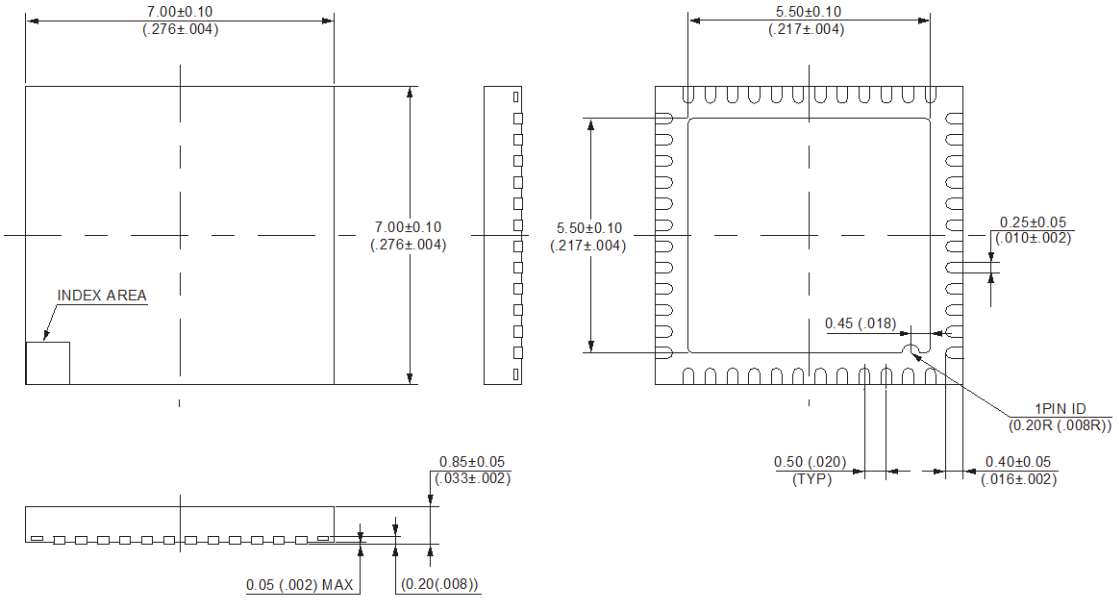
Operation example of return from Low-Power consumption mode (by external interrupt*)



*: External interrupt is set to detecting fall edge.

48-pin plastic QFN		
	Lead pitch	0.5 mm
	Package width × package length	7.00 mm × 7.00 mm
	Sealing method	Plastic mold
	Mounting height	0.90 mm MAX
	Weight	–
(LCC-48P-M73)		

48-pin plastic QFN
(LCC-48P-M73)



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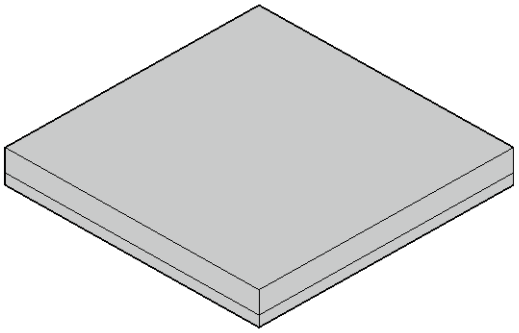
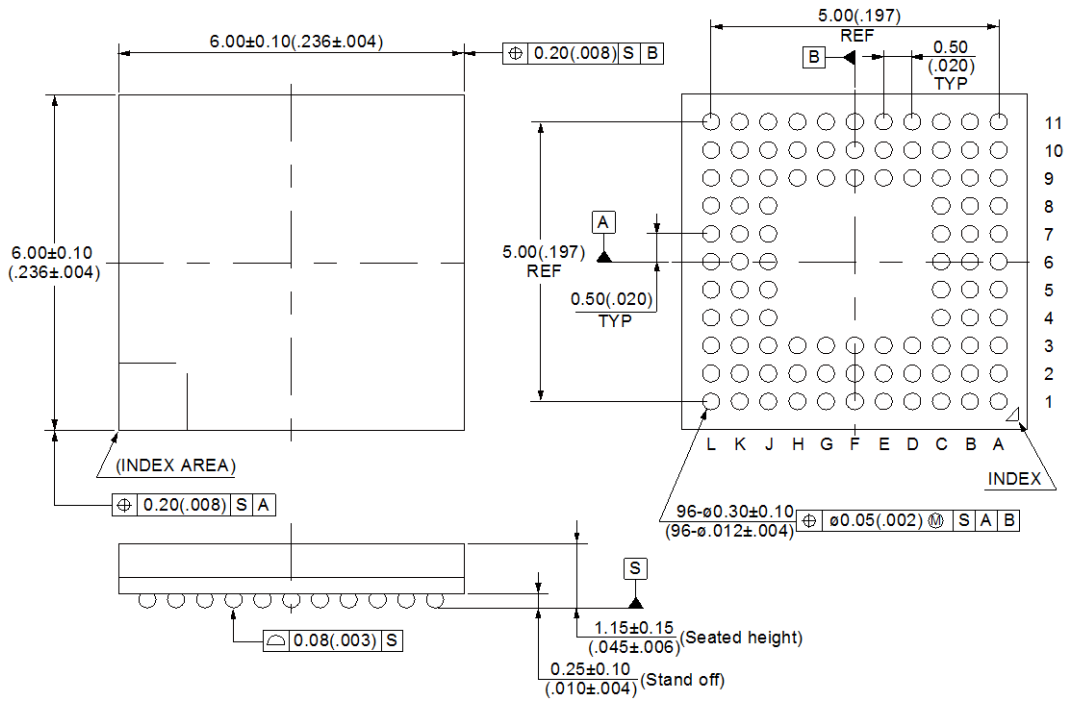
Dimensions in mm (inches).
Note: The values in parentheses are reference **values.**

96-pin plastic FBGA		
	Lead pitch	0.5 mm
	Package width × package length	6.00 mm × 6.00 mm
	Lead shape	Ball
	Sealing method	Plastic mold
	Mounting height	1.30 mm MAX
	Weight	0.08 g
(BGA-96P-M07)		

96-pin plastic FBGA
(BGA-96P-M07)



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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Page	Section	Change Results
20	LIST OF PIN FUNCTIONS List of pin numbers	Corrected the pin number of ZIN1_1.
23	List of pin functions	Corrected the pin number of ADTG_2.
28		Corrected pin numbers of SIN0_1 and SOT0_1.
30		Corrected the pin number of DTTI0X_2.
36	I/O CIRCUIT TYPE	TYPE H : Revised the value of "TBD".
43	HANDLING DEVICES Sub crystal oscillator	Added the descriptions.
46	BLOCK DIAGRAM	Corrected the figure. -A/D Activation Compare: 3ch → 2ch
48	MEMORY MAP Memory Map (2)	Added the explanatory note.
53	PIN STATUS IN EACH CPU STATE List of Pin Status	Added the pin function of selected Analog output about type L.
54		Corrected the footnote. Sub CR timer→ Low-speed CR tim
56	ELECTRICAL CHARACTERISTICS 2. Recommended Operating Conditions	Added the note and footnote. Corrected the value of Analog reference voltage “AVRH”. Min.: AVss → 2.7
57	3. DC Characteristics (1) Current Rating	Added notes and footnotes. Added the remarks of Icc. Added the frequency of main clock crystal oscillator in remarks.
61	4. AC Characteristics (2) Sub clock input Characteristics	Added the footnote.
62	(3) Built-in CR Oscillation Characteristics • Built-in High-speed CR	Added "Frequency stabilization time" Added notes and footnotes.
64	(6) Power-on Reset Timing	Added "Timing until releasing Power-on reset" Added the timing chart
66	(8) CSIO Timing	Corrected the title. UART Timing → CSIO Timing Corrected the footnote. UART → Multi-function serial
68,70,72		Corrected the footnote. UART → Multi-function serial
77	(11) I^2C Timing	Revised the Condition. Revised the footnote.
79	5. 12-bit A/D Converter Electrical characteristics for the A/D converter	Changed the name of parameter. •Non Linearity error → Integral Nonlinearity •Differential linearity error → Differential Nonlinearity Changed the Symbol. Of Zero transition voltage. $Vo_T \rightarrow V_{ZT}$ Changed the pin name. AN00 to AN26 → ANxx Corrected the value of V_{0T}, V_{FST}, Ts, Tstt, and reference voltage. Revised footnotes.
80		Change the figure. AN00 to AN26 → ANxx
81	Definition of 12-bit A/D Converter Terms	•Linearity error → Integral Nonlinearity •Differential linearity error → Differential Nonlinearity $V_{0T} \rightarrow V_{ZT}$
82	6. 10-bit D/A Converter Electrical characteristics for the D/A converter	Revised the remark of IDDA. D/A operation → D/A 1unit operation Changed the name of parameter. •Linearity error → Integral Nonlinearity •Differential linearity error → Differential Nonlinearity
83	7. Low-Voltage Detection Characteristics (1) Low-Voltage Detection Reset	Corrected the condition and the value. Added the note and the footnote. Added “LVD detection delay time”.
84	(2) Interrupt of Low-Voltage Detection	Corrected the condition and the value. Added “LVD detection delay time”.

Page	Section	Change Results
85	8. Flash Memory Write/Erase Characteristics	Changed the title of Chapter. Main Flash Memory Write/Erase Characteristics → Flash Memory Write/Erase Characteristics
86	9. Return Time Low-Power Consumption Mode	Added the Chapter “Return Time from Low-Power Consumption Mode”.
Revision 3.0		
2	Features USB Interface	Added the description of PLL for USB
35, 36	I/O Circuit Type	Added about +B input
48	Memory Map Memory map(2)	Added the summary of Flash memory sector and the note
52	PIN STATUS IN EACH CPU STAE List of Pin Status	Changed the pin status of I-type
55, 56	Electrical Characteristics 1. Absolute Maximum Ratings	Added the Clamp maximum current Added about +B input
58-60	Electrical Characteristics 3. DC Characteristics (1) Current rating	Changed the table format Added Main TIMER mode current Moved A/D Converter Current Moved D/A Converter Current
65	Electrical Characteristics 4. AC Characteristics (4-1) Operating Conditions of Main PLL (4-2) Operating Conditions of Main PLL	· Added the figure of Main PLL connection
68-75	Electrical Characteristics 4. AC Characteristics (7) CSIO/UART Timing	· Modified from UART Timing to CSIO/UART Timing · Changed from Internal shift clock operation to Master mode · Changed from External shift clock operation to Slave mode
76	Electrical Characteristics 4. AC Characteristics (9) External Input Timing	Added input pulse width of WKUPx pin
81	Electrical Characteristics 5. 12bit A/D Converter	· Added the typical value of Integral Nonlinearity, Differential Nonlinearity, Zero transition voltage and Full-scale transition voltage · Added Conversion time at AVcc < 4.5V
92, 93	Ordering Information	Change to full part number

NOTE: Please see “Document History” about later revised information.