Cypress Semiconductor Corp - MB9BF124KPMC-G-JNE2 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CSIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 14x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/rochester-electronics/mb9bf124kpmc-g-jne2

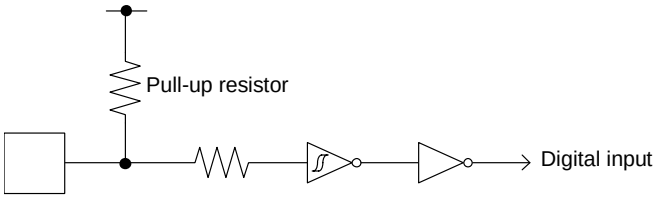
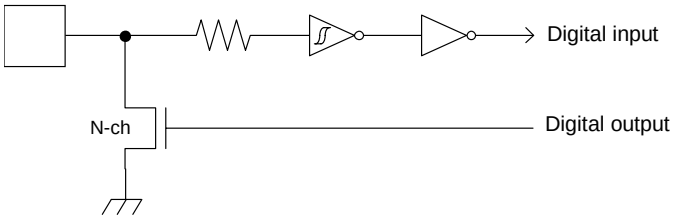
2. Packages

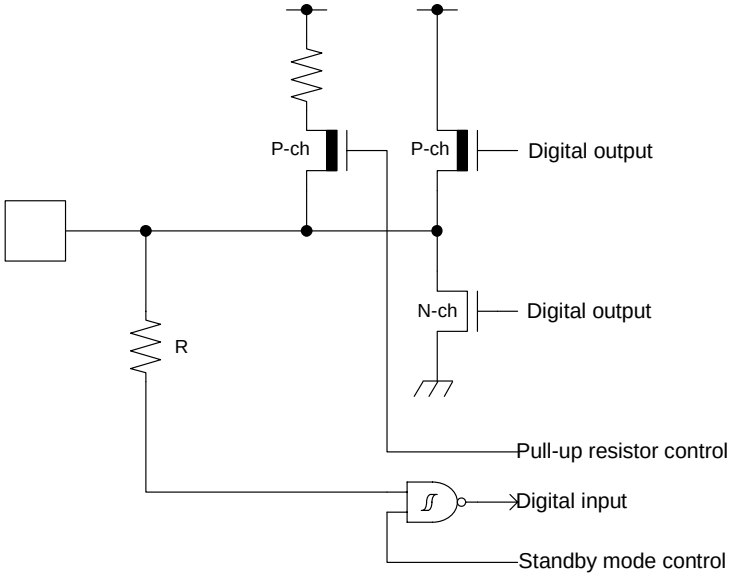
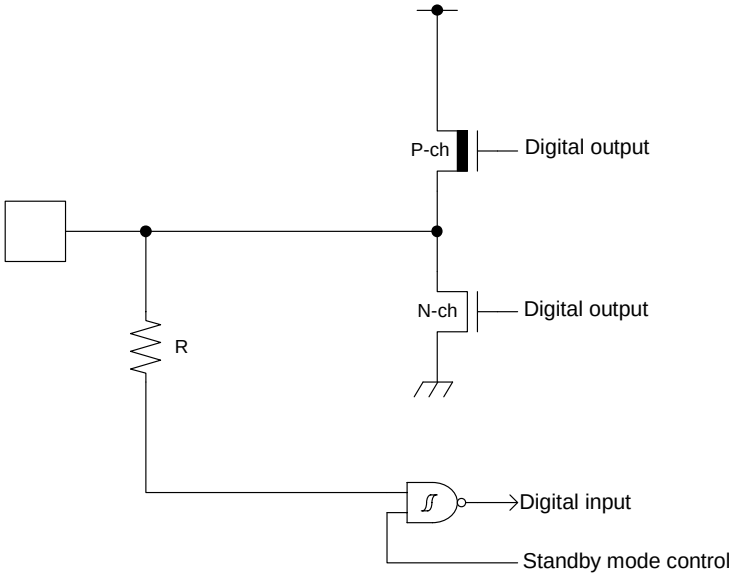
Package / Product name		MB9BF121K MB9BF122K MB9BF124K	MB9BF121L MB9BF122L MB9BF124L	MB9BF121M MB9BF122M MB9BF124M
LQFP:	FPT-48P-M49 (0.5mm pitch)	○	-	-
QFN:	LCC-48P-M73 (0.5mm pitch)	○	-	-
LQFP:	FPT-64P-M38 (0.5mm pitch)	-	○	-
LQFP:	FPT-64P-M39 (0.65mm pitch)	-	○	-
QFP:	LCC-64P-M24 (0.5mm pitch)	-	○	-
LQFP:	FPT-80P-M37 (0.5mm pitch)	-	-	○
LQFP:	FPT-80P-M40 (0.65mm pitch)	-	-	○
BGA:	BGA-96P-M07 (0.5mm pitch)	-	-	○

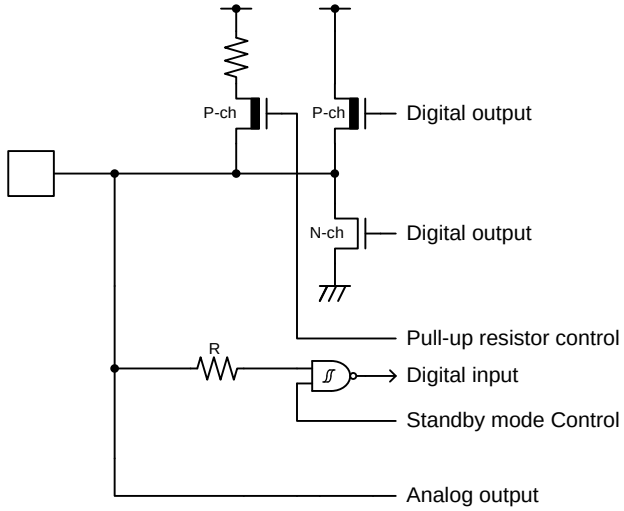
○: Supported

Note: See "Package Dimensions" for detailed information on each package

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
23	L2	17	13	C	-	
24	L4	-	-	VSS	-	
25	K1	18	14	VCC	-	
26	L3	19	15	P46 X0A	D	F
27	K3	20	16	P47 X1A	D	G
28	K4	21	17	INITX	B	C
29	J5	-	-	P48 INT14_1 SIN3_2	E	L
30	K6	22	18	P49 TIOB0_0 INT20_1 DA0_0	L	L
			-	SOT3_2 (SDA3_2) AIN0_1		
31	J6	23	19	P4A TIOB1_0 INT21_1 DA1_0	L	L
			-	SCK3_2 (SCL3_2) BIN0_1		
32	L7	24	-	P4B TIOB2_0 INT22_1 IGTRG_0 ZIN0_1	E	L
33	K7	25	-	P4C TIOB3_0 SCK7_1 (SCL7_1) INT12_0 AIN1_2	I*	L
34	J7	26	-	P4D TIOB4_0 SOT7_1 (SDA7_1) INT13_0 BIN1_2	I*	L
35	K8	27	-	P4E TIOB5_0 INT06_2 SIN7_1 ZIN1_2	I*	L
36	K9	28	20	MD1 PE0	C	E
37	L8	29	21	MD0	K	D

Type	Circuit	Remarks
B		• CMOS level hysteresis input • Pull-up resistor : Approximately 50 kΩ
C		• Open drain output • CMOS level hysteresis input

Type	Circuit	Remarks
G		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -12 mA, I_{OL}= 12 mA • +B input is available
H		• CMOS level output • CMOS level hysteresis input • With standby mode control • I_{OH} = -18 mA, I_{OL} = 16.5 mA

Type	Circuit	Remarks
L		• CMOS level output • CMOS level hysteresis input • With input control • Analog output • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.
2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.
3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

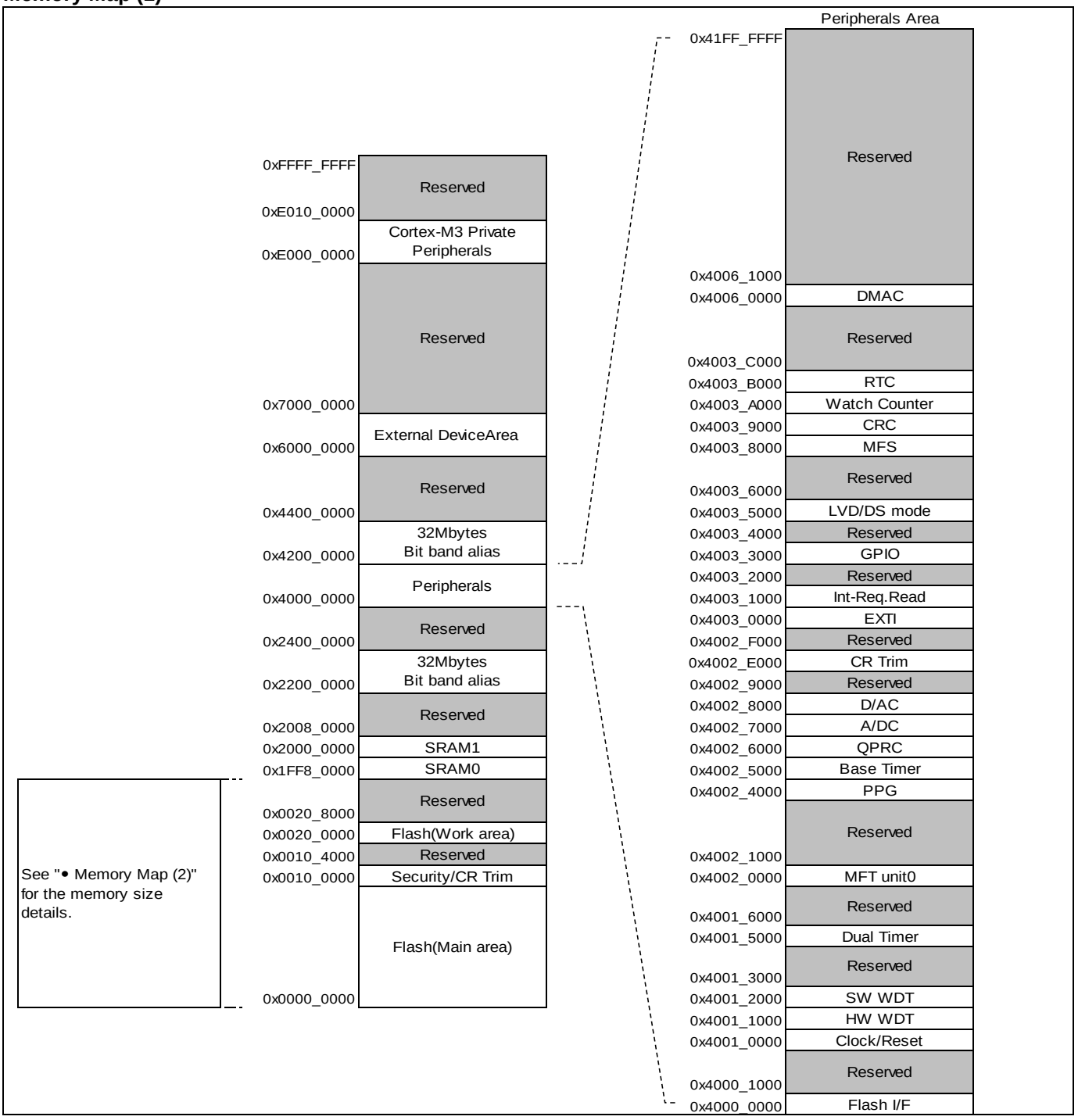
Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

9. Memory Size

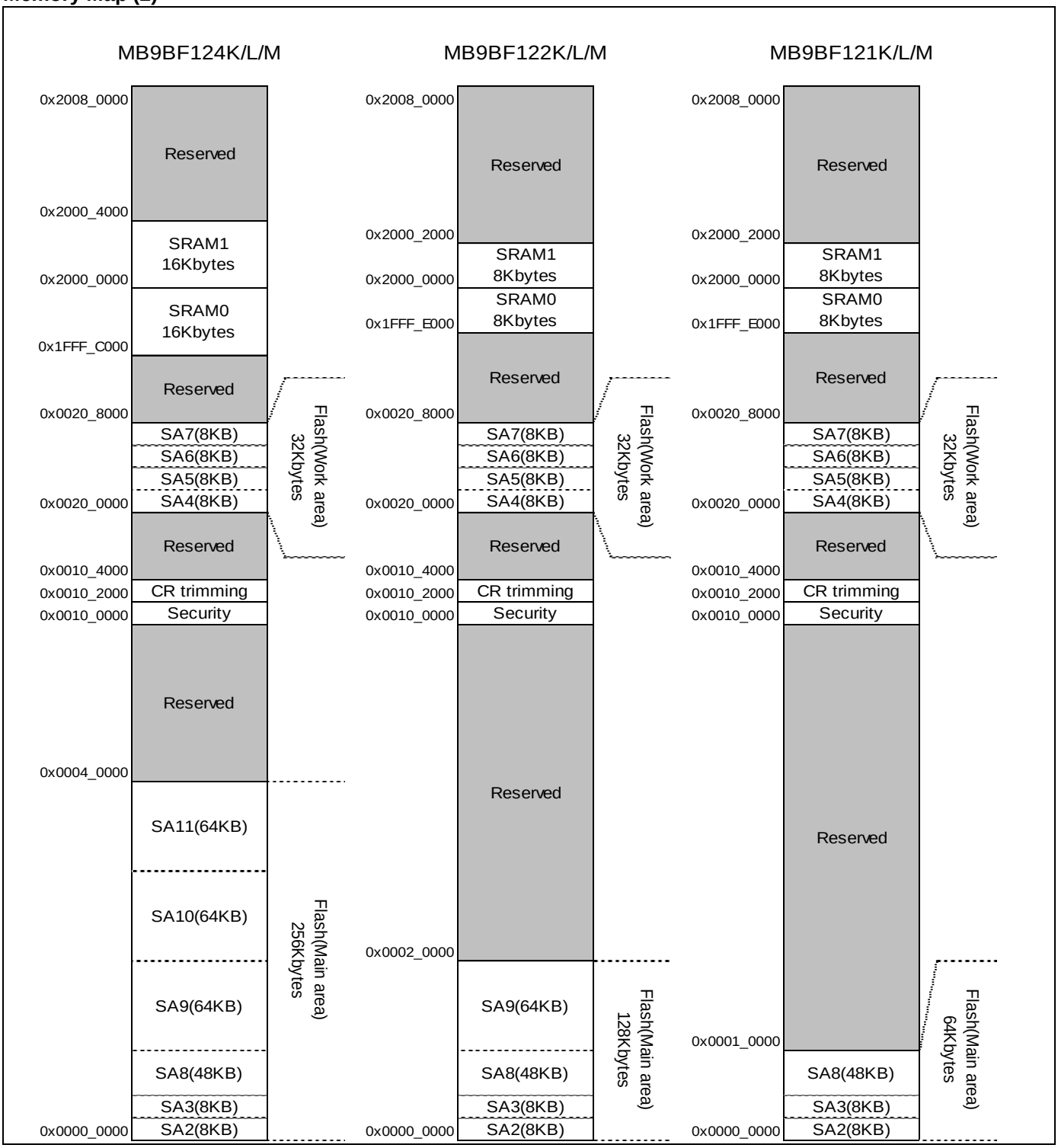
See "Memory Size" in "Product Lineup" to confirm the memory size.

10. Memory Map

Memory Map (1)



Memory Map (2)



Refer to the programming manual for the detail of Flash main area.

■MB9AB40N/A40N/340N/140N/150R,MB9B520M/320M/120M Series Flash Programming Manual

List of Pin Status

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Main crystal oscillator input pin/ External main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state
	Main crystal oscillator output pin	Hi-Z / Internal input fixed at "0"/ or Input enable	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state/ When oscillation stops*1, Hi-Z / Internal input fixed at "0"	Maintain previous state/ When oscillation stops*1, Hi-Z / Internal input fixed at "0"	Maintain previous state/ When oscillation stops*1, Hi-Z / Internal input fixed at "0"	Maintain previous state/ When oscillation stops*1, Hi-Z / Internal input fixed at "0"	Maintain previous state/ When oscillation stops*1, Hi-Z / Internal input fixed at "0"	Maintain previous state/ When oscillation stops*1, Hi-Z / Internal input fixed at "0"
C	INITX input pin	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Input enabled	GPIO selected	Hi-Z / Input enabled	GPIO selected
F	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Sub crystal oscillator input pin / External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
G	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	External sub clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at "0"/ or Input enable	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state	Maintain previous state/ When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state/ When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state/ When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state/ When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state/ When oscillation stops*2, Hi-Z / Internal input fixed at "0"
H	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage *1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage *1, *3	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage *1, *3	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage *1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5V tolerant
Analog pin input voltage *1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5V)	V	
Output voltage *1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5V)	V	
Clamp maximum current	I_{CLAMP}	-2	+2	mA	*7
Clamp total maximum current	$\sum [I_{CLAMP}]$		+20	mA	*7
"L" level maximum output current *4	I_{OL}	-	10	mA	4mA type
			20	mA	12mA type
			39	mA	P80/P81 pin
"L" level average output current *5	I_{OLAV}	-	4	mA	4mA type
			12	mA	12mA type
			16.5	mA	P80/P81 pin
"L" level total maximum output current	$\sum I_{OL}$	-	100	mA	
"L" level total maximum output current *8	$\sum I_{OLAV}$	-	50	mA	
"H" level maximum output current *6	I_{OH}	-	- 10	mA	4mA type
			- 20	mA	12mA type
			- 39	mA	P80/P81 pin
"H" level average output current *7	I_{OHAV}	-	- 4	mA	4mA type
			- 12	mA	12mA type
			- 18	mA	P80/P81 pin
"H" level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
"H" level total average output current *8	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	300	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0$ V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: Ensure that the voltage does not exceed V_{CC} + 0.5 V, for example, when the power is turned on.

*4: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*5: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100 ms period.

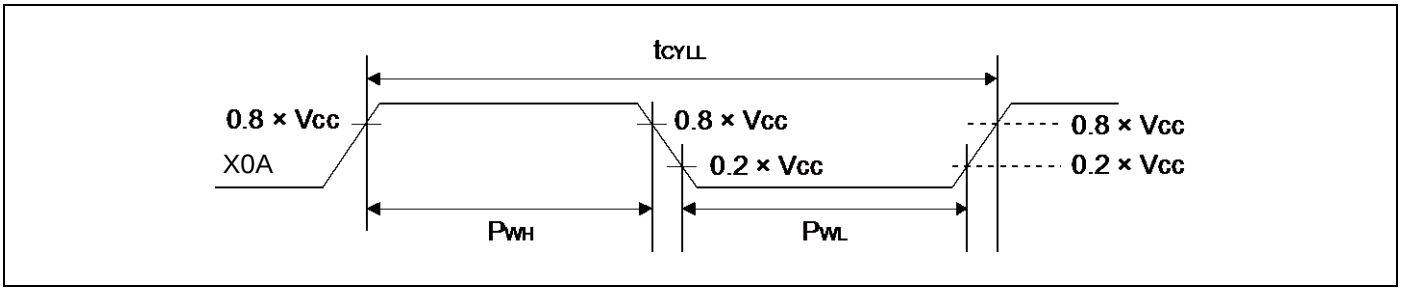
*6: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100 ms period.

12.4.2 Sub Clock Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	1/ t_{CYLL}	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		PWH/tCYLL, PWL/tCYLL	45	-	55	%	When using external clock

*: See "Sub crystal oscillator" in "Handling Devices" for the crystal oscillator used.



12.4.3 Built-in CR Oscillation Characteristics

Built-in High-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRH}	T_A = + 25°C	3.92	4	4.08	MHz	When trimming*1
		T_A = 0°C to + 85°C	3.9	4	4.1		
		T_A = -40°C to + 105°C	3.88	4	4.12		
		T_A = + 25°C $V_{CC} \leq$ 3.6 V	3.94	4	4.06		
		T_A = - 20°C to + 85°C $V_{CC} \leq$ 3.6 V	3.92	4	4.08		
		T_A = - 20°C to + 105°C $V_{CC} \leq$ 3.6 V	3.9	4	4.1		
		T_A = - 40°C to + 105°C	2.8	4	5.2		When not trimming
Frequency stabilization time	t_{CRWT}	-	-	-	30	µs	*2

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency/temperature trimming.

*2: This is the time to stabilize the frequency of high-speed CR clock after setting trimming value.
This period is able to use high-speed CR clock as source clock.

Built-in Low-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	

12.4.4 Operating Conditions of Main PLL (In the case of using main clock for input of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	5	-	37	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	75	-	150	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	72	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see "Chapter: Clock" in "FM3 Family Peripheral Manual".

12.4.5 Operating Conditions of Main PLL (In the case of using built-in high-speed CR for input clock of Main PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

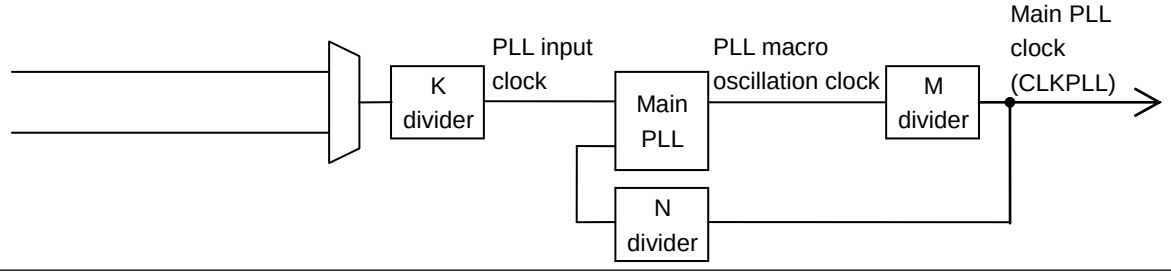
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	3.8	4	4.2	MHz	
PLL multiplication rate	-	19	-	35	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	72	-	150	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	72	MHz	

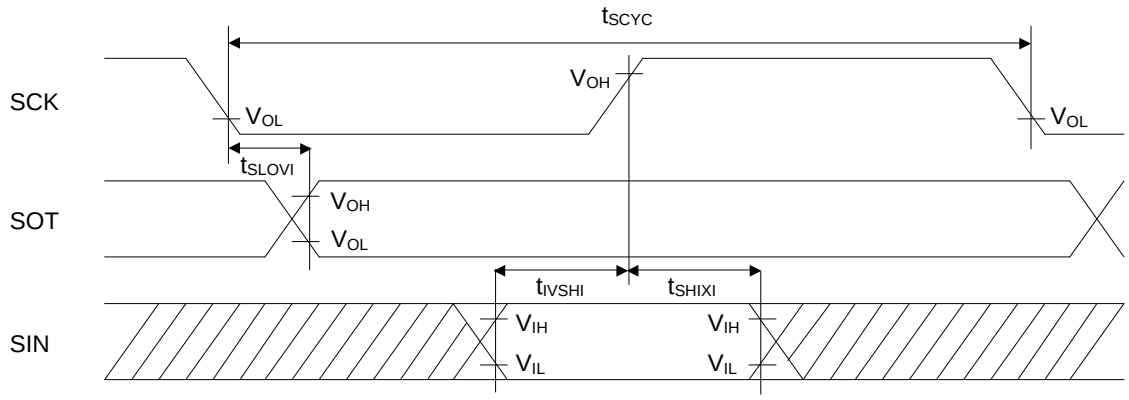
*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see "Chapter 2-1: Clock" in "FM3 Family Peripheral Manual".

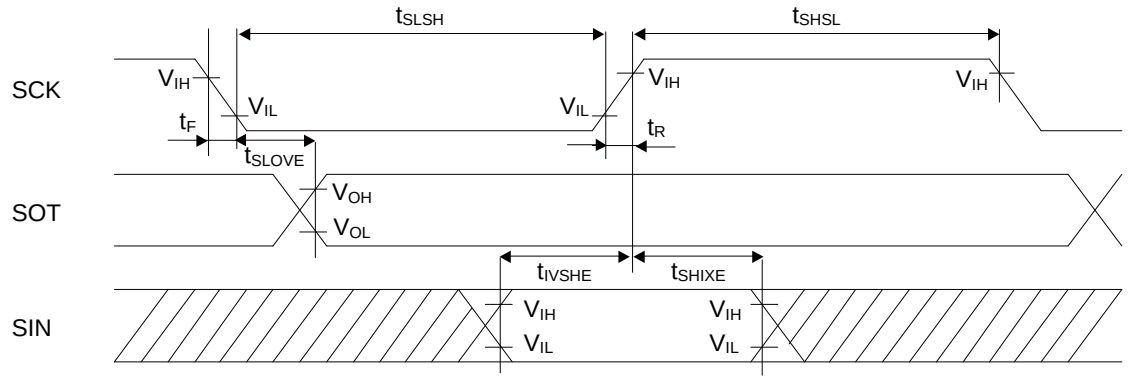
Note: Make sure to input to the Main PLL source clock, the high-speed CR clock (CLKHC) that the frequency/temperature has been trimmed.
When setting PLL multiple rate, please take the accuracy of the built-in high-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.

Main PLL connection

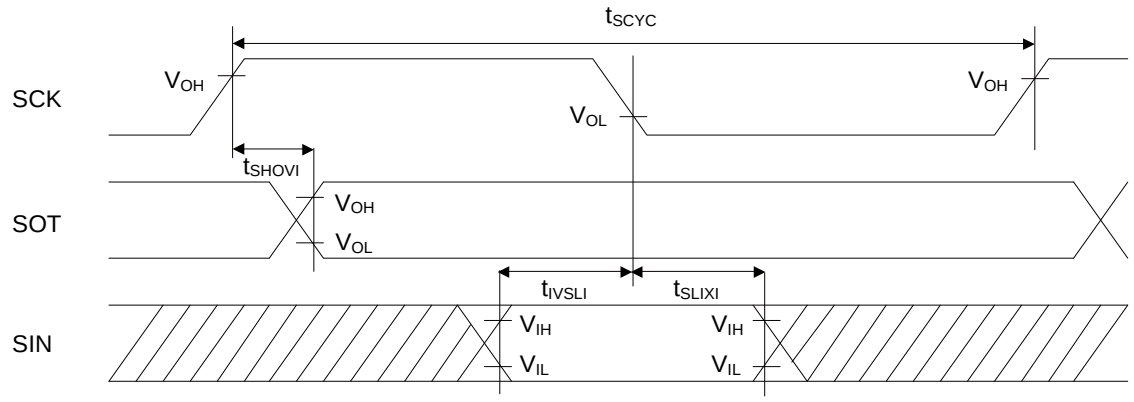




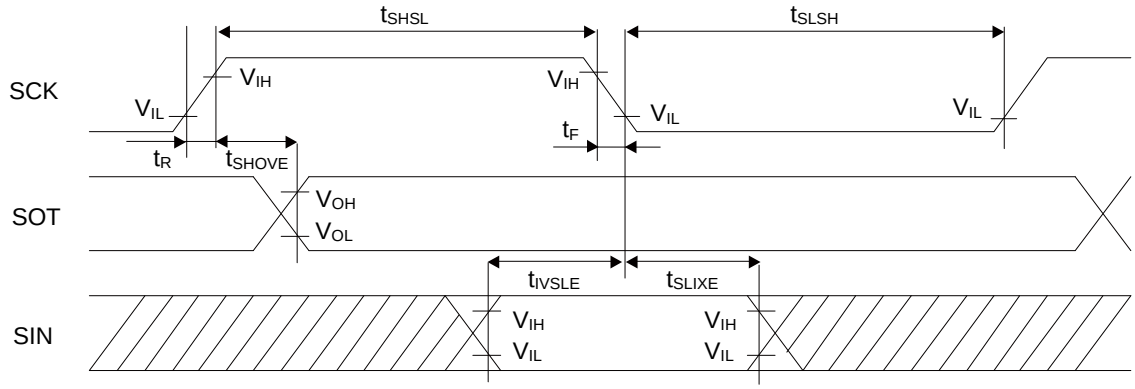
Master mode



Slave mode



Master mode



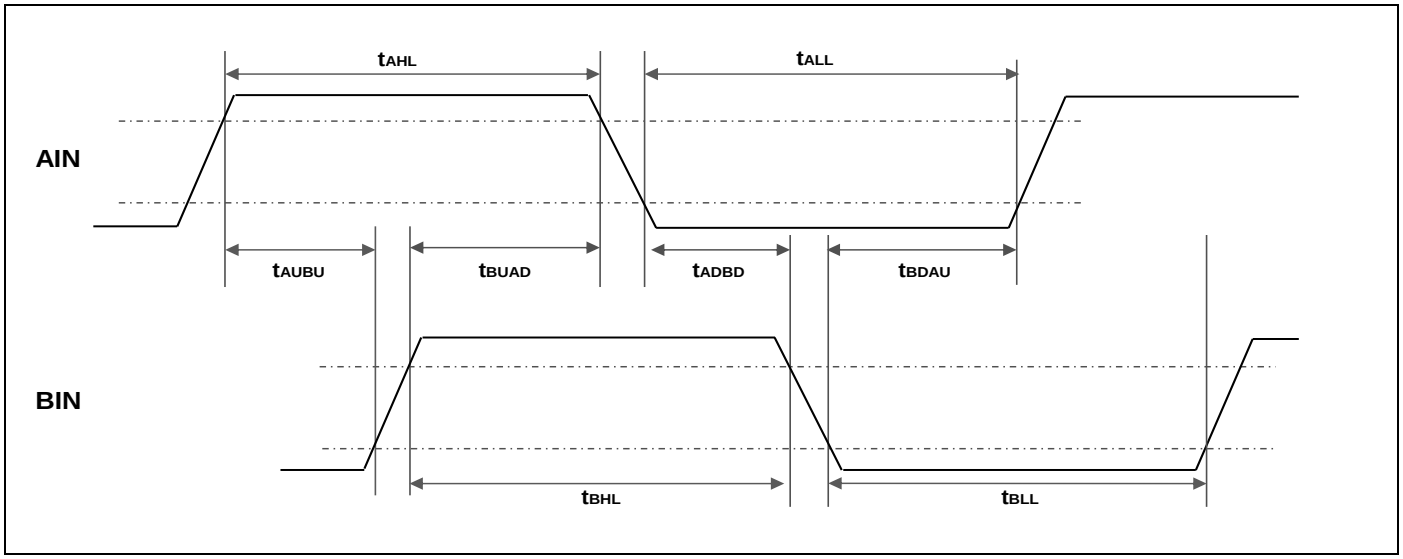
Slave mode

12.4.11 Quadrature Position/Revolution Counter timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin H width	t_{AHL}	-	$2t_{CYCP}$*	-	ns
AIN pin L width	t_{ALL}	-			
BIN pin H width	t_{BHL}	-			
BIN pin L width	t_{BLL}	-			
BIN rising time from AIN pin H level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin H level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin L level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin L level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin H level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin H level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin L level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rising time from AIN pin L level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin H width	t_{ZHL}	QCR:CGSC=0			
ZIN pin L width	t_{ZLL}	QCR:CGSC=0			
AIN/BIN rise and falling time from determined ZIN level	t_{ZABE}	QCR:CGSC=1			
Determined ZIN level from AIN/BIN rise and falling time	t_{ABEZ}	QCR:CGSC=1			

*: t_{CYCP} indicates the APB bus clock cycle time.
About the APB bus number which the Quadrature Position/Revolution Counter is connected to, see "Block Diagram" in this data sheet.



12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-	± 1.5	± 4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential Nonlinearity	-	-	-	± 1.7	± 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	-	± 10	± 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	-	AVRH ± 5	AVRH ± 15	mV	
Conversion time	-	-	0.8*1	-	-	µs	AV_{CC} ≥ 4.5 V
			1.0*1	-	-		AV_{CC} < 4.5 V
Sampling time*2	t_S	-	0.24	-	10	µs	AV_{CC} ≥ 4.5 V
			0.3	-			AV_{CC} < 4.5 V
Compare clock cycle*3	t_{CCK}	-	40	-	1000	ns	AV_{CC} ≥ 4.5 V
			50	-			AV_{CC} < 4.5 V
State transition time to operation permission	t_{STT}	-	-	-	1.0	µs	
Analog input capacity	C_{AIN}	-	-	-	9.7	pF	
Analog input resistor	R_{AIN}	-	-	-	1.7	kΩ	AV_{CC} ≥ 4.5 V
					2.4		AV_{CC} < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AVRL	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	AV_{CC}	V	
	-	AVRL	AV_{SS}	-	AV_{SS}	V	

*1: The conversion time is the value of sampling time (t_S) + compare time (t_C).

The condition of the minimum conversion time is the following.

AV_{CC} ≥ 4.5 V, HCLK=50 MHz sampling time: 240 ns, compare time: 560 ns.

AV_{CC} < 4.5 V, HCLK=40 MHz sampling time: 300 ns, compare time: 700 ns

Ensure that it satisfies the value of the sampling time (t_S) and compare clock cycle (t_{CCK}).

For setting of the sampling time and compare clock cycle, see "Chapter 1-1: A/D Converter" in "FM3 Family Peripheral Manual Analog Macro Part".

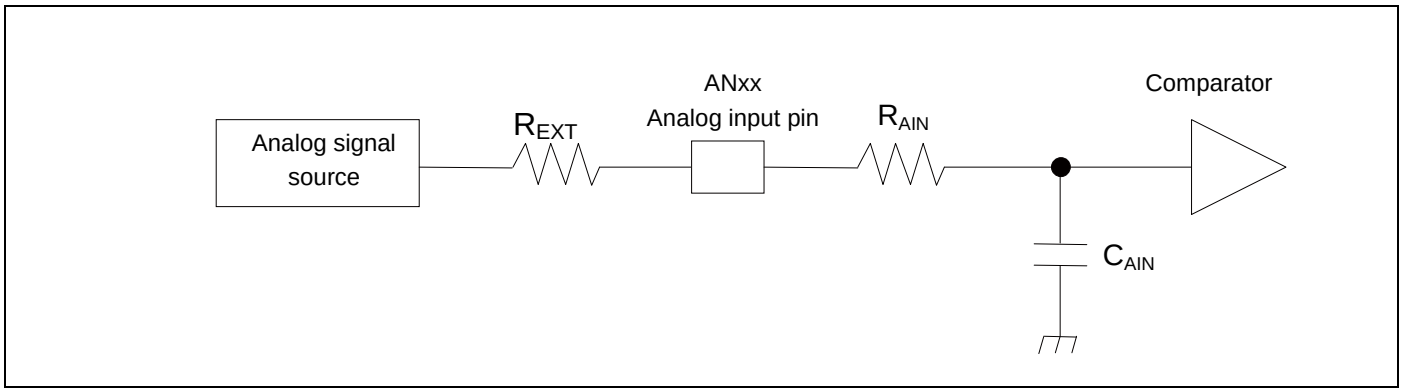
The register settings of the A/D Converter are reflected in the operation according to the APB bus clock timing.

For the number of the APB bus to which the A/D Converter is connected, see "Block Diagram".

The base clock (HCLK) is used to generate the sampling time and the compare clock cycle.

*2: A necessary sampling time changes by external impedance.
Ensure that it sets the sampling time to satisfy (Equation 1).

*3: The compare time (t_C) is the value of (Equation 2).



(Equation 1) $t_S \geq (R_{AIN} + R_{EXT}) \times C_{AIN} \times 9$

t_S: Sampling time

R_{AIN} : input resistor of A/D = 1.5 kΩ at 4.5 V ≤ AV_{CC} ≤ 5.5 V ch.0 to ch.7
input resistor of A/D = 1.6 kΩ at 4.5 V ≤ AV_{CC} ≤ 5.5 V ch.8 to ch.15
input resistor of A/D = 1.7 kΩ at 4.5 V ≤ AV_{CC} ≤ 5.5 V ch.16 to ch.26
input resistor of A/D = 2.2 kΩ at 2.7 V ≤ AV_{CC} < 4.5 V ch.0 to ch.7
input resistor of A/D = 2.3 kΩ at 2.7 V ≤ AV_{CC} < 4.5 V ch.8 to ch.15
input resistor of A/D = 2.4 kΩ at 2.7 V ≤ AV_{CC} < 4.5 V ch.16 to ch.26

C_{AIN}: input capacity of A/D = 9.7 pF at 2.7 V ≤ AV_{CC} ≤ 5.5 V

R_{EXT}: Output impedance of external circuit

(Equation 2) $t_C = t_{CCK} \times 14$

t_C: Compare time

t_{CCK}: Compare clock cycle

12.9.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

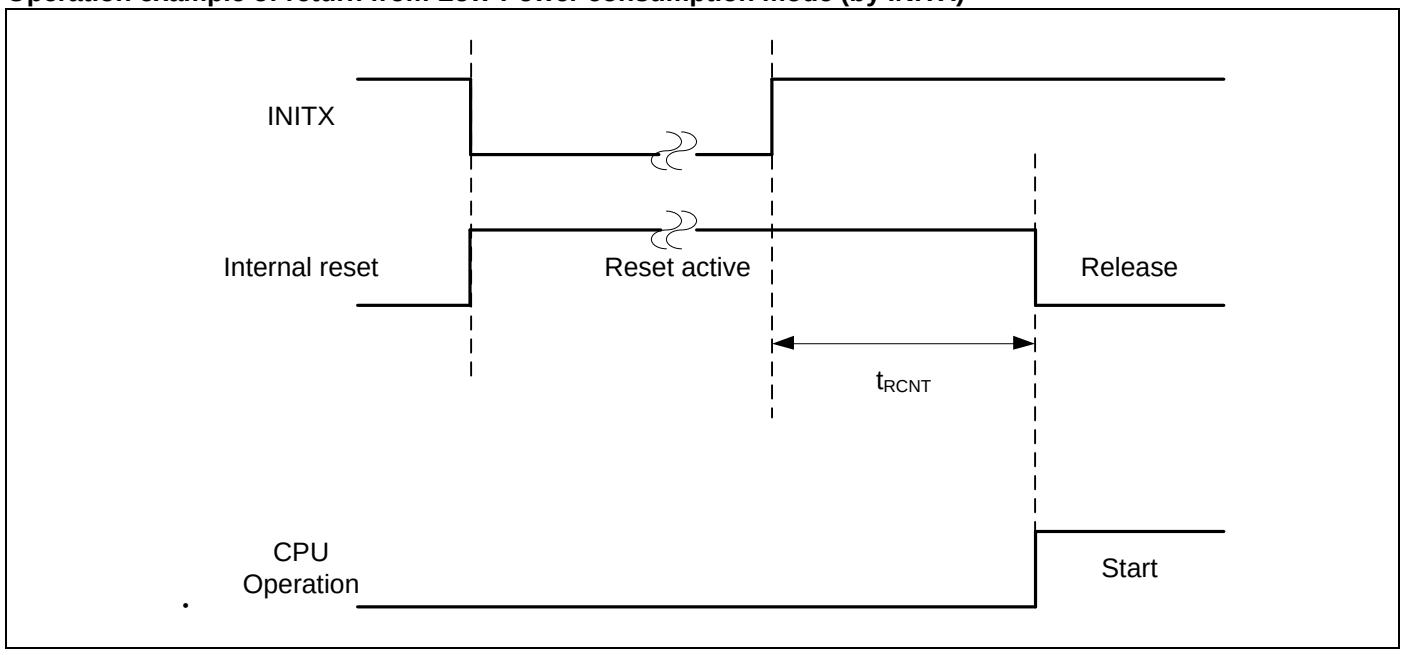
Return Count Time

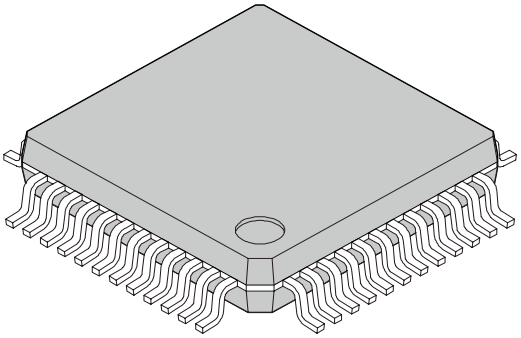
(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{RCNT}	148	263	µs	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		148	263	µs	
Low-speed CR Timer mode		248	463	µs	
Sub Timer mode		312	496	µs	
RTC mode, Stop mode		268	503	µs	
Deep Standby RTC mode		308	583	µs	When RAM is off
Deep Standby Stop mode		268	503	µs	When RAM is on

*: The maximum value depends on the accuracy of built-in CR.

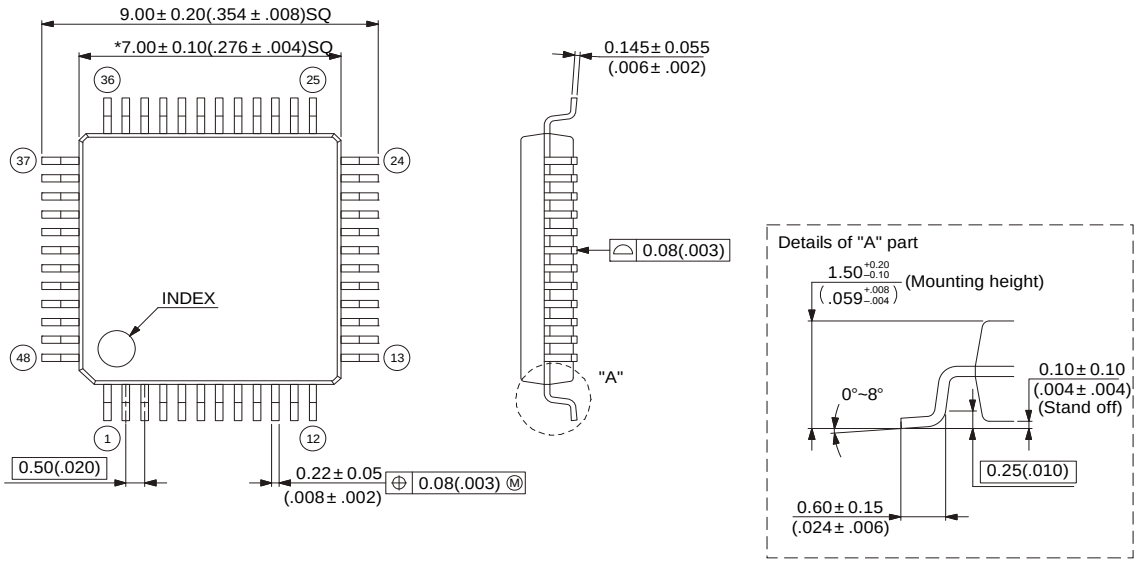
Operation example of return from Low-Power consumption mode (by INITX)



48-pin plastic LQFP		
 (FPT-48P-M49)	Lead pitch	0.50 mm
	Package width × package length	7.00 mm × 7.00 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.17 g

48-pin plastic LQFP
(FPT-48P-M49)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.