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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CSIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 23x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/rochester-electronics/mb9bf124lqn-g-ave2

Contents

1. Product Lineup

Memory Size

Product Name		MB9BF121K/L/M	MB9BF122K/L/M	MB9BF124K/L/M
On-chip Flash memory	Main area	64 Kbytes	128 Kbytes	256 Kbytes
	Work area	32 Kbytes	32 Kbytes	32 Kbytes
On-chip SRAM	SRAM0	8 Kbytes	8 Kbytes	16 Kbytes
	SRAM1	8 Kbytes	8 Kbytes	16 Kbytes
	Total	16 Kbytes	16 Kbytes	32 Kbytes

Function

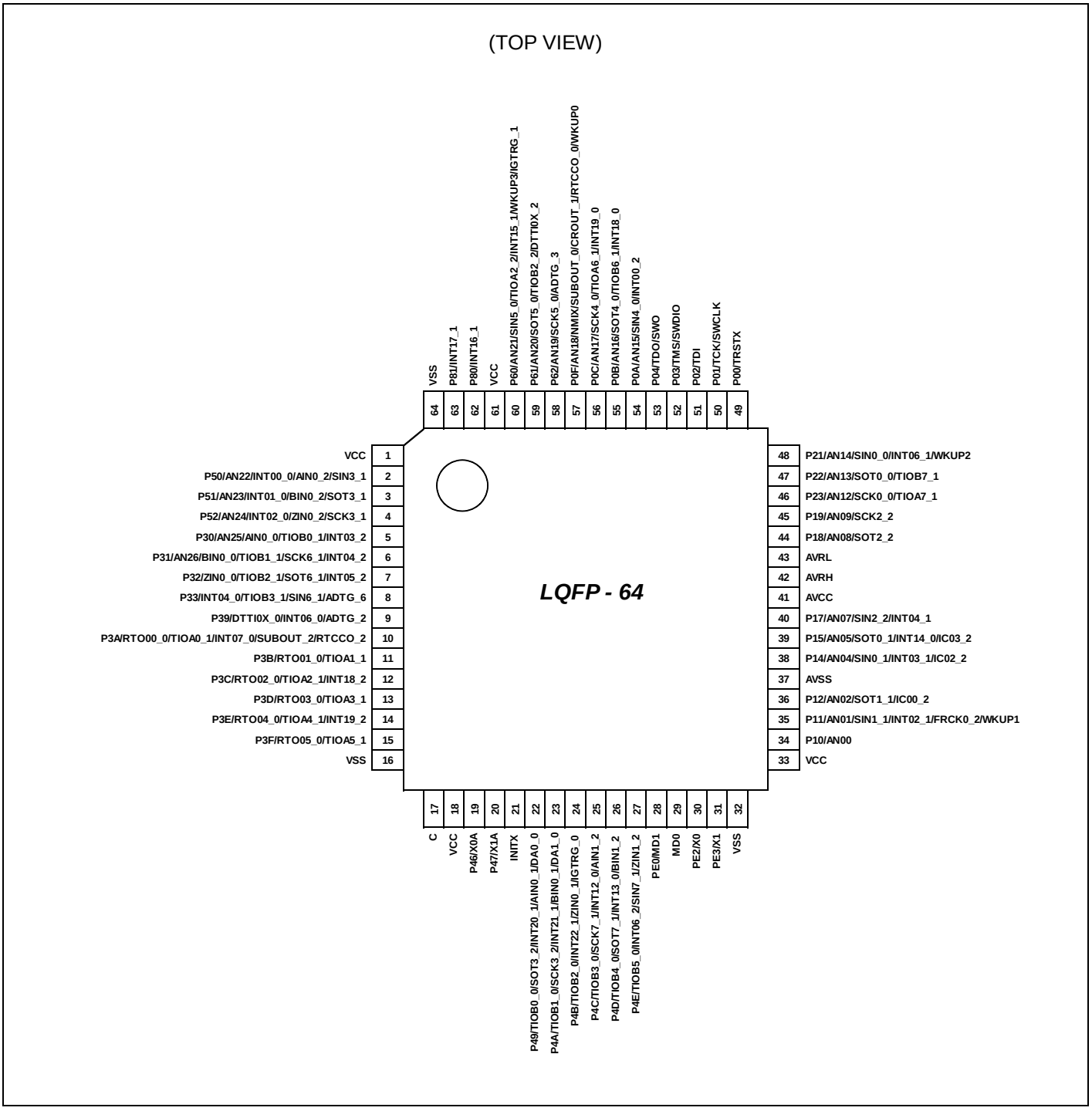
Product Name			MB9BF121K MB9BF122K MB9BF124K	MB9BF121L MB9BF122L MB9BF124L	MB9BF121M MB9BF122M MB9BF124M
Pin count			48	64	80/96
CPU			Cortex-M3		
		Freq.	72 MHz		
Power supply voltage range			2.7 V to 5.5 V		
DMAC			8ch.		
Multi-function Serial Interface (UART/CSIO/LIN/I^{2}C)			4ch. (Max) ch.0/1/3: FIFO ch.5: No FIFO (In ch.1/5, only UART and LIN are available.)	8ch. (Max) ch.0/1/3/4 FIFO ch.2/5/6/7: No FIFO (In ch.1, only UART and LIN are available.)	
Base Timer (PWC/Reload timer/PWM/PPG)			8ch. (Max)		
MF Timer	A/D activation compare	2ch.	1 unit		
	Input capture	4ch.*			
	Free-run timer	3ch.			
	Output compare	6ch.			
	Waveform generator	3ch.			
	PPG	3ch.			
QPRC			1ch.	2ch. (Max)	
Dual Timer			1 unit		
Real-Time Clock			1 unit		
Watch Counter			1 unit		
CRC Accelerator			Yes		
Watchdog Timer			1ch. (SW) + 1ch. (HW)		
External Interrupts			14 pins (Max) + NMI × 1	19 pins (Max) + NMI x 1	23 pins (Max) + NMI x 1
I/O ports			35 pins (Max)	50 pins (Max)	60 pins (Max)
12-bit A/D converter			14ch. (2 units)	23ch. (2 units)	26ch. (2 units)
CSV (Clock Super Visor)			Yes		
LVD (Low-Voltage Detector)			2ch.		
Built-in CR		High-speed	4 MHz		
		Low-speed	100 kHz		
Debug Function			SWJ-DP		
Unique ID			Yes		

*: The external input channel which can be used is shown as follows.

- ch.0 to ch.3 : MB9BF121M/F122M/F124M
- ch.0, ch.2, ch.3 : MB9BF121K/F122K/F124K, MB9BF121L/F122L/F124L

Note: All signals of the peripheral function in each product cannot be allocated by limiting the pins of package.
It is necessary to use the port relocate function of the I/O port according to your function use.
See “12 Electrical Characteristics 12.4 AC Characteristics 12.4.3 Built-in CR Oscillation Characteristics” for the accuracy of the built-in CR.

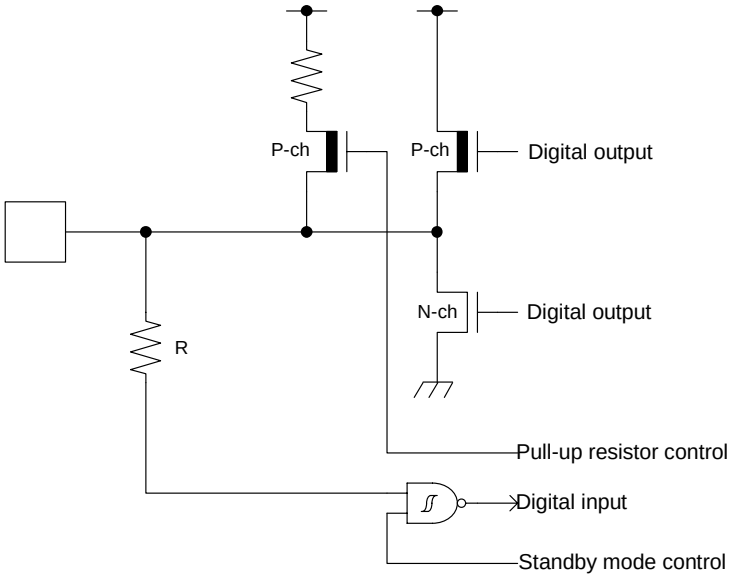
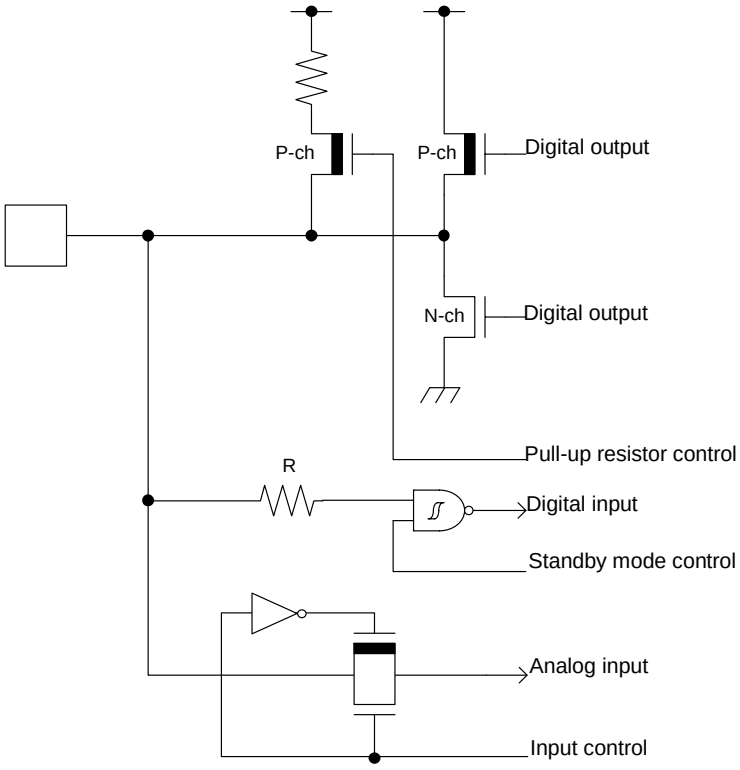
FPT-64P-M38/M39

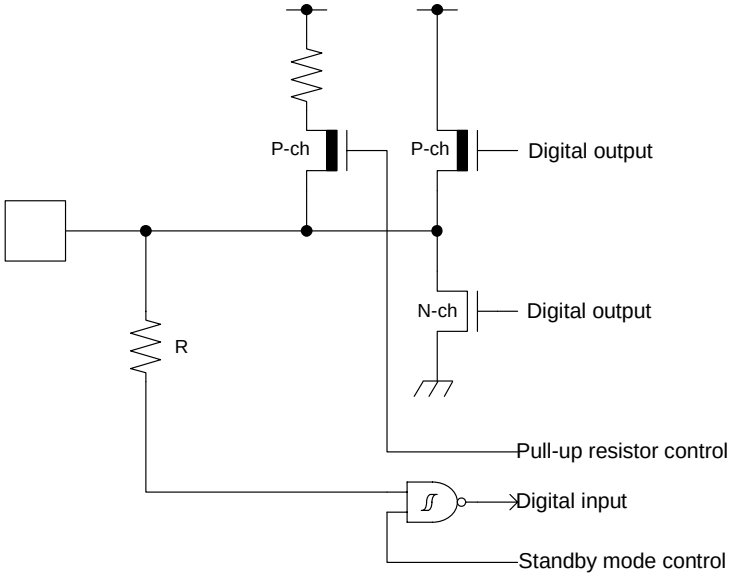
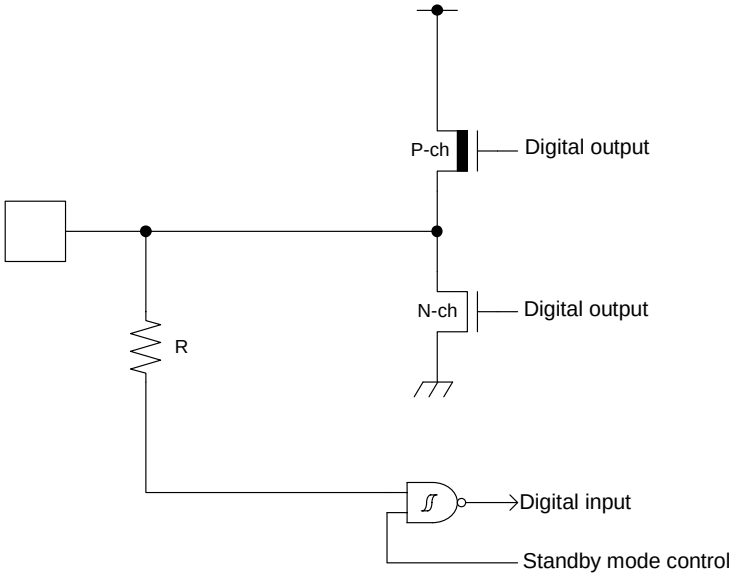


Note:

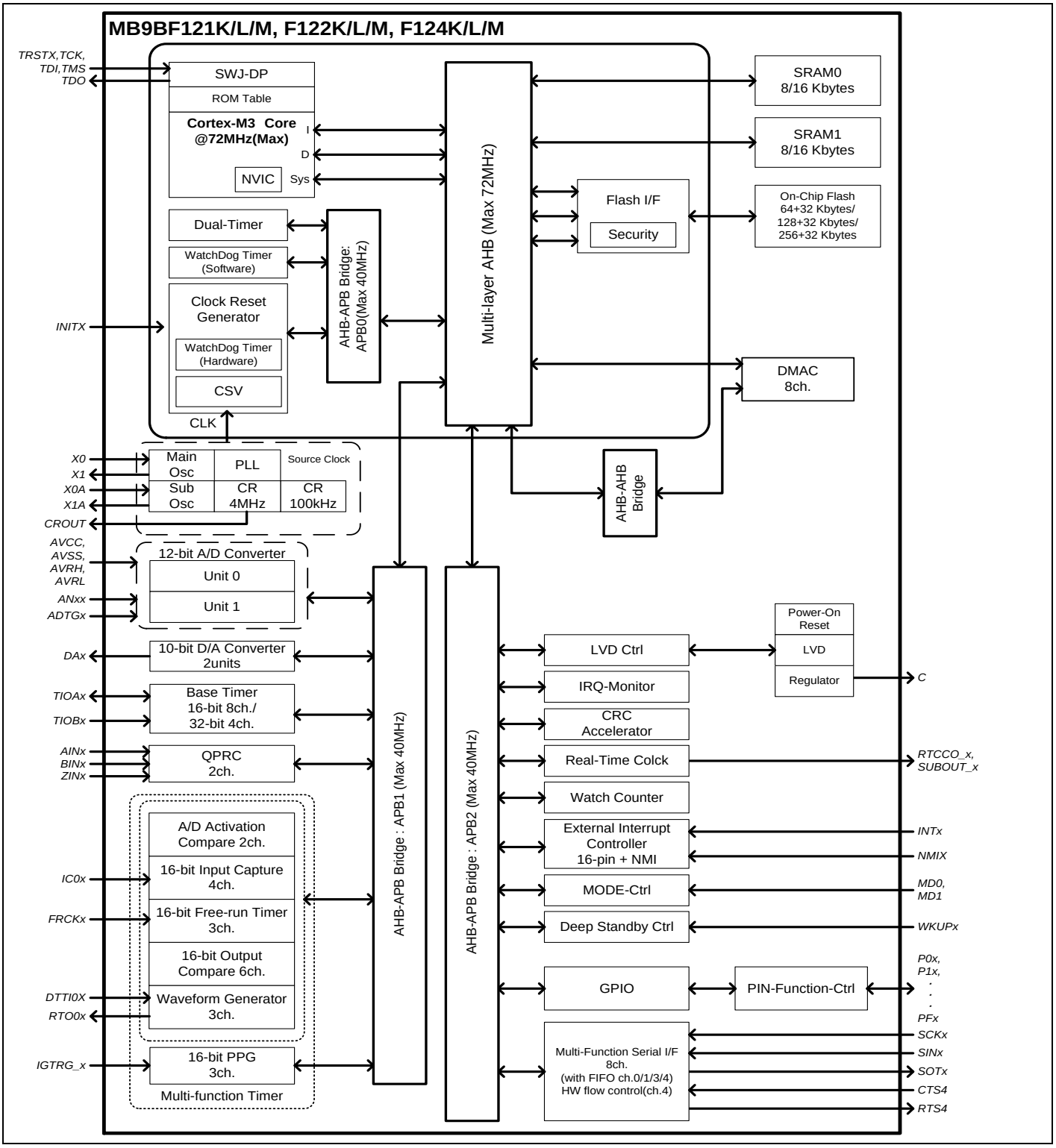
The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
55	E10	-	-	P1A AN10 SIN4_1 INT05_1 IC00_1	F	N
56	E9	-	-	P1B AN11 SOT4_1 (SDA4_1) IC01_1 INT20_2	F	N
57	D10	46	34	P23 SCK0_0 (SCL0_0) TIOA7_1 AN12	F	M
58	D9	47	35	P22 SOT0_0 (SDA0_0) TIOB7_1 AN13	F	M
		-	-	ZIN1_1		
59	C11	48	36	P21 SIN0_0 INT06_1 WKUP2 BIN1_1 AN14	F	N
60	C10	-	-	P20 INT05_0 CROUT_0 AIN1_1	E	N
61	A10	49	37	P00 TRSTX	E	J
62	B9	50	38	P01 TCK SWCLK	E	J
63	B11	51	39	P02 TDI	E	J
64	A9	52	40	P03 TMS SWDIO	E	J
65	B8	53	41	P04 TDO SWO	E	J
66	A8	-	-	P07 ADTG_0 INT23_1	E	L
67	C8	54	-	P0A SIN4_0 INT00_2 AN15	J*	N

Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available
F		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available

Type	Circuit	Remarks
G		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -12 mA, I_{OL}= 12 mA • +B input is available
H		• CMOS level output • CMOS level hysteresis input • With standby mode control • I_{OH} = -18 mA, I_{OL} = 16.5 mA

8. Block Diagram



11. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

■INITX=0
This is the period when the INITX pin is the "L" level.

■INITX=1
This is the period when the INITX pin is the "H" level.

■SPL=0
This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to "0".

■SPL=1
This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to "1".

■Input enabled
Indicates that the input function can be used.

■Internal input fixed at "0"
This is the status that the input function cannot be used. Internal input is fixed at "L".

■Hi-Z
Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

■Setting disabled
Indicates that the setting is disabled.

■Maintain previous state
Maintains the state that was immediately prior to entering the current mode.
If a built-in peripheral function is operating, the output follows the peripheral function.
If the pin is being used as a port, that output is maintained.

■Analog input is enabled
Indicates that the analog input is enabled.

■Trace output
Indicates that the trace function can be used.

■GPIO selected
In Deep standby mode, pins switch to the general-purpose I/O port.

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
I	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input disabled	Hi-Z / Internal input fixed at "0" / Analog input disabled	Hi-Z / Internal input fixed at "0" / Analog input disabled
	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected									Maintain previous state
J	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
K	Resource selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected									
L	Analog output selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	*3	*4	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	External interrupt enabled selected					Maintain previous state	Maintain previous state			
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected									

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
M	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected									
N	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Resource other than above selected						Hi-Z / Internal input fixed at "0"			
	GPIO selected									

*1: Oscillation is stopped at Sub Timer mode, Low-speed CR Timer mode, RTC mode, Stop mode, Deep Standby RTC mode, and Deep Standby Stop mode.

*2: Oscillation is stopped at Stop mode and Deep Standby Stop mode.

*3: Maintain previous state at Timer mode. GPIO selected Internal input fixed at "0" at RTC mode, Stop mode.

*4: Maintain previous state at Timer mode. Hi-Z/Internal input fixed at "0" at RTC mode, Stop mode.

Low-Voltage Detection Current

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation for reset Vcc = 5.5 V	0.13	0.3	µA	At not detect
			At operation for interrupt Vcc = 5.5 V	0.13	0.3	µA	At not detect

Flash Memory Current

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$	VCC	At Write/Erase	9.5	11.2	mA	*

*: The current at which to write or erase Flash memory, "$I_{CCFLASH}$" is added to "I_{CC}".

A/D Converter Current

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At 1unit operation	0.69	0.90	mA	
			At stop	0.25	25.84	µA	
Reference power supply current	I_{CCAVRH}	AVRH	At 1unit operation AVRH=5.5 V	1.1	1.97	mA	
			At stop	0.2	3.4	µA	

D/A Converter Current

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*1	IDDA*2	AVCC	At 1unit operation AV_{CC}=3.3 V	250	315	380	µA	
			At 1unit operation AV_{CC}=5.0 V	380	475	580	µA	
	IDSA		At stop	-	-	16	µA	

*1: No-load

*2: Generates the max current by the CODE about 0x200

12.4 AC Characteristics

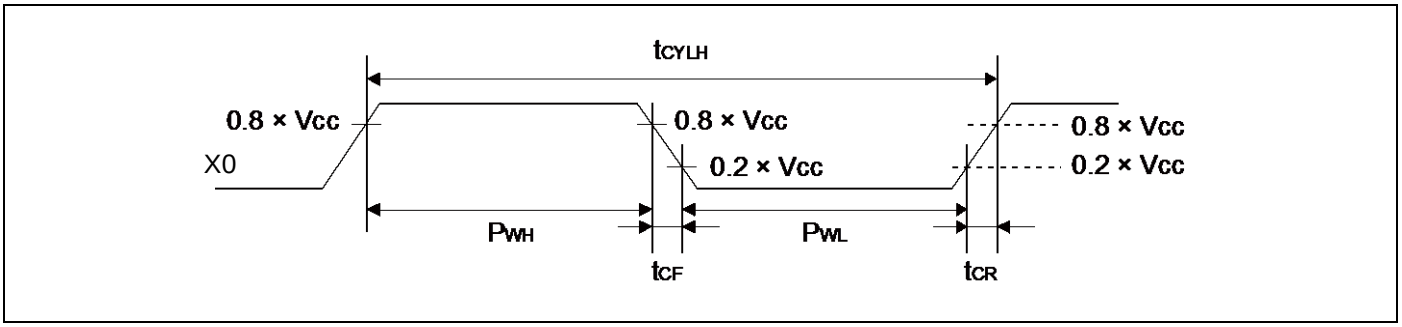
12.4.1 Main Clock Input Characteristics

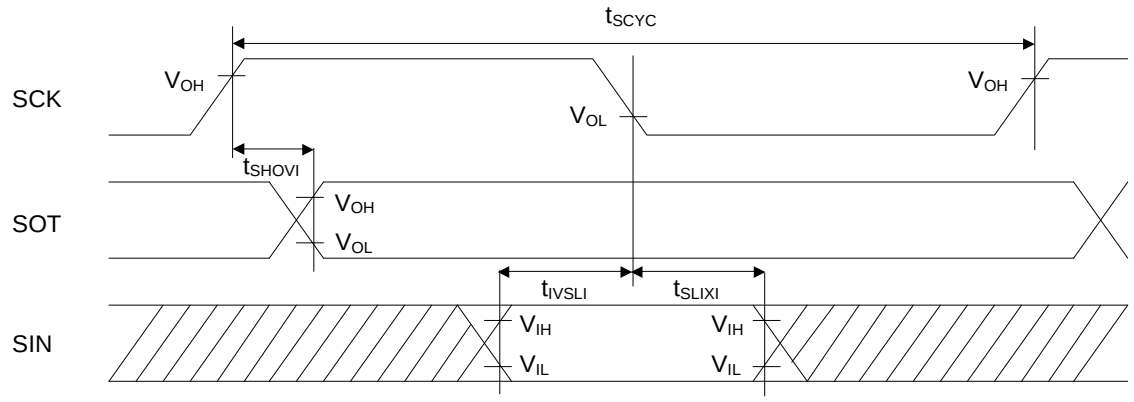
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0, X1	$V_{CC} \geq 4.5$ V	4	48	MHz	When crystal oscillator is connected
			$V_{CC} < 4.5$ V	4	20		
			$V_{CC} \geq 4.5$ V	4	48	MHz	When using external clock
			$V_{CC} < 4.5$ V	4	20		
Input clock cycle	t_{CYLH}		$V_{CC} \geq 4.5$ V	20.83	250	ns	When using external clock
			$V_{CC} < 4.5$ V	50	250		
Input clock pulse width	-		PWH/tCYLH, PWL/tCYLH	45	55	%	When using external clock
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When using external clock
Internal operating clock frequency*1	f_{CM}	-	-	-	72	MHz	Master clock
	f_{CC}	-	-	-	72	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	40	MHz	APB0 bus clock*2
	f_{CP1}	-	-	-	40	MHz	APB1 bus clock*2
	f_{CP2}	-	-	-	40	MHz	APB2 bus clock*2
Internal operating clock cycle time*1	t_{CYCC}	-	-	13.8	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	25	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	25	-	ns	APB1 bus clock*2
	t_{CYCP2}	-	-	25	-	ns	APB2 bus clock*2

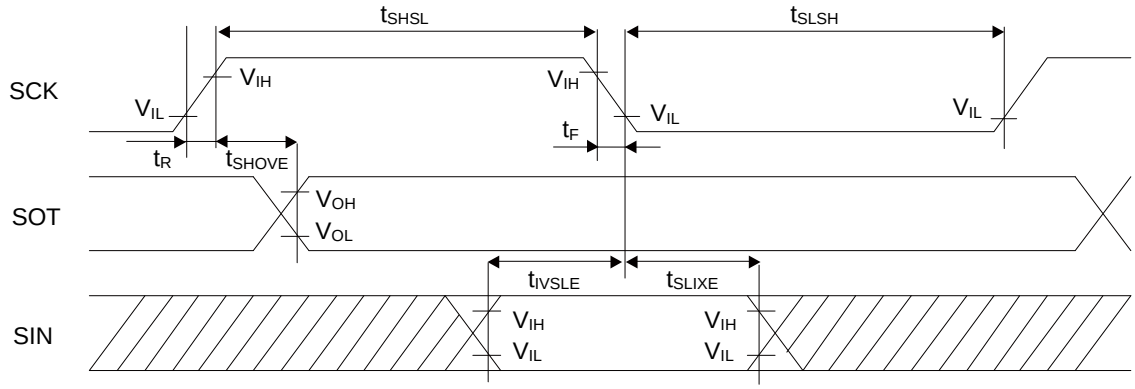
*1: For more information about each internal operating clock, see "Chapter 2-1:Clock" in "FM3 Family Peripheral Manual".

*2: For about each APB bus which each peripheral is connected to, see "Block Diagram" in this data sheet.





Master mode



Slave mode

CSIO (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK ↓→ SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓→ SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function serial is connected to, see "Block Diagram" in this data sheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 30 pF.

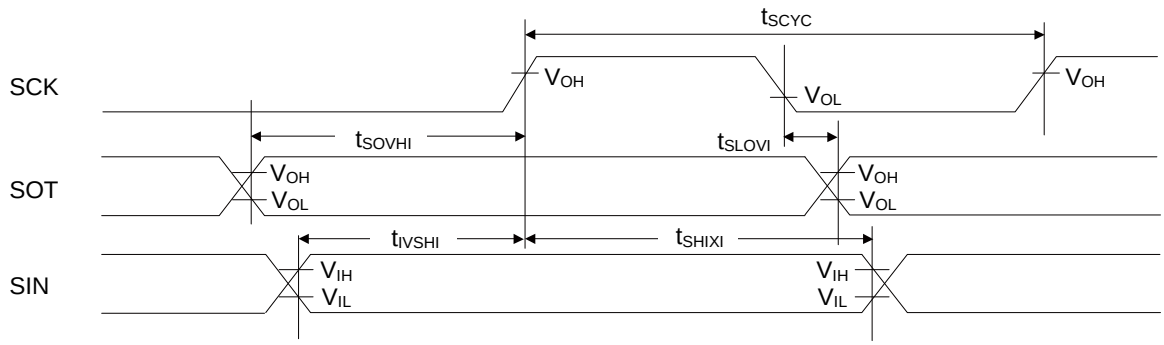
CSIO (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

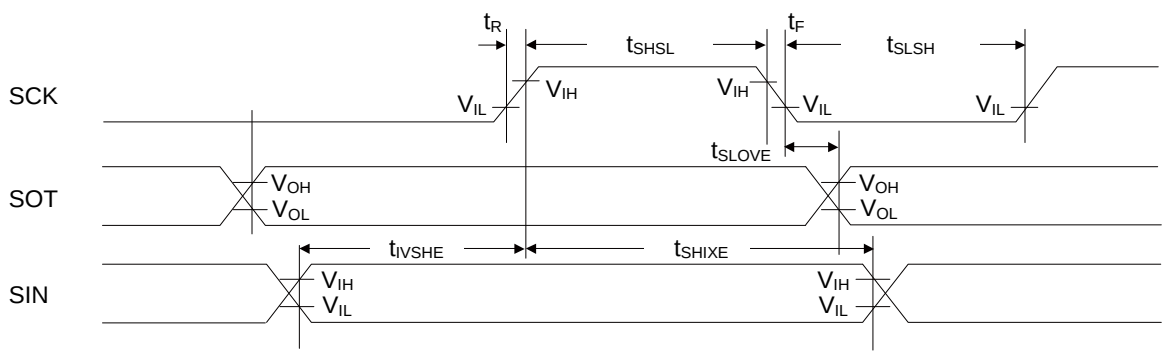
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function serial is connected to, see "Block Diagram" in this data sheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 30 pF.



Master mode

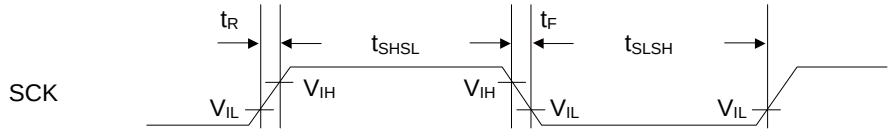


Slave mode

UART external clock input (EXT = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Min	Max	Unit	Remarks
Serial clock L pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock H pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK falling time	t_F		-	5	ns	
SCK rising time	t_R		-	5	ns	



12.4.12 I^2C Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

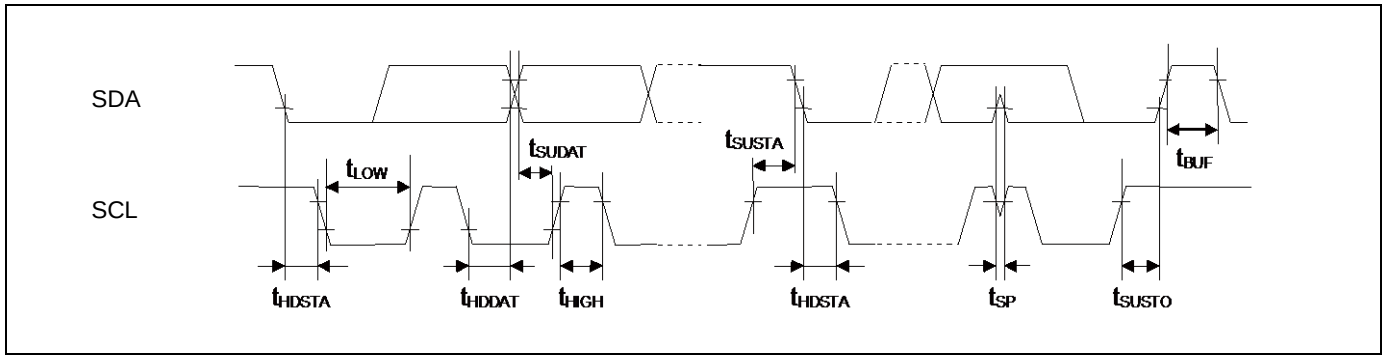
Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, $R = (V_P/I_{OL})$*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock L width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock H width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between STOP condition and START condition	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	-	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	

*1: R and C_L represent the pull-up resistor and load capacitance of the SCL and SDA lines, respectively.
V_P indicates the power supply voltage of the pull-up resistor and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy that it does not extend at least L period (t_{LOW}) of device's SCL signal.

*3: A Fast-speed mode I^2C bus device can be used on a Standard mode I^2C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CYCP} is the APB bus clock cycle time.
About the APB bus number that I^2C is connected to, see "Block Diagram" in this data sheet.
To use Standard-mode, set the APB bus clock at 2 MHz or more
To use Fast-mode, set the APB bus clock at 8 MHz or more.



12.8 Flash Memory Write/Erase Characteristics

12.8.1 Write / Erase time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 105°C)

Parameter		Value		Unit	Remarks
		Typ	Max		
Sector erase time	Large Sector	1.1	2.7	s	Includes write time prior to internal erase
	Small Sector	0.3	0.9		
Half word (16-bit) write time		16	310	µs	Not including system-level overhead time
Chip erase time		6.8	18	s	Includes write time prior to internal erase

*: The typical value is immediately after shipment, the maximum value is guarantee value under 10,000 cycle of erase/write.

12.8.2 Write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20*	
10,000	10*	

*: At average + 85°C

12.9 Return Time from Low-Power Consumption Mode

12.9.1 Return Factor: Interrupt/WKUP

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

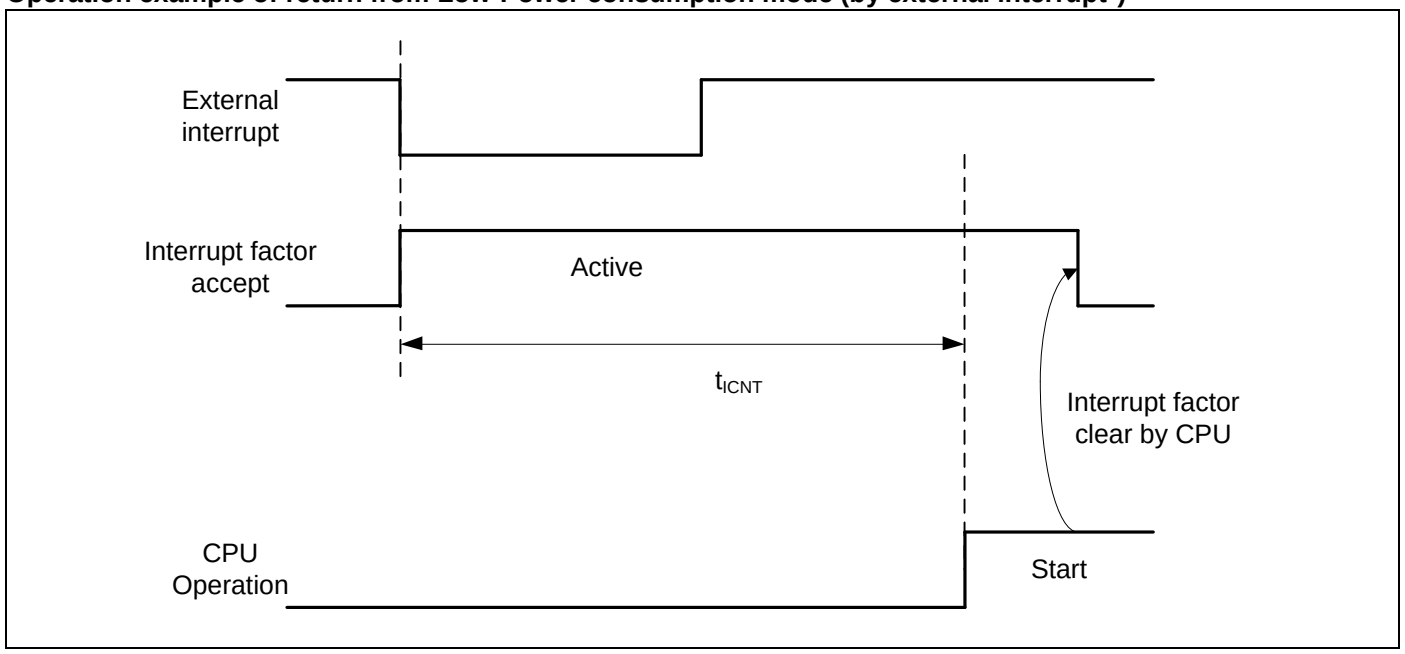
Return Count Time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	tICNT	t_{CYCC}		µs	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		40	80	µs	
Low-speed CR Timer mode		340	680	µs	
Sub Timer mode		680	860	µs	
RTC mode, Stop mode		268	503	µs	
Deep Standby RTC mode		308	583	µs	When RAM is off
Deep Standby Stop mode		268	503	µs	When RAM is on

*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by external interrupt*)



*: External interrupt is set to detecting fall edge.

Page	Section	Change Results
85	8. Flash Memory Write/Erase Characteristics	Changed the title of Chapter. Main Flash Memory Write/Erase Characteristics → Flash Memory Write/Erase Characteristics
86	9. Return Time Low-Power Consumption Mode	Added the Chapter “Return Time from Low-Power Consumption Mode”.
Revision 3.0		
2	Features USB Interface	Added the description of PLL for USB
35, 36	I/O Circuit Type	Added about +B input
48	Memory Map Memory map(2)	Added the summary of Flash memory sector and the note
52	PIN STATUS IN EACH CPU STAE List of Pin Status	Changed the pin status of I-type
55, 56	Electrical Characteristics 1. Absolute Maximum Ratings	Added the Clamp maximum current Added about +B input
58-60	Electrical Characteristics 3. DC Characteristics (1) Current rating	Changed the table format Added Main TIMER mode current Moved A/D Converter Current Moved D/A Converter Current
65	Electrical Characteristics 4. AC Characteristics (4-1) Operating Conditions of Main PLL (4-2) Operating Conditions of Main PLL	· Added the figure of Main PLL connection
68-75	Electrical Characteristics 4. AC Characteristics (7) CSIO/UART Timing	· Modified from UART Timing to CSIO/UART Timing · Changed from Internal shift clock operation to Master mode · Changed from External shift clock operation to Slave mode
76	Electrical Characteristics 4. AC Characteristics (9) External Input Timing	Added input pulse width of WKUPx pin
81	Electrical Characteristics 5. 12bit A/D Converter	· Added the typical value of Integral Nonlinearity, Differential Nonlinearity, Zero transition voltage and Full-scale transition voltage · Added Conversion time at AVcc < 4.5V
92, 93	Ordering Information	Change to full part number

NOTE: Please see “Document History” about later revised information.