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What is "Embedded - Microcontrollers"?

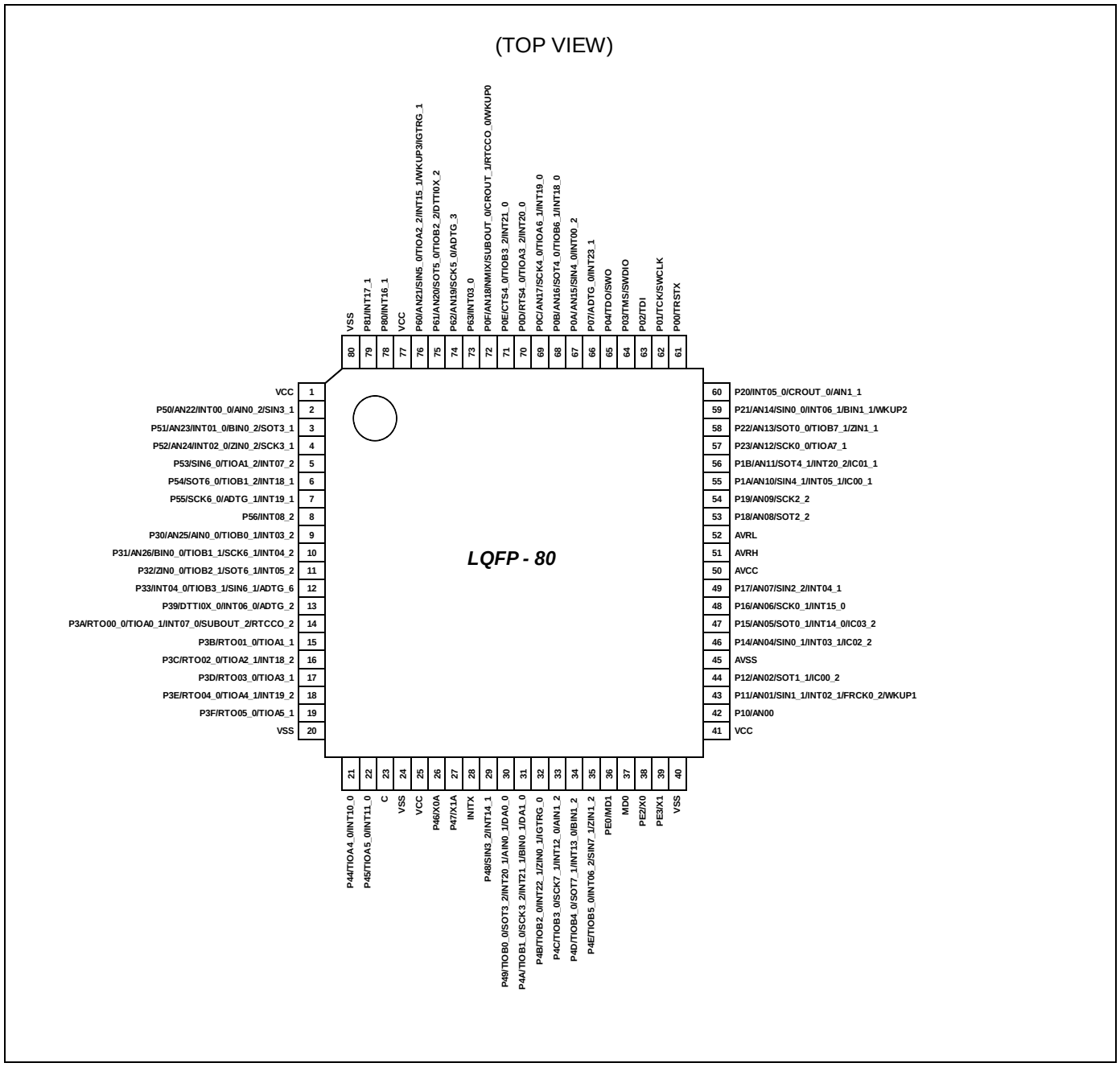
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CSIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	65
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9bf124mpmc-g-jne2

3. Pin Assignment

FPT-80-M37/M40



Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
38	L9	30	22	X0 PE2	A	A
39	L10	31	23	X1 PE3	A	B
40	L11	32	24	VSS	-	
41	K11	33	-	VCC	-	
42	J11	34	25	P10 AN00	F	M
43	J10	35	26	P11 AN01 SIN1_1 INT02_1 FRCK0_2 WKUP1	F	N
44	J8	36	27	P12 AN02 SOT1_1 (SDA1_1) IC00_2	F	M
45	H10	37	28	AVSS	-	
46	H9	38	29	P14 AN04 INT03_1 IC02_2 SIN0_1	F	N
47	G10	39	30	P15 AN05 IC03_2 SOT0_1 (SDA0_1) INT14_0	F	N
48	G9	-	-	P16 AN06 SCK0_1 (SCL0_1) INT15_0	F	N
49	F10	40	-	P17 AN07 SIN2_2 INT04_1	F	N
50	H11	41	31	AVCC	-	
51	F11	42	32	AVRH	-	
52	G11	43	33	AVRL	-	
53	F9	44	-	P18 AN08 SOT2_2 (SDA2_2)	F	M
54	E11	45	-	P19 AN09 SCK2_2 (SCL2_2)	F	M

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
55	E10	-	-	P1A AN10 SIN4_1 INT05_1 IC00_1	F	N
56	E9	-	-	P1B AN11 SOT4_1 (SDA4_1) IC01_1 INT20_2	F	N
57	D10	46	34	P23 SCK0_0 (SCL0_0) TIOA7_1 AN12	F	M
58	D9	47	35	P22 SOT0_0 (SDA0_0) TIOB7_1 AN13	F	M
		-	-	ZIN1_1		
59	C11	48	36	P21 SIN0_0 INT06_1 WKUP2 BIN1_1 AN14	F	N
60	C10	-	-	P20 INT05_0 CROUT_0 AIN1_1	E	N
61	A10	49	37	P00 TRSTX	E	J
62	B9	50	38	P01 TCK SWCLK	E	J
63	B11	51	39	P02 TDI	E	J
64	A9	52	40	P03 TMS SWDIO	E	J
65	B8	53	41	P04 TDO SWO	E	J
66	A8	-	-	P07 ADTG_0 INT23_1	E	L
67	C8	54	-	P0A SIN4_0 INT00_2 AN15	J*	N

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
77	A4	61	45	VCC	-	
78	A3	62	46	P80 INT16_1	H	H
79	A2	63	47	P81 INT17_1	H	H
80	A1	64	48	VSS	-	
-	A5, A7, A11, B2, B10, C3, C9, F1, F2, F3, J3, J9, K2, K10, L6	-	-	VSS	-	

*: 5 V tolerant I/O

List of functions

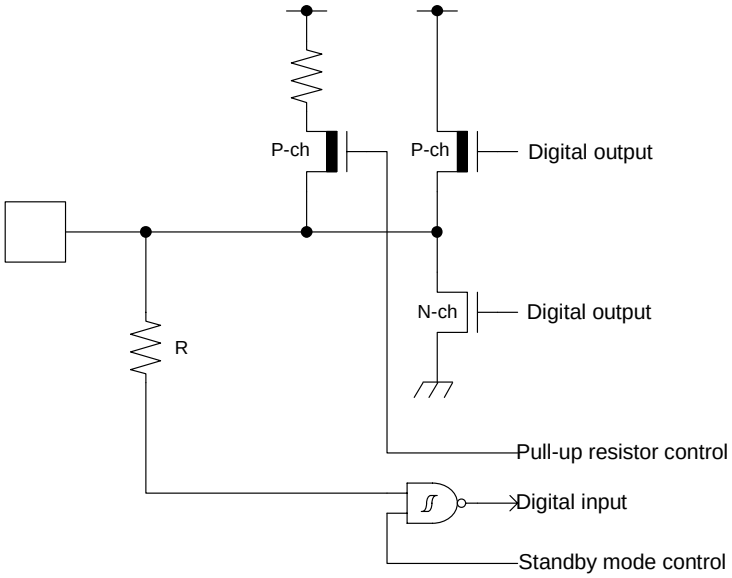
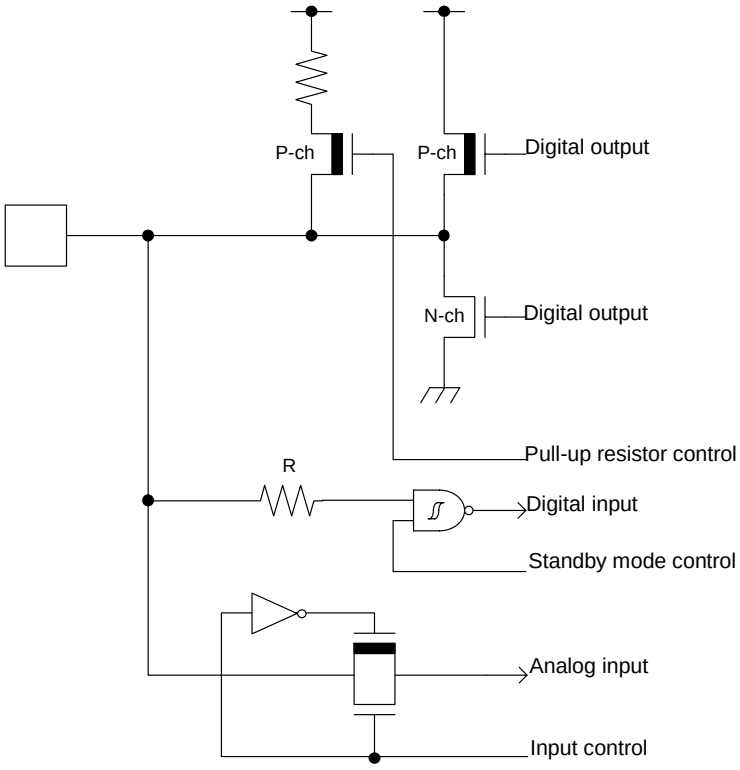
The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

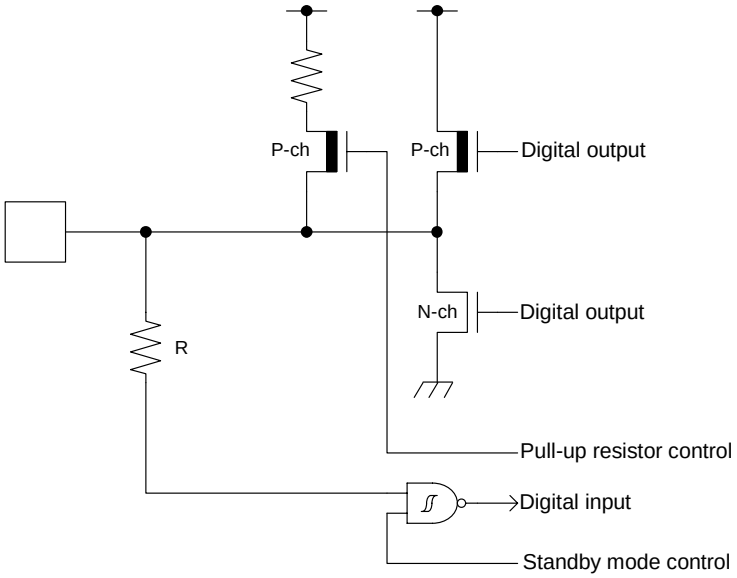
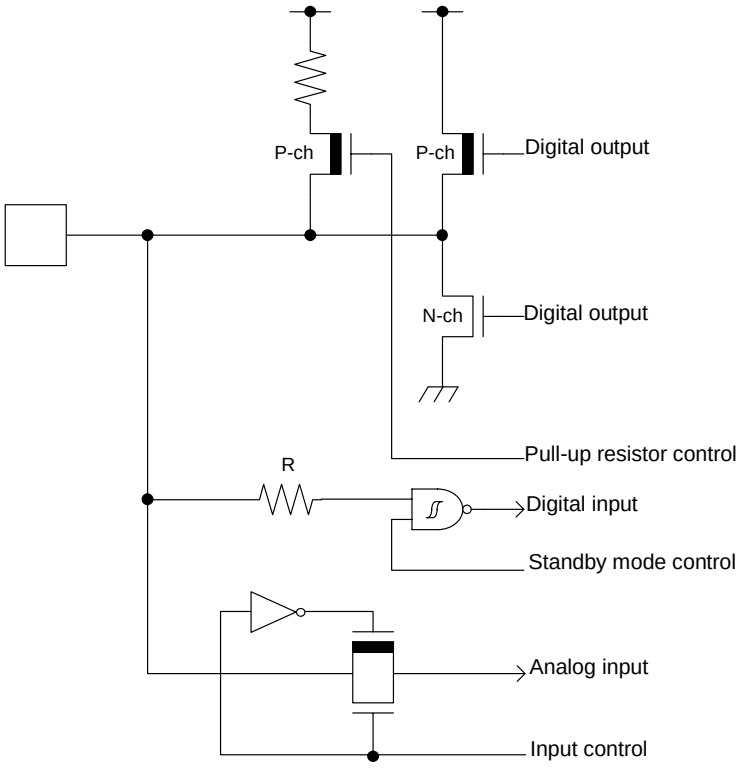
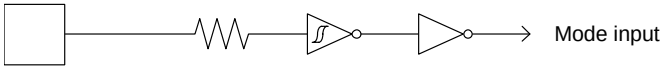
Pin function	Pin name	Function description	Pin No			
			LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48
ADC	ADTG_0	A/D converter external trigger input pin	66	A8	-	-
	ADTG_1		7	D3	-	-
	ADTG_2		13	G3	9	5
	ADTG_3		74	C5	58	-
	ADTG_6		12	G2	8	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	42	J11	34	25
	AN01		43	J10	35	26
	AN02		44	J8	36	27
	AN04		46	H9	38	29
	AN05		47	G10	39	30
	AN06		48	G9	-	-
	AN07		49	F10	40	-
	AN08		53	F9	44	-
	AN09		54	E11	45	-
	AN10		55	E10	-	-
	AN11		56	E9	-	-
	AN12		57	D10	46	34
	AN13		58	D9	47	35
	AN14		59	C11	48	36
	AN15		67	C8	54	-
	AN16		68	C7	55	-
	AN17		69	B7	56	-
	AN18		72	A6	57	42
	AN19		74	C5	58	-
	AN20		75	B4	59	43
	AN21		76	C4	60	44
	AN22		2	C1	2	2
	AN23		3	C2	3	3
	AN24		4	B3	4	4
	AN25		9	E2	5	-
	AN26		10	E3	6	-
Base Timer 0	TIOA0_1	Base timer ch.0 TIOA pin	14	H1	10	6
	TIOB0_0	Base timer ch.0 TIOB pin	30	K6	22	18
	TIOB0_1		9	E2	5	-
Base Timer 1	TIOA1_1	Base timer ch.1 TIOA pin	15	H2	11	7
	TIOA1_2		5	D1	-	-
	TIOB1_0	Base timer ch.1 TIOB pin	31	J6	23	19
	TIOB1_1		10	E3	6	-
	TIOB1_2		6	D2	-	-
Base Timer 2	TIOA2_1	Base timer ch.2 TIOA pin	16	H3	12	8
	TIOA2_2		76	C4	60	44
	TIOB2_0	Base timer ch.2 TIOB pin	32	L7	24	-
	TIOB2_1		11	G1	7	-
	TIOB2_2		75	B4	59	43
Base Timer 3	TIOA3_1	Base timer ch.3 TIOA pin	17	J1	13	9
	TIOA3_2		70	B6	-	-
	TIOB3_0	Base timer ch.3 TIOB pin	33	K7	25	-
	TIOB3_1		12	G2	8	-
	TIOB3_2		71	C6	-	-
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	21	L5	-	-
	TIOA4_1		18	J2	14	10
	TIOB4_0	Base timer ch.4 TIOB pin	34	J7	26	-

Pin function	Pin name	Function description	Pin No			
			LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48
External Interrupt	INT00_0	External interrupt request 00 input pin	2	C1	2	2
	INT00_2		67	C8	54	-
	INT01_0	External interrupt request 01 input pin	3	C2	3	3
	INT02_0	External interrupt request 02 input pin	4	B3	4	4
	INT02_1		43	J10	35	26
	INT03_0	External interrupt request 03 input pin	73	B5	-	-
	INT03_1		46	H9	38	29
	INT03_2		9	E2	5	-
	INT04_0	External interrupt request 04 input pin	12	G2	8	-
	INT04_1		49	F10	40	-
	INT04_2		10	E3	6	-
	INT05_0	External interrupt request 05 input pin	60	P20	-	-
	INT05_1		55	E10	-	-
	INT05_2		11	G1	7	-
	INT06_0	External interrupt request 06 input pin	13	G3	9	5
	INT06_1		59	C11	48	36
	INT06_2		35	K8	27	-
	INT07_0	External interrupt request 07 input pin	14	H1	10	6
	INT07_2		5	D1	-	-
	INT08_2	External interrupt request 08 input pin	8	E1	-	-
	INT10_0	External interrupt request 10 input pin	21	L5	-	-
	INT11_0	External interrupt request 11 input pin	22	K5	-	-
	INT12_0	External interrupt request 12 input pin	33	K7	25	-
	INT13_0	External interrupt request 13 input pin	34	J7	26	-
	INT14_0	External interrupt request 14 input pin	47	G10	39	30
	INT14_1		29	J5	-	-
	INT15_0	External interrupt request 15 input pin	48	G9	-	-
	INT15_1		76	C4	60	44
	INT16_1	External interrupt request 16 input pin	78	A3	62	46
	INT17_1	External interrupt request 17 input pin	79	A2	63	47
	INT18_0	External interrupt request 18 input pin	68	C7	55	-
	INT18_1		6	D2	-	-
	INT18_2		16	H3	12	8
	INT19_0	External interrupt request 19 input pin	59	C11	56	-
	INT19_1		7	D3	-	-
	INT19_2		18	J2	14	10
	INT20_0	External interrupt request 20 input pin	70	B6	-	-
	INT20_1		30	K6	22	18
	INT20_2		56	E9	-	-
	INT21_0	External interrupt request 21 input pin	71	C6	-	-
	INT21_1		31	J6	23	19
	INT22_1	External interrupt request 22 input pin	32	L7	24	-
	INT23_1	External interrupt request 23 input pin	66	A8	-	-
	NMIX	Non-Maskable Interrupt input pin	72	A6	57	42

Pin function	Pin name	Function description	Pin No			
			LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48
Multi-function Serial 6	SIN6_0	Multi-function serial interface ch.6 input pin	5	D1	-	-
	SIN6_1		12	G2	8	-
	SOT6_0 (SDA6_0)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I^2C (operation mode 4).	6	D2	-	-
	SOT6_1 (SDA6_1)		11	G1	7	-
	SCK6_0 (SCL6_0)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a CSIO (operation mode 2) and as SCL6 when it is used in an I^2C (operation mode 4).	7	D3	-	-
	SCK6_1 (SCL6_1)		10	E3	6	-
Multi-function Serial 7	SIN7_1	Multi-function serial interface ch.7 input pin	35	K8	27	-
	SOT7_1 (SDA7_1)	Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I^2C (operation mode 4).	34	J7	26	-
	SCK7_1 (SCL7_1)	Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a CSIO (operation mode 2) and as SCL7 when it is used in an I^2C (operation mode 4).	33	K7	25	-

Pin function	Pin name	Function description	Pin No			
			LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of Real-time clock	72	A6	57	42
	RTCCO_2		14	H1	10	6
	SUBOUT_0	Sub clock output pin	72	A6	57	42
	SUBOUT_2		14	H1	10	6
Low-Power Consumption Mode	WKUP0	Deep standby mode return signal input pin 0	72	A6	57	42
	WKUP1	Deep standby mode return signal input pin 1	43	J10	35	26
	WKUP2	Deep standby mode return signal input pin 2	59	C11	48	36
	WKUP3	Deep standby mode return signal input pin 3	76	C4	60	44
DAC	DA0	D/A converter ch.0 analog output pin	30	K6	22	18
	DA1	D/A converter ch.1 analog output pin	31	J6	23	19
RESET	INITX	External Reset Input pin. A reset is valid when INITX="L".	28	K4	21	17
Mode	MD0	Mode 0 pin. During normal operation, MD0="L" must be input. During serial programming to Flash memory, MD0="H" must be input.	37	L8	29	21
	MD1	Mode 1 pin. During serial programming to Flash memory, MD1="L" must be input.	36	K9	28	20
POWER	VCC	Power supply Pin	1	B1	1	1
	VCC	Power supply Pin	25	K1	18	14
	VCC	Power supply Pin	41	K11	33	-
	VCC	Power supply Pin	77	A4	61	45
GND	VSS	GND Pin	-	F1	-	-
	VSS	GND Pin	-	F2	-	-
	VSS	GND Pin	-	F3	-	-
	VSS	GND Pin	-	B2	-	-
	VSS	GND Pin	20	L1	16	12
	VSS	GND Pin	-	K2	-	-
	VSS	GND Pin	-	J3	-	-
	VSS	GND Pin	-	L6	-	-
	VSS	GND Pin	24	L4	-	-
	VSS	GND Pin	40	L11	32	24
	VSS	GND Pin	-	K10	-	-
	VSS	GND Pin	-	J9	-	-
	VSS	GND Pin	-	B10	-	-
	VSS	GND Pin	-	C9	-	-
	VSS	GND Pin	-	D11	-	-
	VSS	GND Pin	-	A11	-	-
	VSS	GND Pin	-	A7	-	-
	VSS	GND Pin	-	C3	-	-
	VSS	GND Pin	-	A5	-	-
	VSS	GND Pin	80	A1	64	48
CLOCK	X0	Main clock (oscillation) input pin	38	L9	30	22
	X0A	Sub clock (oscillation) input pin	26	L3	19	15
	X1	Main clock (oscillation) I/O pin	39	L10	31	23
	X1A	Sub clock (oscillation) I/O pin	27	K3	20	16
	CROUT_0	Built-in high-speed CR-osc clock output port	60	C10	-	-
	CROUT_1		72	A6	57	42
Analog POWER	AVCC	A/D converter and D/A converter analog power supply pin	50	H11	41	31
	AVRH	A/D converter analog reference voltage input pin	51	F11	42	32
Analog GND	AVSS	A/D converter and D/A converter GND pin	45	H10	37	28
	AVRL	A/D converter analog reference voltage input pin	52	G11	43	33
C pin	C	Power supply stabilization capacity pin	23	L2	17	13

Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available
F		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available

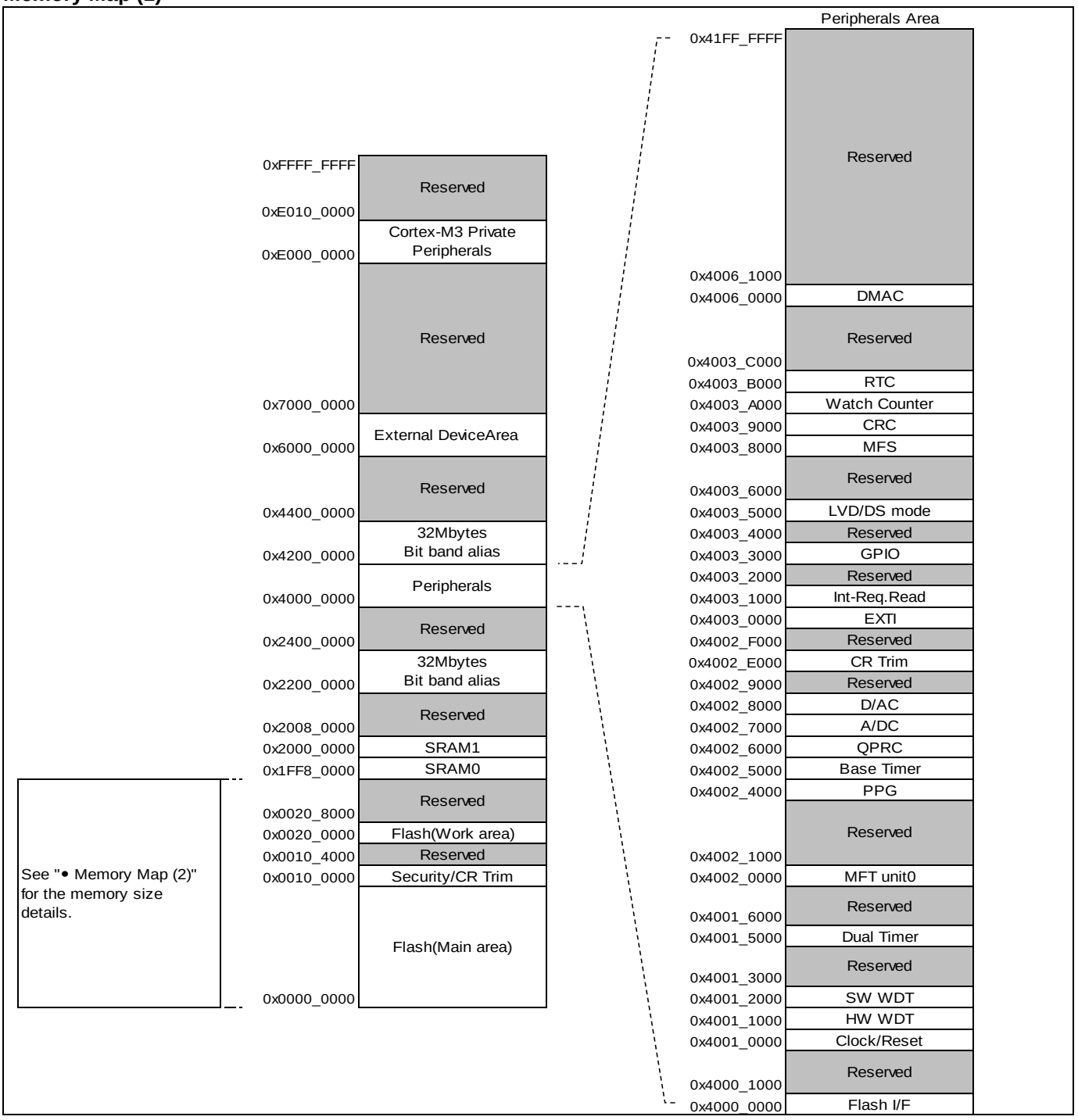
Type	Circuit	Remarks
I		• CMOS level output • CMOS level hysteresis input • 5 V tolerant • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA • Available to control PZR registers. • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
J		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • 5 V tolerant • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA • Available to control PZR registers. • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
K		• CMOS level hysteresis input

9. Memory Size

See "Memory Size" in "Product Lineup" to confirm the memory size.

10. Memory Map

Memory Map (1)



12.3 DC Characteristics

12.3.1 Current Rating

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ	Max		
Run mode current	I_{CC}	VCC	PLL Run mode	CPU : 72MHz, Peripheral : 36MHz	32.5	41	mA	*1, *5
				CPU:72MHz, Peripheral clock stops NOP operation	18	23	mA	*1, *5
			High-speed CR Run mode	CPU/ Peripheral : 4MHz*2	2.5	3.4	mA	*1
			Sub Run mode	CPU/ Peripheral : 32kHz	110	980	µA	*1, *6
			Low-speed CR Run mode	CPU/ Peripheral : 100kHz	130	1030	µA	*1
Sleep mode current	I_{CCS}		PLL Sleep mode	Peripheral : 36MHz	22	28	mA	*1, *5
			High-speed CR Sleep mode	Peripheral : 4MHz*2	1.6	2.6	mA	*1
			Sub Sleep mode	Peripheral : 32kHz	96	955	µA	*1, *6
			Low-speed CR Sleep mode	Peripheral : 100kHz	115	975	µA	*1

*1: When all ports are fixed.

*2: When setting it to 4 MHz by trimming.

*3: T_A=+25°C, V_{CC}=5.5 V

*4: T_A=+105°C, V_{CC}=5.5 V

*5: When using the crystal oscillator of 4 MHz (Including the current consumption of the oscillation circuit)

*6: When using the crystal oscillator of 32 kHz (Including the current consumption of the oscillation circuit)

Built-in Low-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	

12.4.4 Operating Conditions of Main PLL (In the case of using main clock for input of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	5	-	37	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	75	-	150	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	72	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see "Chapter: Clock" in "FM3 Family Peripheral Manual".

12.4.5 Operating Conditions of Main PLL (In the case of using built-in high-speed CR for input clock of Main PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

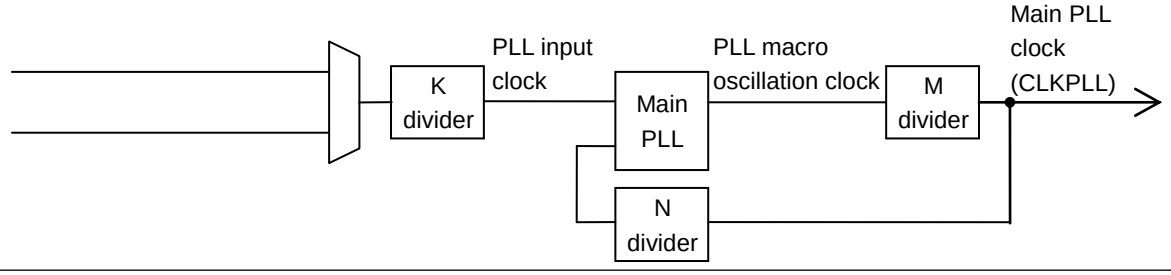
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	3.8	4	4.2	MHz	
PLL multiplication rate	-	19	-	35	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	72	-	150	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	72	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see "Chapter 2-1: Clock" in "FM3 Family Peripheral Manual".

Note: Make sure to input to the Main PLL source clock, the high-speed CR clock (CLKHC) that the frequency/temperature has been trimmed.
When setting PLL multiple rate, please take the accuracy of the built-in high-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.

Main PLL connection



12.4.9 CSIO/UART Timing

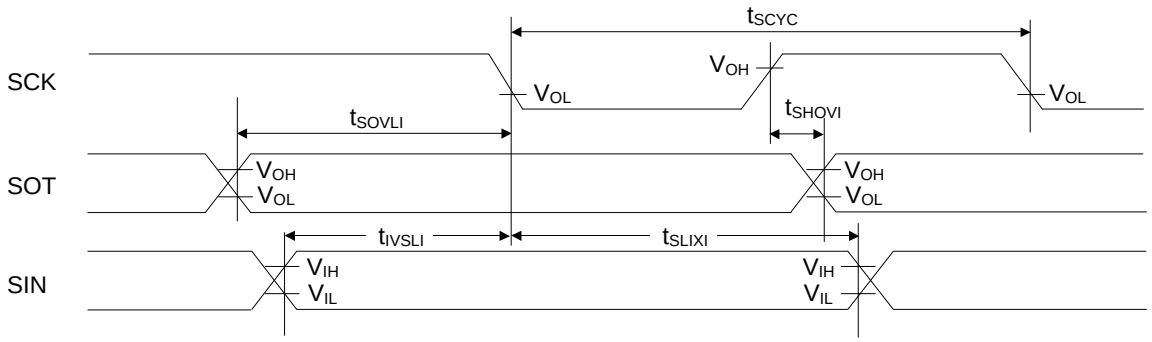
CSIO (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

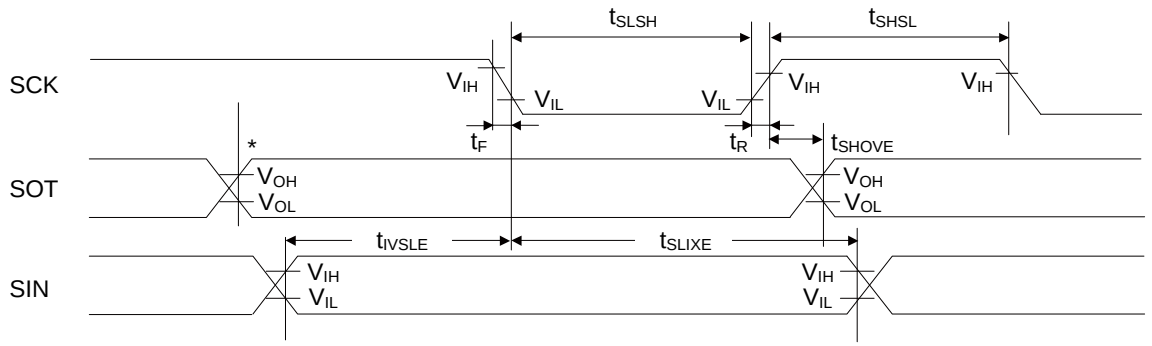
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function serial is connected to, see "Block Diagram" in this data sheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 30 pF.



Master mode



Slave mode

*: Changes when writing to TDR register

CSIO (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function serial is connected to, see "Block Diagram" in this data sheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 30 pF.

12.7 Low-Voltage Detection Characteristics

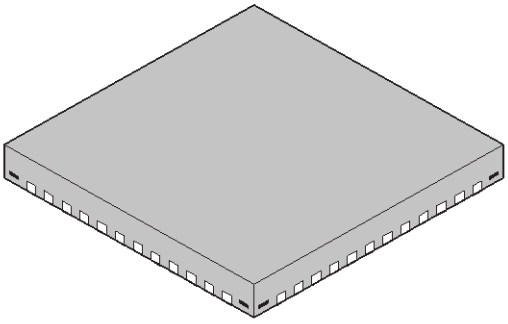
12.7.1 Low-Voltage Detection Reset

(T_A = - 40°C to + 105°C)

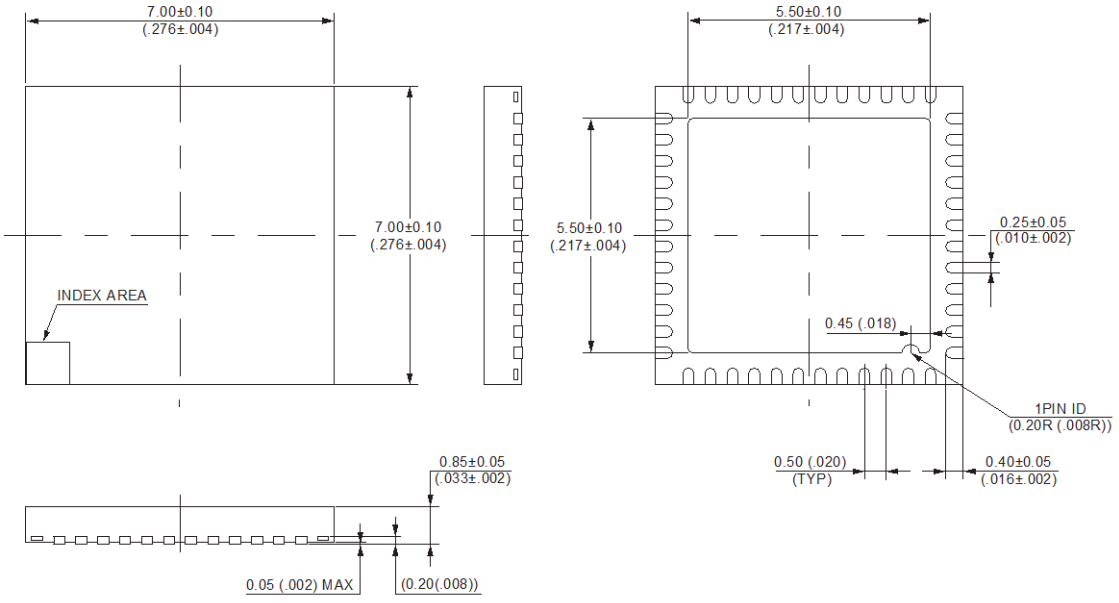
Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHR*1= 00000	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH		2.30	2.50	2.70	V	When voltage rises
Detected voltage	VDL	SVHR*1= 00001	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH		2.48	2.70	2.92	V	When voltage rises
Detected voltage	VDL	SVHR*1= 00010	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH		2.58	2.80	3.02	V	When voltage rises
Detected voltage	VDL	SVHR*1= 00011	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVHR*1= 00100	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVHR*1= 00101	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		3.04	3.30	3.56	V	When voltage rises
Detected voltage	VDL	SVHR*1= 00110	3.31	3.60	3.89	V	When voltage drops
Released voltage	VDH		3.40	3.70	4.00	V	When voltage rises
Detected voltage	VDL	SVHR*1= 00111	3.40	3.70	4.00	V	When voltage drops
Released voltage	VDH		3.50	3.80	4.10	V	When voltage rises
Detected voltage	VDL	SVHR*1= 01000	3.68	4.00	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.10	4.43	V	When voltage rises
Detected voltage	VDL	SVHR*1= 01001	3.77	4.10	4.43	V	When voltage drops
Released voltage	VDH		3.86	4.20	4.54	V	When voltage rises
Detected voltage	VDL	SVHR*1= 01010	3.86	4.20	4.54	V	When voltage drops
Released voltage	VDH		3.96	4.30	4.64	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	8160 × t_{CYCP}*2	µs	
LVD detection delay time	t_{LVDDL}	-	-	-	200	µs	

*1: The SVHR bit of Low-Voltage Detection Voltage Control Register (LVD_CTL) is initialized to "00000" by Low-Voltage Detection Reset.

*2: t_{CYCP} indicates the APB2 bus clock cycle time.

48-pin plastic QFN		
	Lead pitch	0.5 mm
	Package width × package length	7.00 mm × 7.00 mm
	Sealing method	Plastic mold
	Mounting height	0.90 mm MAX
	Weight	–
(LCC-48P-M73)		

48-pin plastic QFN
(LCC-48P-M73)



Dimensions in mm (inches).
Note: The values in parentheses are reference **values.**

15. Major Changes

Spansion Publication Number: MB9B120M_DS706-00050

Page	Section	Change Results
Revision 1.0		
-	-	Preliminary → Data Sheet
3	FEATURES A/D Converter (Max 26channels)	Revised the conversion time: 1.0µs → 0.8µs
5	UniqueID	Added the "Unique ID".
6	PRODUCT LINEUP Function	Added the "Unique ID".
15 to 17	LIST OF PIN FUNCTIONS List of pin numbers	Corrected the I/O circuit type. Corrected the Pin state type.
32	List of pin functions	Corrected the Pin function.
38	I/O CIRCUIT TYPE	Added the "Type: L".
45	BLOCK DIAGRAM	Corrected the figure. - TIOA: input → input/output - TIOB: output → input
54	ELECTRICAL CHARACTERISTICS 1. Absolute Maximum Ratings	Revised the value of "TBD".
55	2. Recommended Operating Conditions	Revised the Condition of "Operating temperature".
56, 57	3. DC Characteristics (1) Current Rating	Revised the value of "TBD". Added "Flash memory write/erase current".
60	4. AC Characteristics (3) Built-in CR Oscillation Characteristics	Revised the Condition. Revised the footnote.
61	(4-2) Operating Conditions of Main PLL (In the case of using built-in high-speed CR for input clock of main PLL)	Revised the value of "TBD".
77	5. 12-bit A/D Converter Electrical characteristics for the A/D converter	Deleted "(Preliminary value)". Revised the conversion time. Min: 1.0µs → 0.8µs Revised the value of "Compare clock cycle ($AV_{CC} \geq 4.5V$)". Min: 50ns → 40ns Revised the footnote.
80	6. 10-bit D/A Converter	Deleted "(Preliminary value)".
81	7. Low-Voltage Detection Characteristics	Revised the value of "TBD".
82	8. MainFlash Memory Write/Erase Characteristics	Revised the value of "TBD". Revised the value of "Sector erase time". - Large Sector Typ: 1.065s → 1.1s - Small Sector Typ: 0.606s → 0.3s Revised the value of "Chip erase time". Typ: 9.11s → 6.8s Deleted "(targeted value)".
Revision 1.1		
-	-	Company name and layout design change
Revision 2.0		
2	FEATURES On-chip Memories [Flash memory]	Revised the features of Dual operation Flash memory
	Multi-function Serial Interface [I^2C]	Corrected the mode. High speed mode → Fast mode
3	General-Purpose I/O Port	Revised the features of 5V tolerant I/O.
4	Multi-function Timer	Corrected the number of A/D activating compare channels. 3ch. → 2ch.
6	PRODUCT LINEUP Function	Corrected the number of A/D activating compare channels. 3ch. → 2ch. Revised Built-in CR. High-speed: 4MHz(± 2%) → 4MHz Low-speed: 100kHz(Typ) → 100kHz
7		Revised the footnote.

Document History

Document Title: MB9B120M Series 32-Bit ARM® Cortex®-M3 FM3 Microcontroller
Document Number: 002-05655

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	TOYO	03/18/2015	Migrated to Cypress and assigned document number 002-05655. No change to document contents or format.
*A	5171443	TOYO	03/18/2016	Updated to Cypress format.