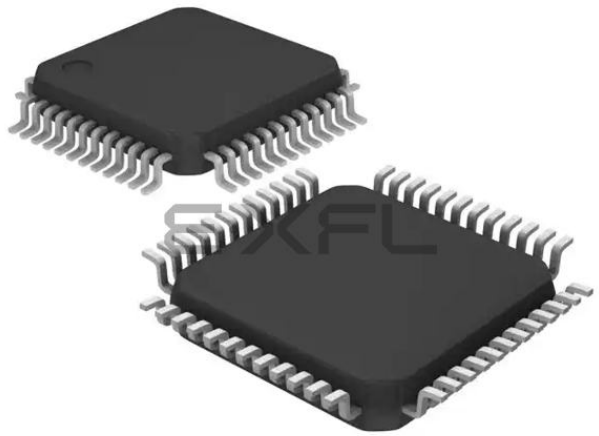

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PS2, PWM, WDT
Number of I/O	30
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc122lc1an

List of Figures

4 BLOCK DIAGRAM

4.1 NuMicro™ NUC122 Block Diagram

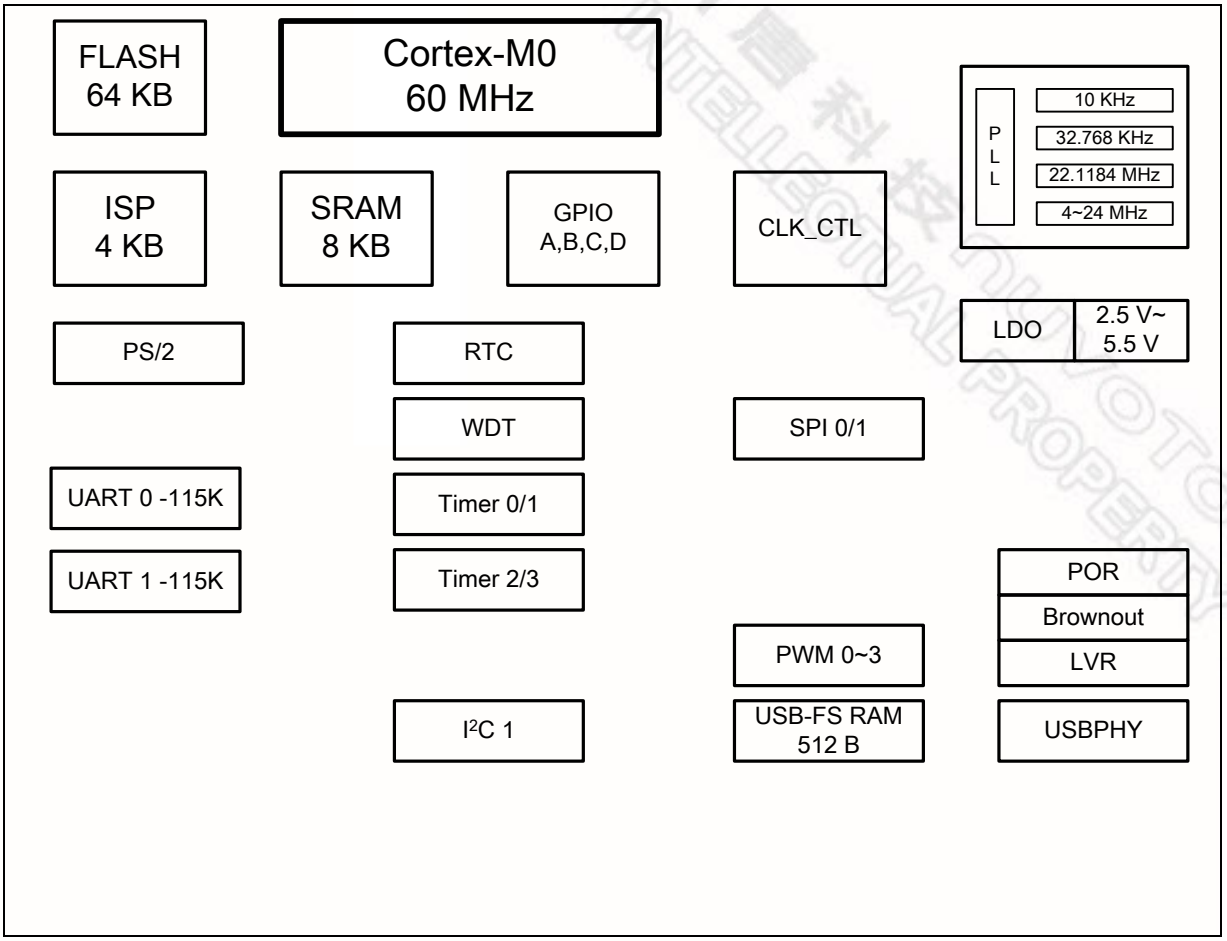


Figure 4-1 NuMicro™ NUC122 Block Diagram

5.2.3 System Power Distribution

In this chip, the power distribution is divided into three segments.

- Analog power from AVDD and AVSS provides the power for analog components operation.
- Digital power from VDD and VSS supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.
- USB transceiver power from VBUS offers the power for operating the USB transceiver.

The outputs of internal voltage regulators, LDO and VDD33, require an external capacitor which should be located close to the corresponding pin. Analog power (AVDD) should be the same voltage level of the digital power (VDD). The following diagram shows the power distribution of this chip.

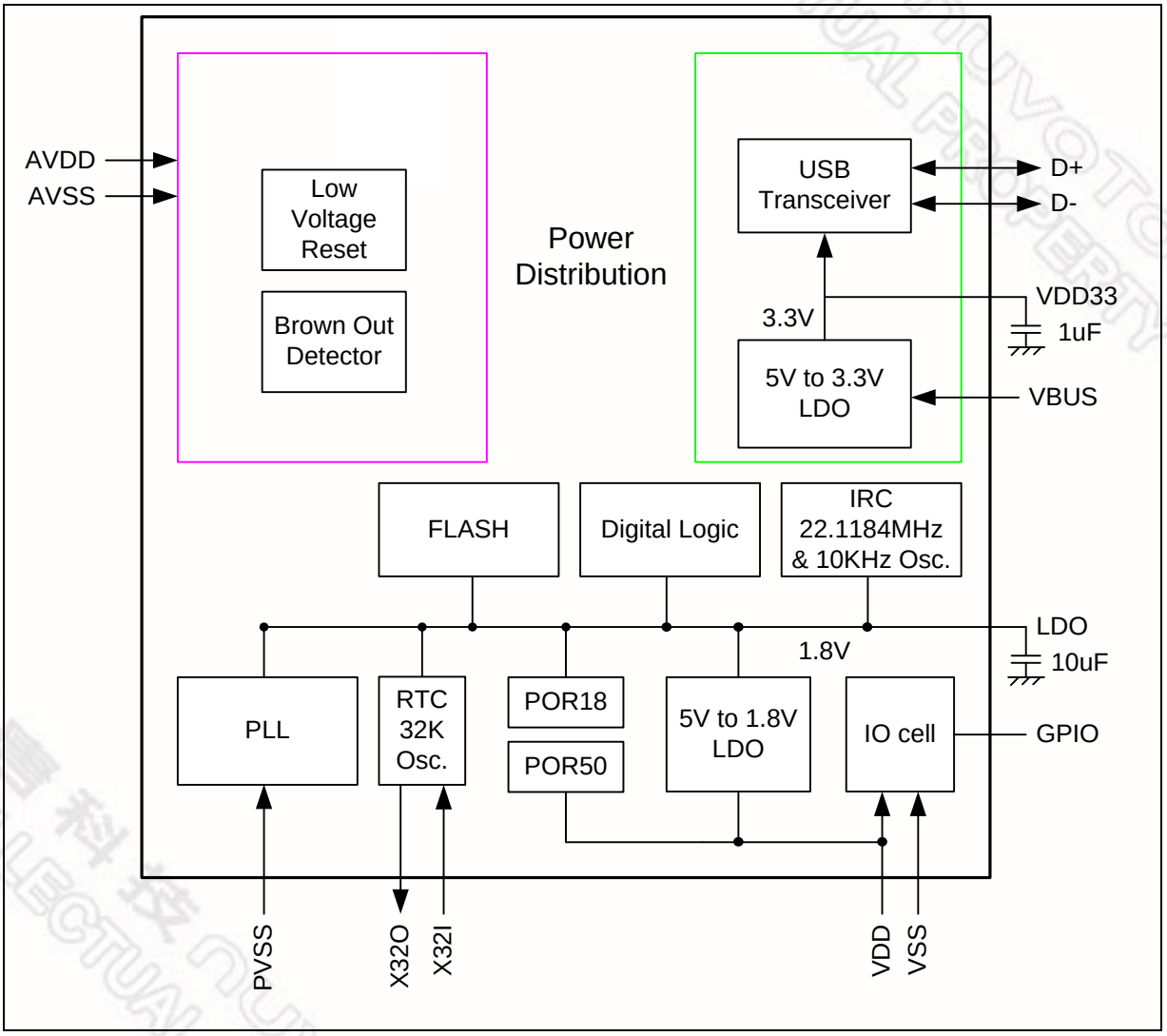


Figure 5-2 NuMicro™ NUC122 Power Distribution Diagram

5.2.5.1 Exception Model and System Interrupt Map

The following table lists the exception model supported by NuMicro™ NUC122. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0” and the lowest priority is denoted as “3”. The default priority of all the user-configurable interrupts is “0”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 5-1 Exception Model

Vector Number	Interrupt Number (Bit in Interrupt Registers)	Interrupt Name	Source IP	Interrupt description
0 ~ 15	-	-	-	System exceptions
16	0	**BOD_OUT**	Brownout	Brownout low voltage detected interrupt
17	1	**WDT_INT**	WDT	Watchdog Timer interrupt
18	2	**EINT0**	GPIO	External signal interrupt from PB.14 pin
19	3	**EINT1**	GPIO	External signal interrupt from PB.15 pin
20	4	**GPAB_INT**	GPIO	External signal interrupt from PA[15:0]/PB[13:0]
21	5	**GPCD_INT**	GPIO	External interrupt from PC[15:0]/PD[15:0]
22	6	**PWMA_INT**	PWM0~3	PWM0, PWM1, PWM2 and PWM3 interrupt
23	7	**Reserved**	Reserved	Reserved
24	8	**TMR0_INT**	TMR0	Timer 0 interrupt
25	9	**TMR1_INT**	TMR1	Timer 1 interrupt
26	10	**TMR2_INT**	TMR2	Timer 2 interrupt
27	11	**TMR3_INT**	TMR3	Timer 3 interrupt

5.2.5.2 Vector Table

When any interrupts is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARM® v6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 5-3 Vector Table Format

5.2.5.3 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

5.6 Timer Controller (TMR)

5.6.1 Overview

The timer controller includes four 32-bit timers, TIMER0~TIMER3, which allows user to easily implement a timer control for applications. The timer can perform functions like frequency measurement, event counting, interval measurement, clock generation, delay timing, and so on. The timer can generates an interrupt signal upon timeout, or provide the current value during operation.

5.6.2 Features

- 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Time out period = (Period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}), T is the period of timer clock
- 24-bit timer value is readable through TDR (Timer Data Register)
- Support event counting function to count the event from external pin

5.10 UART Interface Controller (UART)

NuMicro™ NUC122 provides two channels of Universal Asynchronous Receiver/Transmitters (UART0/1). Both of UART0 and UART1 perform Normal Speed UART, besides, UART0 and UART1 also support flow control function.

5.10.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART0/1) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function and RS-485 mode functions. Each UART channel supports seven types of interrupts including transmitter FIFO empty interrupt (INT_THRE), receiver threshold level reaching interrupt (INT_RDA), line status interrupt (parity error or framing error or break interrupt) (INT_RLS), receiver buffer time-out interrupt (INT_TOUT), MODEM/Wake-Up status interrupt (INT_MODEM), Buffer error interrupt (INT_BUF_ERR). Interrupt number 13 (vector number is 29) supports UART0/1 interrupt. Refer to Nested Vectored Interrupt Controller chapter for System Interrupt Map.

The UART0/1 are equipped 14-byte transmitter FIFO (TX_FIFO) and 14-byte receiver FIFO (RX_FIFO). The CPU can read the status of the UART at any time during the operation. The reported status information includes the type and condition of the transfer operations being performed by the UART, as well as 4 error conditions (parity error, framing error, break interrupt and buffer error) probably occur while receiving data. The UART includes a programmable baud rate generator that is capable of dividing clock input by divisors to produce the serial clock that transmitter and receiver need. The baud rate equation is Baud Rate = UART_CLK / M * [BRD + 2], where M and BRD are defined in Baud Rate Divider Register (UA_BAUD). Below table lists the equations in the various conditions and the UART baud rate setting table.

Mode	DIV_X_EN	DIV_X_ONE	Divider X	BRD	Baud rate equation
0	0	0	B	A	UART_CLK / [16 * (A+2)]
1	1	0	B	A	UART_CLK / [(B+1) * (A+2)] , B must >= 8
2	1	1	Don't care	A	UART_CLK / (A+2), A must >=3

Table 5-5 UART Baud Rate Equation

System clock = 22.1184 MHz high speed			
Baud rate	Mode0	Mode1	Mode2
921600	x	A=0,B=11	A=22
460800	A=1	A=1,B=15 A=2,B=11	A=46
230400	A=4	A=4,B=15 A=6,B=11	A=94
115200	A=10	A=10,B=15 A=14,B=11	A=190
57600	A=22	A=22,B=15 A=30,B=11	A=382

5.10.2 Features

- Full duplex, asynchronous communications
- Separate receive / transmit 14 bytes entry FIFO for data payloads
- Support hardware auto flow control/flow control function (CTS, RTS) and programmable RTS flow control trigger level
- Programmable receiver buffer trigger level
- Support programmable baud-rate generator for each channel individually
- Support CTS wake-up function
- Support 8 bits receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting UA_TOR [DLY] register
- Support break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5, 6, 7, 8 bits character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bits generation
- Support IrDA SIR function mode
  - Support for 3/16 bits duration for normal mode
- Support RS-485 function mode.
  - Support RS-485 9-bit mode
  - Support hardware or software direct enable control provided by RTS pin

6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into VDD		-	120	mA
Maximum Current out of VSS			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

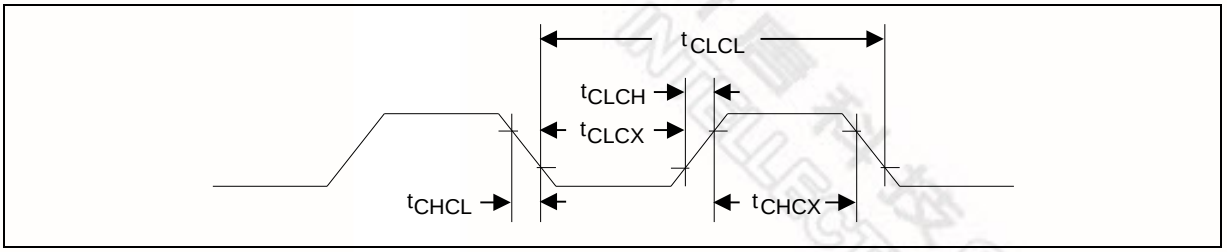
Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
						disable all IP and PLL, XTAL=4 MHz
	I_{DD11}		3		mA	V_{DD} = 3.3 V @ 4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{DD12}		2		mA	V_{DD} = 3.3 V @ 4 MHz, disable all IP and PLL, XTAL=4 MHz
Operating Current Idle Mode @ 60 MHz	I_{IDLE1}		17		mA	V_{DD} = 5.5 V @ 60 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{IDLE2}		12		mA	V_{DD} = 5.5 V @ 60 MHz, disable all IP and enable PLL, XTAL=12 MHz
	I_{IDLE3}		15		mA	V_{DD} = 3.3 V @ 60 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{IDLE4}		11		mA	V_{DD} = 3.3 V @ 60 MHz, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Idle Mode @ 12 MHz	I_{IDLE5}		4.5		mA	V_{DD} = 5.5 V @ 12 MHz, enable all IP and disable PLL, XTAL=12 MHz
	I_{IDLE6}		3.5		mA	V_{DD} = 5.5 V @ 12 MHz, disable all IP and PLL, XTAL=12 MHz
	I_{IDLE7}		3		mA	V_{DD} = 3.3 V @ 12 MHz, enable all IP and disable PLL, XTAL=12 MHz
	I_{IDLE8}		2		mA	V_{DD} = 3.3 V @ 12 MHz, disable all IP and PLL, XTAL=12 MHz
Operating Current Idle Mode @ 4 MHz	I_{IDLE9}		3		mA	V_{DD} = 5.5 V @ 4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{IDLE10}		2.5		mA	V_{DD} = 5.5 V @ 4 MHz, disable all IP and PLL, XTAL=4 MHz
	I_{IDLE11}		2		mA	V_{DD} = 3.3 V @ 4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{IDLE12}		1		mA	V_{DD} = 3.3 V @ 4 MHz, disable all IP and PLL, XTAL=4 MHz

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Standby Current Power Down Mode	I_{PWD1}		13		μA	V_{DD} = 5.5 V, RTC OFF, No load @ Disable BOV function
	I_{PWD2}		12		μA	V_{DD} = 3.3 V, RTC OFF, No load @ Disable BOV function
	I_{PWD3}		15		μA	V_{DD} = 5.5 V, RTC run , No load @ Disable BOV function
	I_{PWD4}		13		μA	V_{DD} = 3.3 V, RTC run , No load @ Disable BOV function
Input Current PA, PB, PC, PD (Quasi-bidirectional mode)	I_{IN1}	-60	-	+15	μA	V_{DD} = 5.5 V, V_{IN} = 0 V or V_{IN}=V_{DD}
Input Current at /RESET[1]	I_{IN2}	-55	-45	-30	μA	V_{DD} = 3.3 V, V_{IN} = 0.45 V
Input Leakage Current PA, PB, PC, PD	I_{LK}	-2	-	+2	μA	V_{DD} = 5.5 V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current PA~PD (Quasi-bidirectional mode)	I_{TL} [3]	-650	-	-200	μA	V_{DD} = 5.5 V, V_{IN}<2.0 V
Input Low Voltage PA, PB, PC, PD (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5 V
		-0.3	-	0.6		V_{DD} = 2.5 V
Input High Voltage PA, PB, PC, PD(TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5 V
		1.5	-	V_{DD} +0.2		V_{DD} = 3.0 V
Input Low Voltage PA, PB, PC, PD (Schmitt input)	V_{IL2}	-0.5		0.4 V_{DD}	V	
Input High Voltage PA, PB, PC, PD(Schmitt input)	V_{IH2}	0.6 V_{DD}		V_{DD}+0.5	V	
Hysteresis voltage of PA~PD (Schmitt input)	V_{HY}		0.2 V_{DD}		V	
Negative going threshold (Schmitt input), /RESET	V_{ILS}	-0.5	-	0.3 V_{DD}	V	
Positive going threshold (Schmitt input), /RESET	V_{IHS}	0.7 V_{DD}	-	V_{DD}+0.5	V	
Source Current PA, PB, PC, PD (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	V_{DD} = 4.5 V, V_S = 2.4 V
	I_{SR12}	-50	-70	-90	μA	V_{DD} = 2.7 V, V_S = 2.2 V
	I_{SR12}	-40	-60	-80	μA	V_{DD} = 2.5 V, V_S = 2.0 V
Source Current PA, PB, PC, PD (Push-pull Mode)	I_{SR21}	-22	-28	-32	mA	V_{DD} = 4.5 V, V_S = 2.4 V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7 V, V_S = 2.2 V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5 V, V_S = 2.0 V

6.3 AC Electrical Characteristics

6.3.1 External 4~24 MHz High Speed Crystal AC Electrical Characteristics



Note: Duty cycle is 50 %.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		20	-	-	nS
t_{CLCX}	Clock Low Time		20	-	-	nS
t_{CLCH}	Clock Rise Time		-	-	10	nS
t_{CHCL}	Clock Fall Time		-	-	10	nS

6.3.2 External 4~24 MHz High Speed Crystal

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	℃

6.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	without	without	without

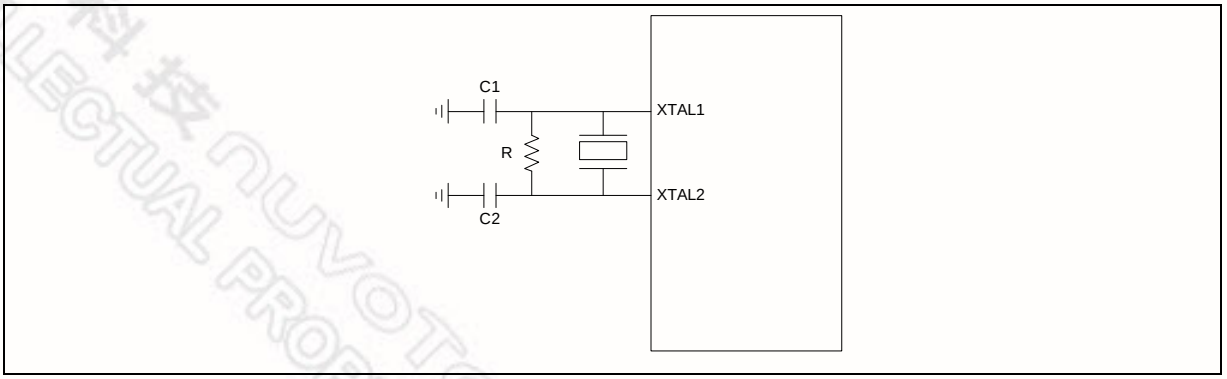


Figure 6-1 Typical Crystal Application Circuit

6.3.3 External 32.768 KHz Low Speed Crystal

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	-	32.768	-	KHz
Temperature	-	-40	-	85	℃

6.3.4 Internal 22.1184 MHz High Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Center Frequency	-	-	22.1184	-	MHz
Calibrated Internal Oscillator Frequency	+25 ℃; V_{DD} = 3.3 V	-1	-	+1	%
	-40 ℃ ~ +85 ℃; V_{DD} = 2.5 V ~ 5.5 V	-5	-	+5	%

6.3.5 Internal 10 KHz Low Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Center Frequency	-	-	10	-	KHz
Calibrated Internal Oscillator Frequency	+25℃; V_{DD} = 5 V	-30	-	+30	%
	-40 ℃ ~ +85 ℃; V_{DD} = 2.5 V ~ 5.5 V	-50	-	+50	%

6.4.2 Specification of Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent current	V_{DD}=5.5 V	-	-	5	μA
Temperature	-	-40	25	85	℃
Threshold voltage	Temperature=25 ℃	1.7	2.0	2.3	V
	Temperature=-40 ℃	-		-	V
	Temperature=85 ℃	-		-	V
Hysteresis	-	0	0	0	V

6.4.3 Specification of Brownout Detector

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent current	AV_{DD}=5.5 V	-	-	140	μA
Temperature	-	-40	25	85	℃
Brownout voltage	BOV_VL[1:0]=11	4.2	4.4	4.6	V
	BOV_VL [1:0]=10	3.6	3.75	3.9	V
	BOV_VL [1:0]=01	2.6	2.7	2.8	V
	BOV_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

6.4.4 Specification of Power-On Reset (5 V)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	℃
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA

6.5 SPI Dynamic Characteristics

6.5.1 Dynamic Characteristics of Data Input and Output Pin

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
SPI Master Mode (VDD = 4.5 V ~ 5.5 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	16	10	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	5	8	ns
SPI Master Mode (VDD = 3.0 V ~ 3.6 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	20	13	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	7	14	ns
SPI Slave Mode (VDD = 4.5 V ~ 5.5 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2*PCLK+4	-	-	ns
t_V	Data output valid time	-	2*PCLK+11	2*PCLK+20	ns
SPI Slave Mode (VDD = 3.0 V ~ 3.6 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2*PCLK+8	-	-	ns
t_V	Data output valid time	-	2*PCLK+20	2*PCLK+32	ns

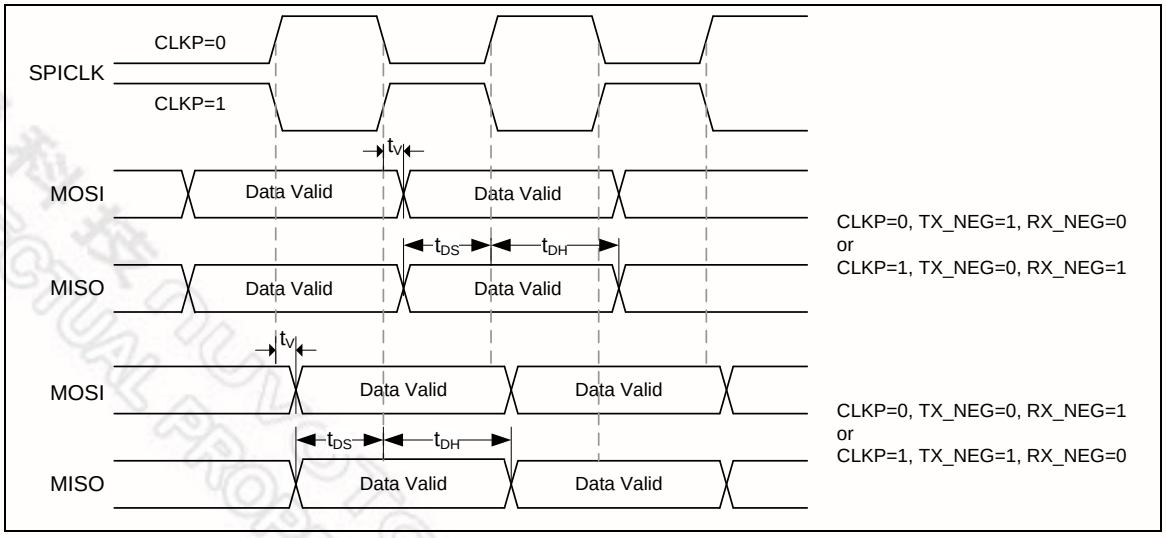
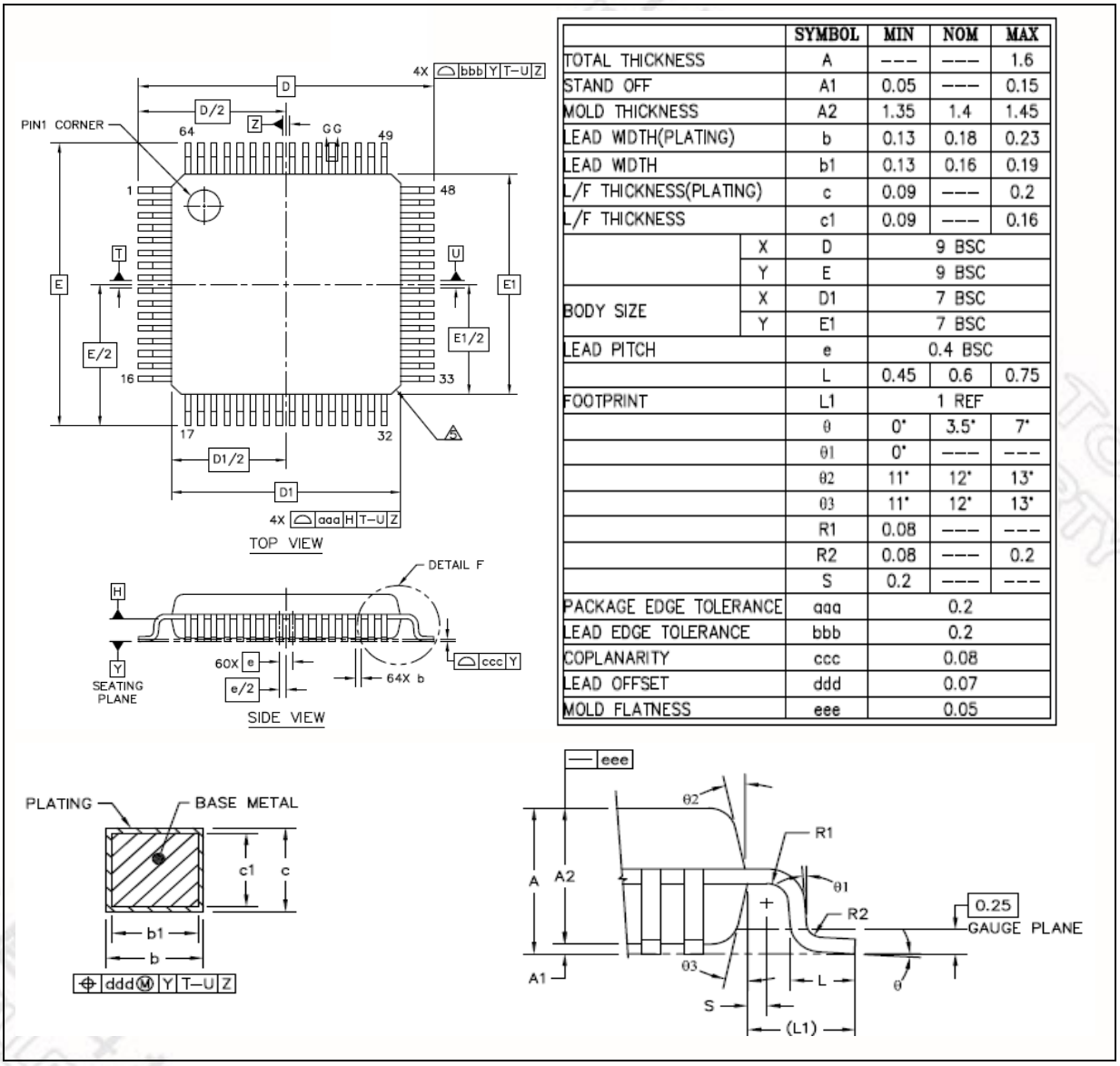


Figure 6-2 SPI Master Mode Timing

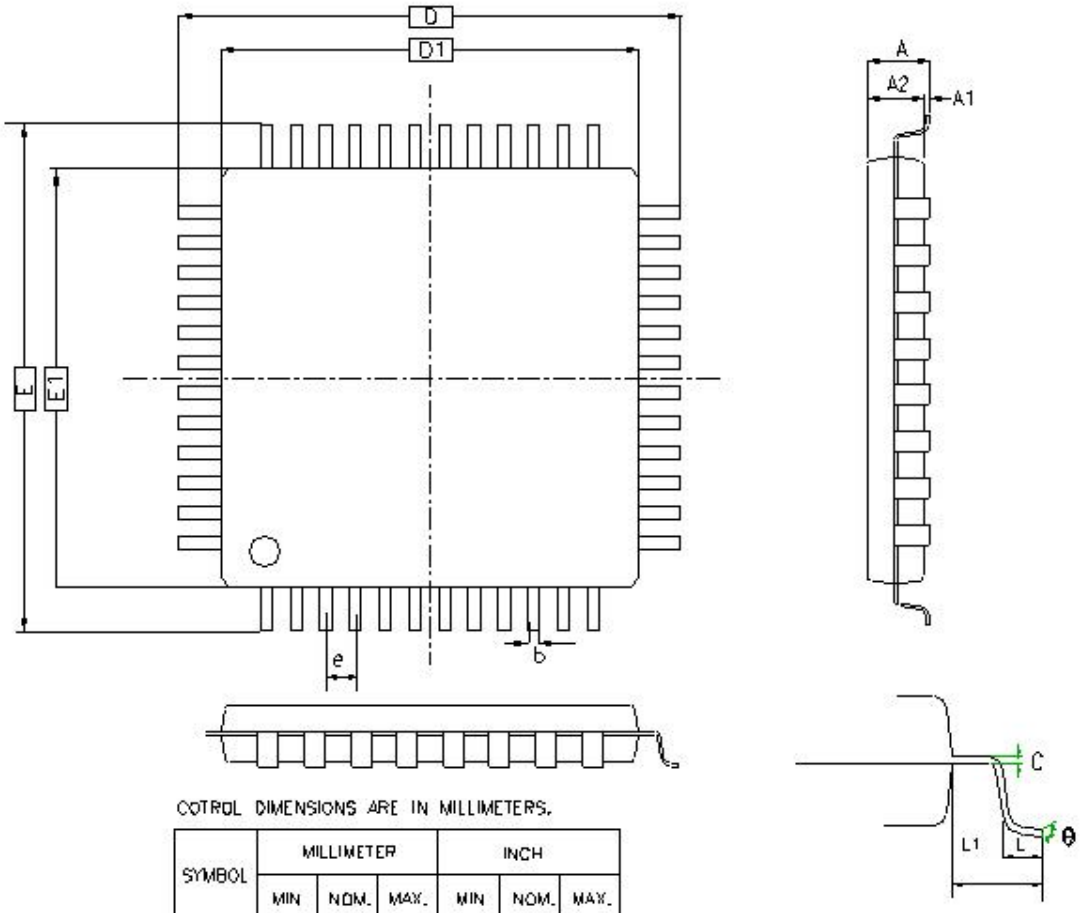
7 PACKAGE DIMENSIONS

7.1 64L LQFP (7x7x1.4mm footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

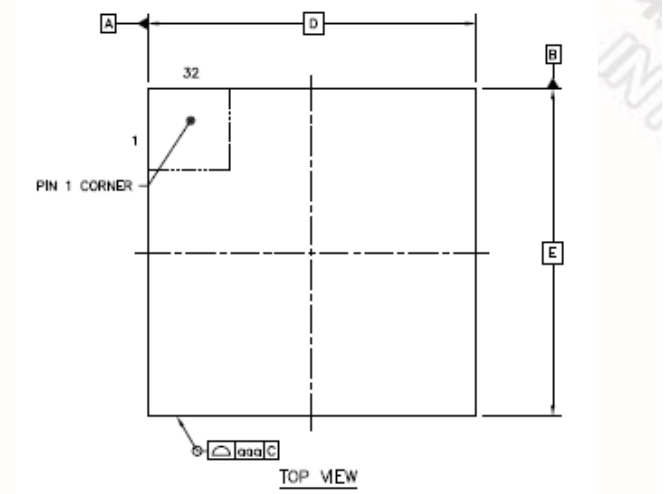
7.2 48L LQFP (7x7x1.4mm footprint 2.0mm)

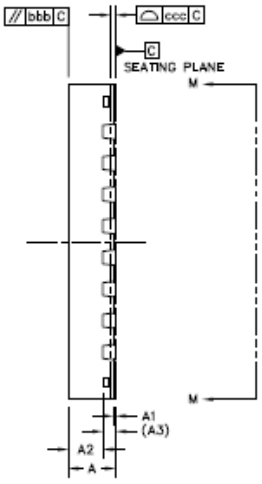


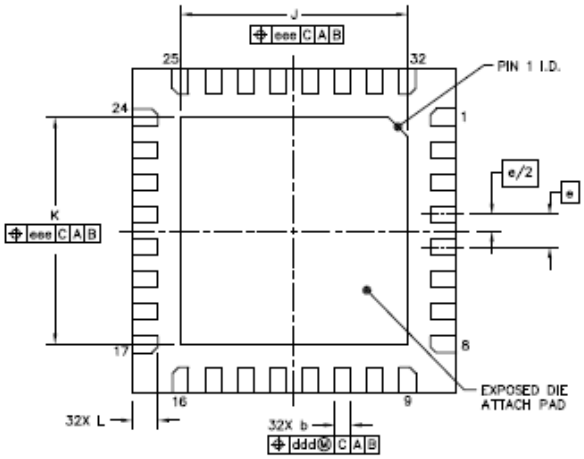
CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN	NOM.	MAX.	MIN	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.280
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.0035	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

7.3 33L QFN (5x5x0.8mm)







BOTTOM VIEW
VIEW M–M

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

8 REVISION HISTORY

VERSION	DATE	PAGE/ CHAP.	DESCRIPTION
V1.00	Nov. 15, 2010	-	Preliminary version initial issued
V1.01	Dec. 7, 2010	Chap. 3	Corrected the Selection Guide Table for QFN33.
V1.02	Jan. 13, 2011	Chap. 5 Chap. 7	1. Corrected the Watchdog Timer Clock Source Selection 2. Corrected the Electrical Characteristics.
V1.03	March 14, 2011	Chap. 3 Chap. 7 Chap. 8	1. Added the LQFP 64-pin part number for 7x7x1.4mm package. (NUC122SD2AN, NUC122SC1AN) 2. Corrected the LQFP 64-pin Pin Diagram. 3. Updated DC and AC Electrical Characteristics and added the SPI Dynamic Characteristics. 4. Updated LQFN 48-pin package dimensions.
V1.04	March 31, 2011	Chap. 2 Chap. 3 Chap. 4 Chap. 5 Chap. 8	1. Removed the LQFP 64-pin part number for 10x10x1.4mm package. 2. Replaced “12 MHz” with “4~24 MHz” in some contents and block diagrams.
V1.05	Apr.29 , 2011	Chap. 1 Chap. 2 Chap. 3 Chap. 5 Chap. 7	1. Updated the table of specification of LDO and Power Management. 2. Removed the LIN function from UART controller. 3. Corrected the “PWM_CRLx/PWM_CFLx(x=0~3)” to “CRLRx/CFLRx(x=0~3)” in the Overview of PWM Generator and Capture Timer chapter. 4. Corrected the “1xx” to “111” in System Clock and SysTick Clock Control Block Diagram. 5. Added the Clock Generator Global View Diagram. 6. Corrected the “RX0/1” and “TX0/1” to “RXD0/1” and “TXD0/1” in Pin Configuration and Pin Description.
V1.06	May 30, 2011	Chap. 3 All	1. Corrected the Pin Description of pins 17 and 18 for LQFP 48-pin. 2. Corrected the typo of Year on the Footer.
V1.07	June 8, 2011	Chap. 2 Chap. 7	1. Corrected the trimmed condition for the internal 22.1184 MHz high speed oscillator in the “Clock Control” item of Feature list. 2. Corrected the specification of the “Internal 22.1184 MHz High Speed Oscillator”.
V1.08	June 21, 2011	Chap. 2	1. Added the condition and corrected the speed of SPI in Master/Slave mode in the “SPI” item of Feature list.
V1.09	May 16, 2014	Chap. 3 Chap. 8	1. Added the PF.2 and PF.3 function on PS2DAT and PS2CLK in Pin Diagram and Pin Description. 2. Corrected QFN33 package dimension.
V1.10	Dec. 22, 2014	Chap. 5	1. Corrected the 5.9.2 Features of SPI. 2. Rearranged the chapter 5 session sequence.