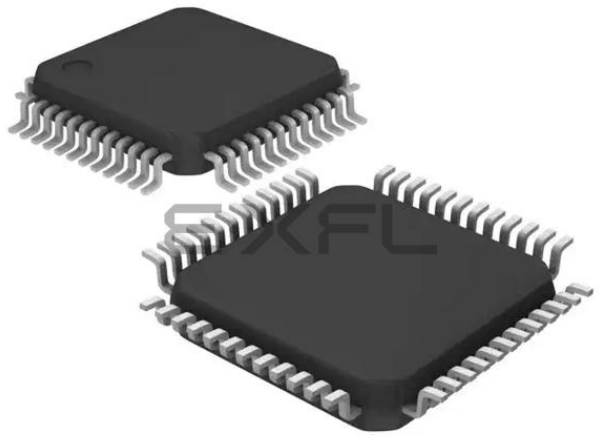

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PS2, PWM, WDT
Number of I/O	30
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc122ld2an

1 GENERAL DESCRIPTION

The NuMicro™ NUC122 series are 32-bit microcontrollers with Cortex®-M0 core runs up to 60 MHz, up to 32K/64K-byte embedded flash, 4K/8K-byte embedded SRAM, and 4K-byte loader ROM for the In System Program (ISP) function. It also integrates Timers, Watchdog Timer, RTC, UART, SPI, I^2C, PWM Timer, GPIO, USB 2.0 Full Speed Device, Low Voltage Reset Controller and Brownout Detector.

Product Line	UART	SPI	I^2C	USB	PS/2
NUC122	Y	Y	Y	Y	Y

Table 1-1 Connectivity Supported Table

- I^2C
  - One set of I^2C device
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow versatile rate control
  - I^2C-bus controller supports multiple address recognition (four slave address with mask option)
- USB 2.0 Full-Speed Device
  - One set of USB 2.0 FS Device 12Mbps
  - On-chip USB Transceiver
  - Provide 1 interrupt source with 4 interrupt events
  - Support Control, Bulk In/Out, Interrupt and Isochronous transfers
  - Auto suspend function when no bus signaling for 3 ms
  - Provide 6 programmable endpoints
  - Include 512 bytes internal SRAM as USB buffer
  - Provide remote wake-up capability
- Brownout Detector
  - With 4 levels: 4.5 V/3.8 V/2.7 V/2.2 V
  - Support Brownout Interrupt and Reset options
- One built-in LDO
- Low Voltage Reset
- Operating Temperature: -40 ℃ ~ 85 ℃
- Packages:
  - All Green package (RoHS)
  - LQFP 64-pin (7mmX7mm)
  - LQFP 48-pin
  - QFN 33-pin

3.2.2 NuMicro™ NUC122 LQFP 48-pin

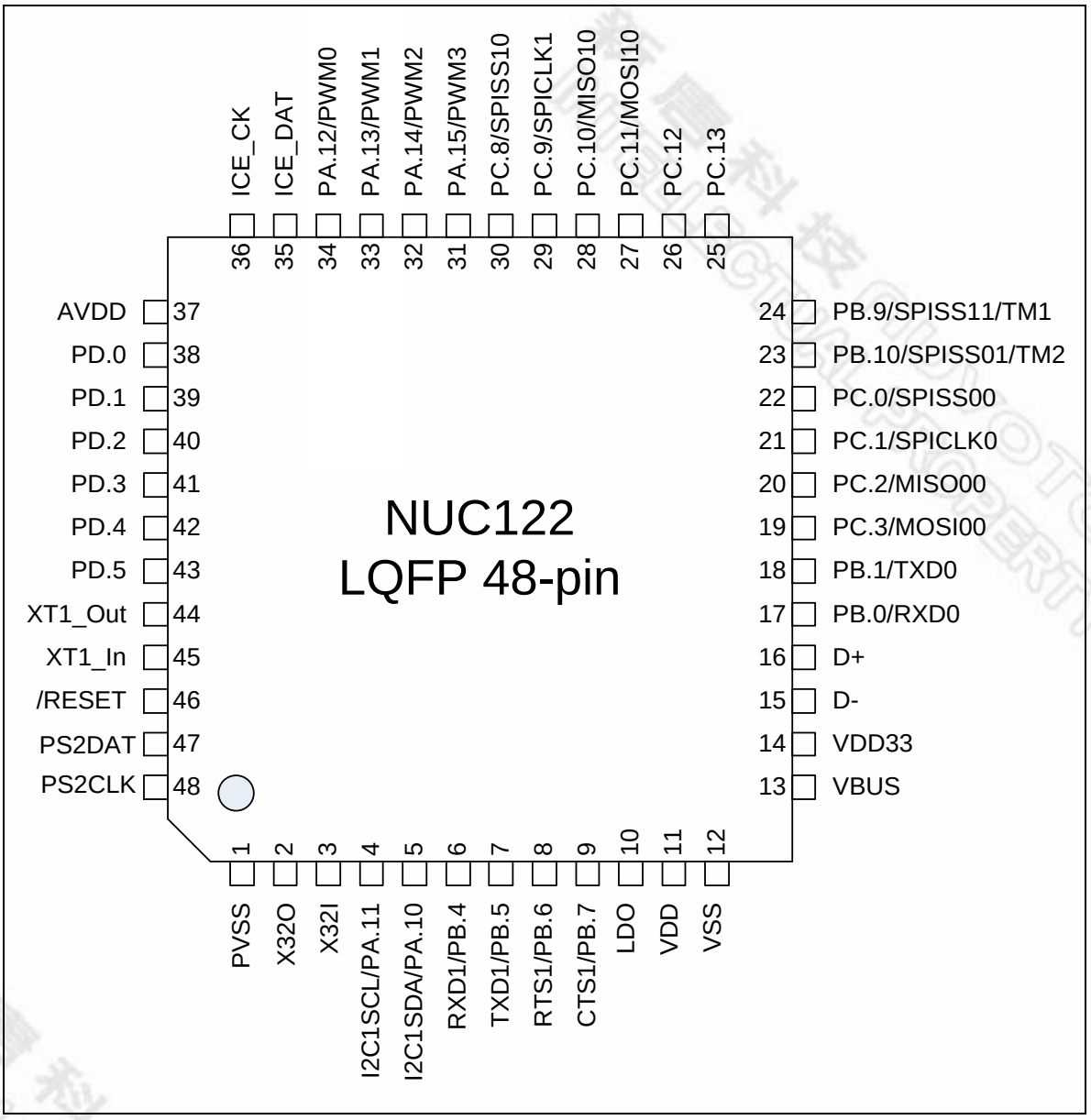


Figure 3-2 NuMicro™ NUC122 LQFP 48-pin Pin Diagram

Pin No.			Pin Name	Pin Type	Description
LQFP 64	LQFP 48	QFN 33			
36	27	19	PC.11	I/O	General purpose input/output digital pin
			MOSI10	O	MOSI10: SPI1 MOSI (Master Out, Slave In) pin
37	28	20	PC.10	I/O	General purpose input/output digital pin
			MISO10	I	MISO10: SPI1 MISO (Master In, Slave Out) pin
38			VDD	P	Power supply for I/O ports
39	29	21	PC.9	I/O	General purpose input/output digital pin
			SPICLK1	I/O	SPICLK1: SPI1 serial clock pin
40	30	22	PC.8	I/O	General purpose input/output digital pin
			SPISS10	I/O	SPISS10: SPI1 slave select pin
41	31		PA.15	I/O	General purpose input/output digital pin
			PWM3	O	PWM3: PWM output pin
42			VSS	P	Ground
43	32		PA.14	I/O	General purpose input/output digital pin
			PWM2	O	PWM2: PWM output pin
44	33		PA.13	I/O	General purpose input/output digital pin
			PWM1	O	PWM1: PWM output pin
45	34		PA.12	I/O	General purpose input/output digital pin
			PWM0	O	PWM0: PWM output pin
46	35	23	ICE_DAT	I/O	Serial Wired Debugger Data pin
47	36	24	ICE_CK	I	Serial Wired Debugger Clock pin
48	37	25	AVDD	AP	Power supply for internal analog circuit
49	38		PD.0	I/O	General purpose input/output digital pin
50	39	26	PD.1	I/O	General purpose input/output digital pin
			SPISS01	I/O	SPISS01: SPI0 2nd slave select pin (for QFN33 only)
51	40	27	PD.2	I/O	General purpose input/output digital pin
52	41	28	PD.3	I/O	General purpose input/output digital pin
53	42		PD.4	I/O	General purpose input/output digital pin
54	43		PD.5	I/O	General purpose input/output digital pin
55			PB.15	I/O	General purpose input/output digital pin

Pin No.			Pin Name	Pin Type	Description
LQFP 64	LQFP 48	QFN 33			
			/INT1	**I**	/INT1: External interrupt 1 input pin
56	44	29	XT1_OUT	**O**	Crystal output pin
57	45	30	XT1_IN	**I**	Crystal input pin
58	46	31	/RESET	**I**	External reset input: Low active, set this pin low reset chip to initial state. With internal pull-up.
59		33	VSS	**P**	Ground
60			VDD	**P**	Power supply for I/O ports
61	47		PS2DAT	**I/O**	PS/2 data pin
62	48		PS2CLK	**I/O**	PS/2 clock pin
63	1	32	PVSS	**P**	PLL Ground
64			PB.8	**I/O**	General purpose input/output digital pin
			TM0	**O**	TM0: Timer0 external counter input

Note: Pin Type I=Digital Input, O=Digital Output; AI=Analog Input; P=Power Pin; AP=Analog Power

- Debug support
  - Four hardware breakpoints.
  - Two watchpoints.
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling.
  - Single step and vector catch capabilities.
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory.
  - Single 32-bit slave port that supports the DAP (Debug Access Port).

5.3.2 Clock Generator

The clock generator consists of 5 clock sources which are listed as below:

- One external 32.768 KHz low speed crystal
- One external 4~24 MHz high speed crystal
- One programmable PLL FOUT (PLL source consists of external 4~24 MHz high speed crystal and internal 22.1184 MHz high speed oscillator)
- One internal 22.1184 MHz high speed oscillator
- One internal 10 KHz low speed oscillator

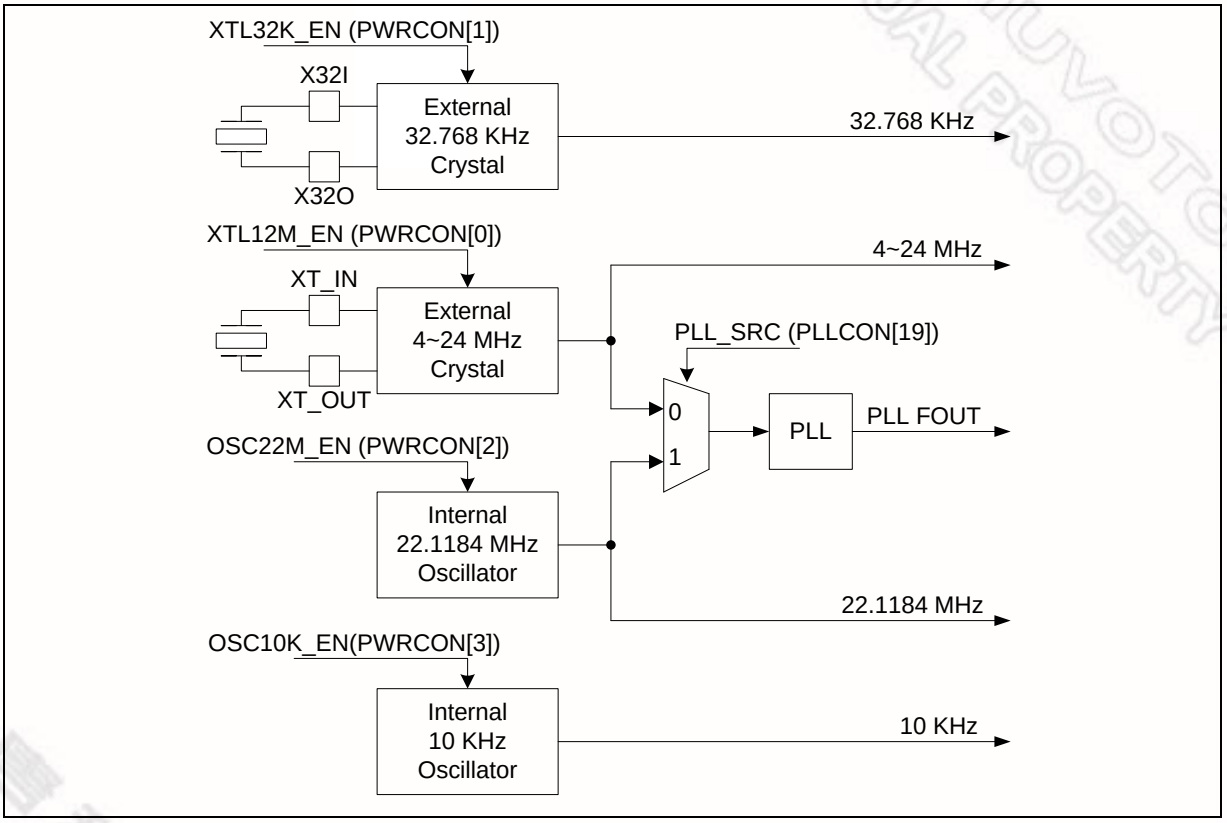


Figure 5-4 Clock Generator Block Diagram

5.3.4 Peripherals Clock

The peripherals clock had different clock source switch setting which depends on the different peripheral.

5.3.5 Power Down Mode Clock

When chip enters into power down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clock are still active in power down mode.

These clocks which still keep activity that are listed as below:

- Clock Generator
  - Internal 10 KHz low speed oscillator clock
  - External 32.768 KHz low speed crystal clock
- Peripherals Clock (When WDT adopts 10 KHz low speed as clock source and RTC adopts 32.768 KHz low speed as clock source)

5.9 Real Time Clock (RTC)

5.9.1 Overview

Real Time Clock (RTC) controller provides user the real time and calendar message. The clock source of RTC is from an external 32.768 KHz low speed crystal connected at pins X32I and X32O (reference to pin descriptions) or from an external 32.768 KHz low speed oscillator output fed at pin X32I. The RTC controller provides the time message (second, minute, hour) in Time Loading Register (TLR) as well as calendar message (day, month, year) in Calendar Loading Register (CLR). The data message is expressed in BCD format. It also offers alarm function that user can preset the alarm time in Time Alarm Register (TAR) and alarm calendar in Calendar Alarm Register (CAR).

The RTC controller supports periodic Time Tick and Alarm Match interrupts. The periodic interrupt has 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second which are selected by TTR (TTR[2:0]). When RTC counter in TLR and CLR is equal to alarm setting time registers TAR and CAR, the alarm interrupt flag (RIIR.AIF) is set and the alarm interrupt is requested if the alarm interrupt is enabled (RIER.AIER=1). Both RTC Time Tick and Alarm Match can cause chip be woken-up from power down mode if wake-up function is enabled (TWKE (TTR[3])=1).

5.9.2 Features

- There is a time counter (second, minute, hour) and calendar counter (day, month, year) for user to check the time
- Alarm register (second, minute, hour, day, month, year)
- 12-hour or 24-hour mode is selectable
- Leap year compensation automatically
- Day of week counter
- Frequency compensate register (FCR)
- All time and calendar message is expressed in BCD code
- Support periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Support RTC Time Tick and Alarm Match interrupt
- Support wake-up chip from power down mode

5.10 UART Interface Controller (UART)

NuMicro™ NUC122 provides two channels of Universal Asynchronous Receiver/Transmitters (UART0/1). Both of UART0 and UART1 perform Normal Speed UART, besides, UART0 and UART1 also support flow control function.

5.10.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART0/1) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function and RS-485 mode functions. Each UART channel supports seven types of interrupts including transmitter FIFO empty interrupt (INT_THRE), receiver threshold level reaching interrupt (INT_RDA), line status interrupt (parity error or framing error or break interrupt) (INT_RLS), receiver buffer time-out interrupt (INT_TOUT), MODEM/Wake-Up status interrupt (INT_MODEM), Buffer error interrupt (INT_BUF_ERR). Interrupt number 13 (vector number is 29) supports UART0/1 interrupt. Refer to Nested Vectored Interrupt Controller chapter for System Interrupt Map.

The UART0/1 are equipped 14-byte transmitter FIFO (TX_FIFO) and 14-byte receiver FIFO (RX_FIFO). The CPU can read the status of the UART at any time during the operation. The reported status information includes the type and condition of the transfer operations being performed by the UART, as well as 4 error conditions (parity error, framing error, break interrupt and buffer error) probably occur while receiving data. The UART includes a programmable baud rate generator that is capable of dividing clock input by divisors to produce the serial clock that transmitter and receiver need. The baud rate equation is Baud Rate = UART_CLK / M * [BRD + 2], where M and BRD are defined in Baud Rate Divider Register (UA_BAUD). Below table lists the equations in the various conditions and the UART baud rate setting table.

Mode	DIV_X_EN	DIV_X_ONE	Divider X	BRD	Baud rate equation
0	0	0	B	A	UART_CLK / [16 * (A+2)]
1	1	0	B	A	UART_CLK / [(B+1) * (A+2)] , B must >= 8
2	1	1	Don't care	A	UART_CLK / (A+2), A must >=3

Table 5-5 UART Baud Rate Equation

System clock = 22.1184 MHz high speed			
Baud rate	Mode0	Mode1	Mode2
921600	x	A=0,B=11	A=22
460800	A=1	A=1,B=15 A=2,B=11	A=46
230400	A=4	A=4,B=15 A=6,B=11	A=94
115200	A=10	A=10,B=15 A=14,B=11	A=190
57600	A=22	A=22,B=15 A=30,B=11	A=382

38400	A=34	A=62,B=8 A=46,B=11 A=34,B=15	A=574
19200	A=70	A=126,B=8 A=94,B=11 A=70,B=15	A=1150
9600	A=142	A=254,B=8 A=190,B=11 A=142,B=15	A=2302
4800	A=286	A=510,B=8 A=382,B=11 A=286,B=15	A=4606

Table 5-6 UART Baud Rate Setting Table

The UART0/1 controllers support auto-flow control function that uses two low-level signals, /CTS (clear-to-send) and /RTS (request-to-send), to control the flow of data transfer between the UART and external devices (ex: Modem). When auto-flow is enabled, the UART is not allowed to receive data until the UART asserts /RTS to external device. When the number of bytes in the RX FIFO equals the value of RTS_TRI_LEV (UA_FCR [19:16]), the /RTS is de-asserted. The UART sends data out when UART controller detects /CTS is asserted from external device. If a valid asserted /CTS is not detected the UART controller will not send data out.

The UART controllers also provides Serial IrDA (SIR, Serial Infrared) function (User must set IrDA_EN (UA_FUN_SEL [1]) to enable IrDA function). The SIR specification defines a short-range infrared asynchronous serial transmission mode with one start bit, 8 data bits, and 1 stop bit. The maximum data rate is 115.2 Kbps (half duplex). The IrDA SIR block contains an IrDA SIR Protocol encoder/decoder. The IrDA SIR protocol is half-duplex only. So it cannot transmit and receive data at the same time. The IrDA SIR physical layer specifies a minimum 10 ms transfer delay between transmission and reception. This delay feature must be implemented by software.

For NuMicro™ NUC122, another alternate function of UART controllers is RS-485 9-bit mode function, and direction control provided by RTS pin or can program GPIO (PB.2 for RTS0 and PB.6 for RTS1) to implement the function by software. The RS-485 mode is selected by setting the UA_FUN_SEL register to select RS-485 function. The RS-485 driver control is implemented using the RTS control signal from an asynchronous serial port to enable the RS-485 driver. In RS-485 mode, many characteristics of the RX and TX are same as UART.

5.12 I²C Serial Interface Controller (Master/Slave) (I²C)

5.12.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8 bits long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the following figure for more detail I²C BUS Timing.

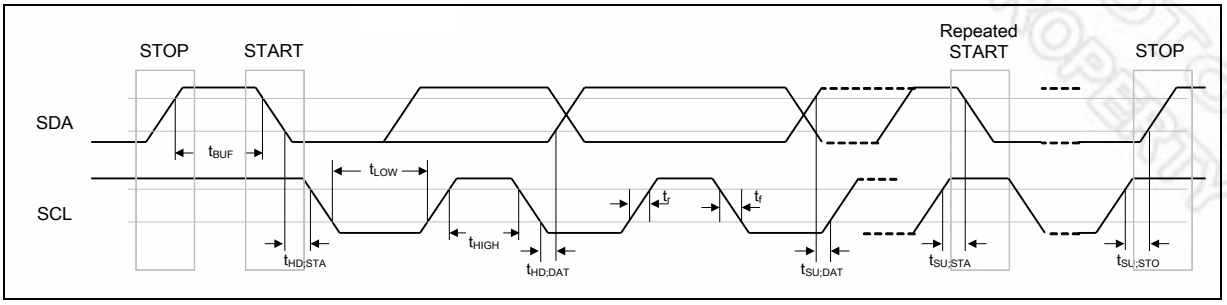


Figure 5-11 I²C Bus Timing

The device's on-chip I²C logic provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. To enable this port, the bit ENS1 in I2CON should be set to '1'. The I²C H/W interfaces to the I²C bus via two pins: SDA (PA10, serial data line) and SCL (PA11, serial clock line). Pull up resistor is needed for Pin PA10 and PA11 for I²C operation as these are open drain pins. When the I/O pins are used as I²C port, user must set the pins function to I²C in advance.

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus are:

- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Built-in a 14-bit time-out counter will request the I²C interrupt if the I²C bus hangs up and timer-out counter overflows.

5.13 Serial Peripheral Interface (SPI)

5.13.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol which operates in full duplex mode. Devices communicate in master/slave mode with 4-wire bi-direction interface. The NuMicro™ NUC122 contains up to two sets of SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each set of SPI controller can be set as a master that can drive up to 2 external peripheral slave devices; it also can be configured as a slave device controlled by an off-chip master device.

This controller also supports a variable serial clock for special application.

5.13.2 Features

- Up to two sets of SPI controller for NuMicro™ NUC122
- Support master or slave mode operation
- Support 1-bit transfer mode
- Configurable bit length up to 32 bits of a transfer word and configurable word numbers up to 2 of a transaction, so the maximum bit length is 64 bits for each data transfer
- Provide burst mode operation, transmit/receive can be transferred up to two times word transaction in one transfer
- Support MSB or LSB first transfer
- 2 device/slave select lines in master mode, but 1 device/slave select line in slave mode
- Support byte reorder in data register
- Support byte or word suspend mode
- Variable output serial clock frequency in master mode
- Support two programmable serial clock frequencies in master mode

6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into VDD		-	120	mA
Maximum Current out of VSS			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Sink Current PA, PB, PC, PD(Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	17	20	mA	V_{DD} = 4.5 V, V_S = 0.45 V
	I_{SK1}	7	10	13	mA	V_{DD} = 2.7 V, V_S = 0.45 V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5 V, V_S = 0.45 V
Brownout voltage with BOV_VL [1:0] =00b	$V_{BO2.2}$	2.1	2.2	2.3	V	
Brownout voltage with BOV_VL [1:0] =01b	$V_{BO2.7}$	2.6	2.7	2.8	V	
Brownout voltage with BOV_VL [1:0] =10b	$V_{BO3.8}$	3.6	3.75	3.9	V	
Brownout voltage with BOV_VL [1:0] =11b	$V_{BO4.5}$	4.2	4.4	4.6	V	
Hysteresis range of BOD voltage	V_{BH}	30	-	150	mV	V_{DD} = 2.5 V ~ 5.5 V

Note:

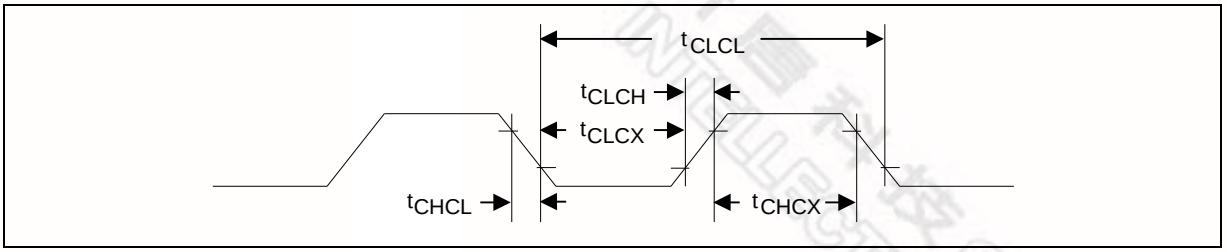
1. /RESET pin is a Schmitt trigger input.

2. Crystal Input is a CMOS input.

3. Pins of PA, PB, PC and PD can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5 V, the transition current reaches its maximum value when V_{IN} approximates to 2 V.

6.3 AC Electrical Characteristics

6.3.1 External 4~24 MHz High Speed Crystal AC Electrical Characteristics



Note: Duty cycle is 50 %.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		20	-	-	nS
t_{CLCX}	Clock Low Time		20	-	-	nS
t_{CLCH}	Clock Rise Time		-	-	10	nS
t_{CHCL}	Clock Fall Time		-	-	10	nS

6.3.2 External 4~24 MHz High Speed Crystal

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	℃

6.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	without	without	without

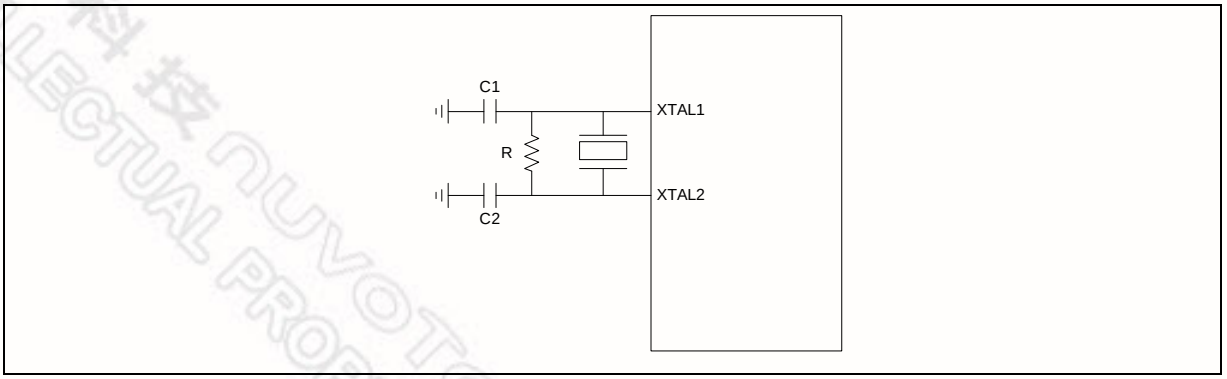


Figure 6-1 Typical Crystal Application Circuit

6.4.5 Specification of USB PHY

6.4.5.1 USB DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input high (driven)		2.0			V
V_{IL}	Input low				0.8	V
V_{DI}	Differential input sensitivity	|PADP-PADM|	0.2			V
V_{CM}	Differential common-mode range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended receiver threshold		0.8		2.0	V
	Receiver hysteresis			200		mV
V_{OL}	Output low (driven)		0		0.3	V
V_{OH}	Output high (driven)		2.8		3.6	V
V_{CRS}	Output signal cross voltage		1.3		2.0	V
R_{PU}	Pull-up resistor		1.425		1.575	kΩ
R_{PD}	Pull-down resistor		14.25		15.75	kΩ
V_{TRM}	Termination Voltage for upstream port pull up (RPU)		3.0		3.6	V
Z_{DRV}	Driver output resistance	Steady state drive*		10		Ω
C_{IN}	Transceiver capacitance	Pin to GND			20	pF

*Driver output resistance doesn't include series resistor resistance.

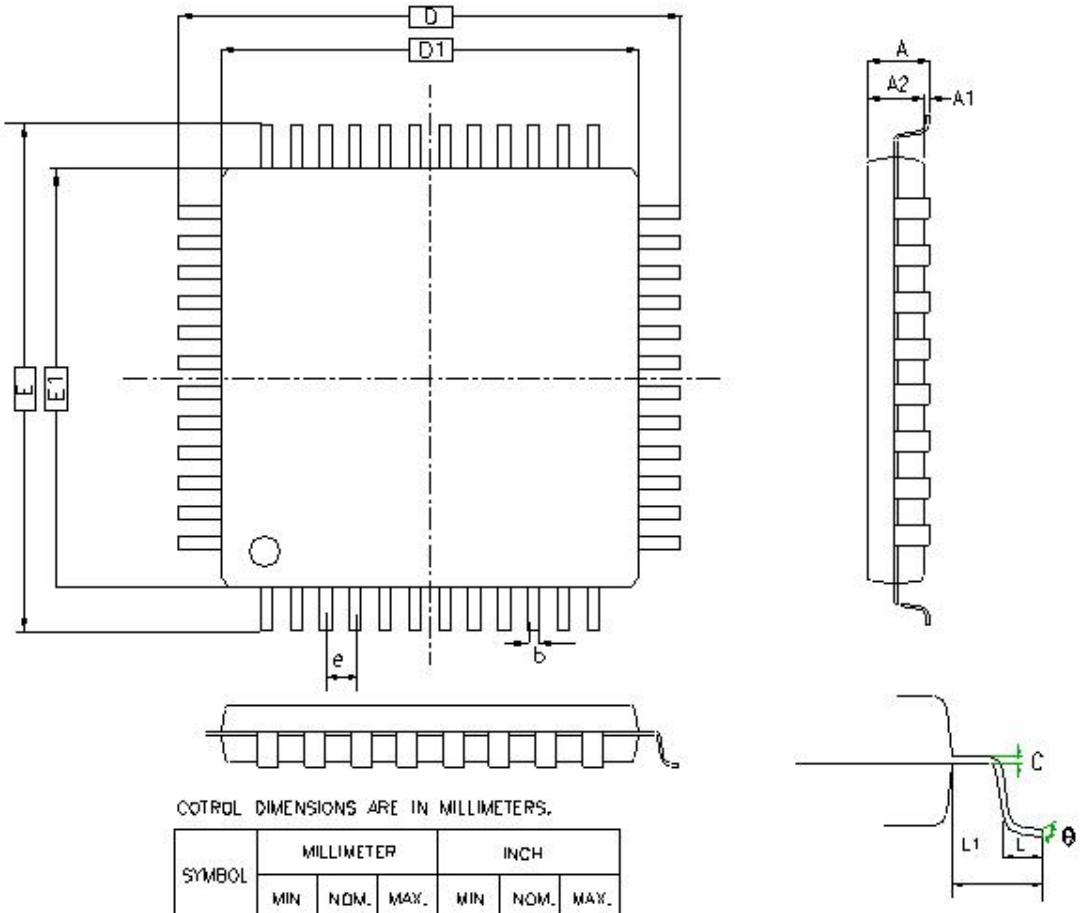
6.4.5.2 USB Full-Speed Driver Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{FR}	Rise Time	C_L=50p	4		20	ns
T_{FF}	Fall Time	C_L=50p	4		20	ns
T_{FRFF}	Rise and fall time matching	$T_{FRFF}=T_{FR}/T_{FF}$	90		111.11	%

6.4.5.3 USB Power Dissipation

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{VDDREG} (Full Speed)	V_{DDD} and V_{DDREG} Supply Current (Steady State)	Standby		50		μA
		Input mode				μA
		Output mode				μA

7.2 48L LQFP (7x7x1.4mm footprint 2.0mm)



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN	NOM.	MAX.	MIN	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.280
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.0035	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

8 REVISION HISTORY

VERSION	DATE	PAGE/ CHAP.	DESCRIPTION
V1.00	Nov. 15, 2010	-	Preliminary version initial issued
V1.01	Dec. 7, 2010	Chap. 3	Corrected the Selection Guide Table for QFN33.
V1.02	Jan. 13, 2011	Chap. 5 Chap. 7	1. Corrected the Watchdog Timer Clock Source Selection 2. Corrected the Electrical Characteristics.
V1.03	March 14, 2011	Chap. 3 Chap. 7 Chap. 8	1. Added the LQFP 64-pin part number for 7x7x1.4mm package. (NUC122SD2AN, NUC122SC1AN) 2. Corrected the LQFP 64-pin Pin Diagram. 3. Updated DC and AC Electrical Characteristics and added the SPI Dynamic Characteristics. 4. Updated LQFN 48-pin package dimensions.
V1.04	March 31, 2011	Chap. 2 Chap. 3 Chap. 4 Chap. 5 Chap. 8	1. Removed the LQFP 64-pin part number for 10x10x1.4mm package. 2. Replaced “12 MHz” with “4~24 MHz” in some contents and block diagrams.
V1.05	Apr.29 , 2011	Chap. 1 Chap. 2 Chap. 3 Chap. 5 Chap. 7	1. Updated the table of specification of LDO and Power Management. 2. Removed the LIN function from UART controller. 3. Corrected the “PWM_CRLx/PWM_CFLx(x=0~3)” to “CRLRx/CFLRx(x=0~3)” in the Overview of PWM Generator and Capture Timer chapter. 4. Corrected the “1xx” to “111” in System Clock and SysTick Clock Control Block Diagram. 5. Added the Clock Generator Global View Diagram. 6. Corrected the “RX0/1” and “TX0/1” to “RXD0/1” and “TXD0/1” in Pin Configuration and Pin Description.
V1.06	May 30, 2011	Chap. 3 All	1. Corrected the Pin Description of pins 17 and 18 for LQFP 48-pin. 2. Corrected the typo of Year on the Footer.
V1.07	June 8, 2011	Chap. 2 Chap. 7	1. Corrected the trimmed condition for the internal 22.1184 MHz high speed oscillator in the “Clock Control” item of Feature list. 2. Corrected the specification of the “Internal 22.1184 MHz High Speed Oscillator”.
V1.08	June 21, 2011	Chap. 2	1. Added the condition and corrected the speed of SPI in Master/Slave mode in the “SPI” item of Feature list.
V1.09	May 16, 2014	Chap. 3 Chap. 8	1. Added the PF.2 and PF.3 function on PS2DAT and PS2CLK in Pin Diagram and Pin Description. 2. Corrected QFN33 package dimension.
V1.10	Dec. 22, 2014	Chap. 5	1. Corrected the 5.9.2 Features of SPI. 2. Rearranged the chapter 5 session sequence.