**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 60MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LVD, POR, PS2, PWM, WDT |
| Number of I/O | 41 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc122sc1an |

## TABLE OF CONTENTS

## List of Figures

# 2 FEATURES

## 2.1 NuMicro™ NUC122 Features

- Core
  - ARM® Cortex®-M0 core runs up to 60 MHz
  - One 24-bit system timer
  - Support low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Wide operating voltage ranges from 2.5 V to 5.5 V
- Flash Memory
  - 32K/64K bytes Flash for program code
  - 4KB Flash for ISP loader
  - Support In System Program (ISP) function to update Application code
  - 512 bytes page erase for Flash
  - 4KB Data Flash
  - Support 2 wire In Circuit Program (ICP) function to update code through SWD/ICE interface
  - Support fast parallel programming mode by external programmer
- SRAM Memory
  - 4K/8K bytes embedded SRAM
- Clock Control
  - Flexible selection from different clock sources
  - Built-in 22.1184 MHz high speed OSC for system operation
    - Trimmed to ± 1 % at +25 ℃ and $V_{DD}$ = 3.3 V
    - Trimmed to ± 5 % at -40 ℃ ~ +85 ℃ and $V_{DD}$ = 2.5 V ~ 5.5 V
  - Built-in 10 KHz low speed OSC for Watchdog Timer and Wake-up operation
  - Support one PLL, up to 60 MHz, for high performance system operation
  - External 4~24 MHz high speed crystal input for USB and precise timing operation
  - External 32.768 KHz low speed crystal input for RTC function and low power system operation
- GPIO
  - Four I/O modes:
    - Quasi bi-direction
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin can be configured as interrupt source with edge/level setting
  - High driver and high sink IO mode support
- Timers
  - 4 sets of 32-bit timers with 24-bit counters and one 8-bit prescaler
  - Counter auto reload

- $I^2C$
  - One set of $I^2C$ device
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow versatile rate control
  - $I^2C$-bus controller supports multiple address recognition (four slave address with mask option)
- USB 2.0 Full-Speed Device
  - One set of USB 2.0 FS Device 12Mbps
  - On-chip USB Transceiver
  - Provide 1 interrupt source with 4 interrupt events
  - Support Control, Bulk In/Out, Interrupt and Isochronous transfers
  - Auto suspend function when no bus signaling for 3 ms
  - Provide 6 programmable endpoints
  - Include 512 bytes internal SRAM as USB buffer
  - Provide remote wake-up capability
- Brownout Detector
  - With 4 levels: 4.5 V/3.8 V/2.7 V/2.2 V
  - Support Brownout Interrupt and Reset options
- One built-in LDO
- Low Voltage Reset
- Operating Temperature: -40 ℃ ~ 85 ℃
- Packages:
  - All Green package (RoHS)
  - LQFP 64-pin (7mmX7mm)
  - LQFP 48-pin
  - QFN 33-pin

## 3.2 NuMicro™ NUC122 Pin Diagram

### 3.2.1 NuMicro™ NUC122 LQFP 64-pin

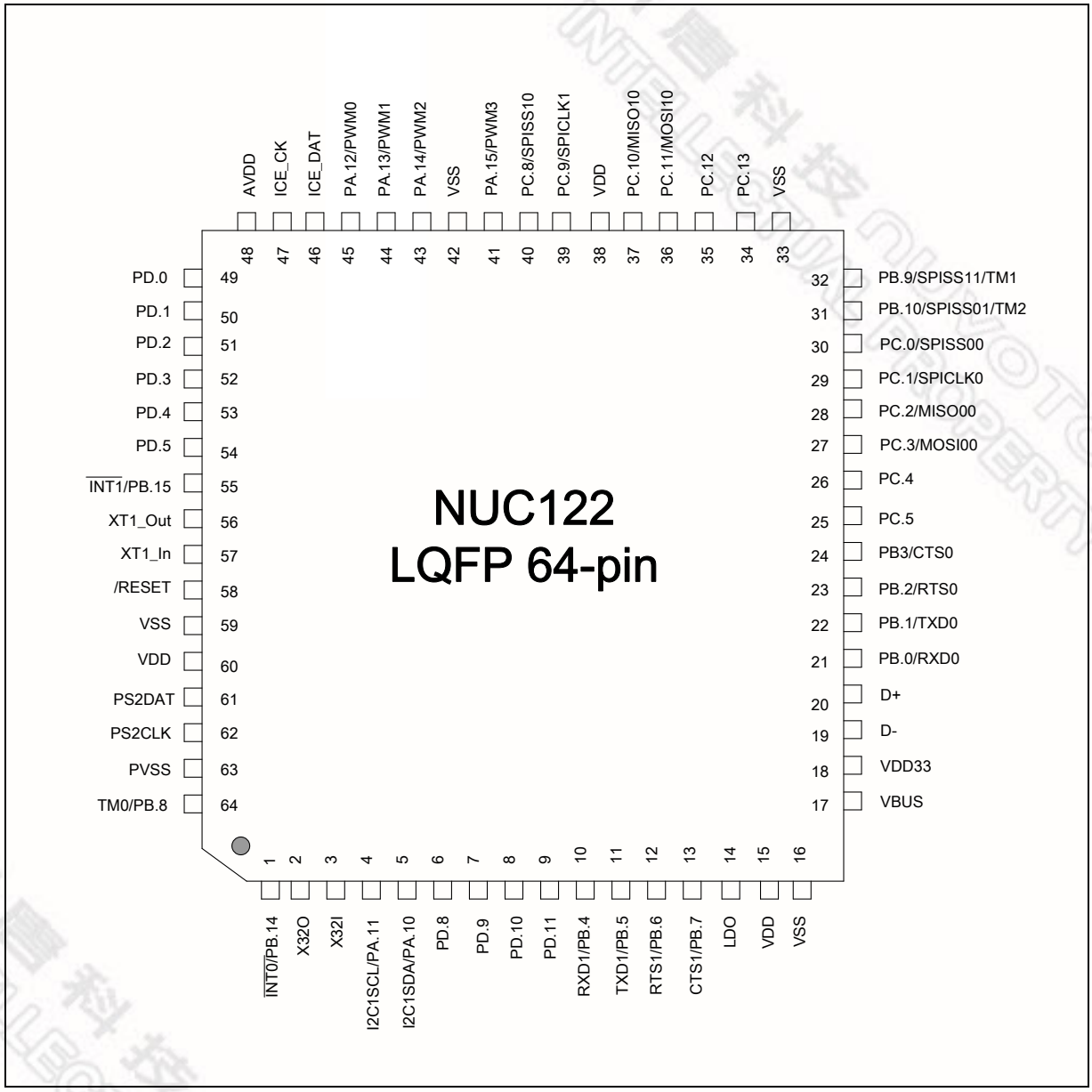


Figure 3-1 NuMicro™ NUC122 LQFP 64-pin Pin Diagram

## 3.3 NuMicro™ NUC122 Pin Description

### 3.3.1 NuMicro™ NUC122 Pin Description for LQFP64/LQFP48/QFN33

| Pin No. | | | Pin Name | Pin Type | Description |
|---|---|---|---|---|---|
| LQFP 64 | LQFP 48 | QFN 33 | | | |
| 1 | | 1 | PB.14 | I/O | General purpose input/output digital pin |
| | | | /INT0 | I | /INT0: External interrupt1 input pin |
| 2 | 2 | | X32O | O | 32.768 KHz low speed crystal output pin |
| 3 | 3 | | X32I | I | 32.768 KHz low speed crystal input pin |
| 4 | 4 | 2 | PA.11 | I/O | General purpose input/output digital pin |
| | | | I2C1SCL | I/O | I2C1SCL: $I^2C$1 clock pin |
| 5 | 5 | 3 | PA.10 | I/O | General purpose input/output digital pin |
| | | | I2C1SDA | I/O | I2C1SDA: $I^2C$1 data input/output pin |
| 6 | | | PD.8 | I/O | General purpose input/output digital pin |
| 7 | | | PD.9 | I/O | General purpose input/output digital pin |
| 8 | | | PD.10 | I/O | General purpose input/output digital pin |
| 9 | | | PD.11 | I/O | General purpose input/output digital pin |
| 10 | 6 | 4 | PB.4 | I/O | General purpose input/output digital pin |
| | | | RXD1 | I | RXD1: Data receiver input pin for UART1 |
| | | | SPISS11 | I/O | SPISS11: SPI1 slave select pin (for QFN33 only) |
| 11 | 7 | 5 | PB.5 | I/O | General purpose input/output digital pin |
| | | | TXD1 | O | TXD1: Data transmitter output pin for UART1 |
| 12 | 8 | | PB.6 | I/O | General purpose input/output digital pin |
| | | | RTS1 | O | RTS1: Request to Send output pin for UART1 |
| 13 | 9 | | PB.7 | I/O | General purpose input/output digital pin |
| | | | CTS1 | I | CTS1: Clear to Send input pin for UART1 |
| 14 | 10 | 6 | LDO | P | LDO output pin |
| 15 | 11 | 7 | VDD | P | Power supply for I/O ports and LDO source for internal PLL and digital function |
| 16 | 12 | 8 | VSS | P | Ground |
| 17 | 13 | 9 | VBUS | P | POWER SUPPLY: From USB Host or HUB. |
| 18 | 14 | 10 | VDD33 | P | Internal Power Regulator Output 3.3 V Decoupling Pin |

| Pin No. | | | Pin Name | Pin Type | Description |
|---|---|---|---|---|---|
| LQFP 64 | LQFP 48 | QFN 33 | | | |
| | | | /INT1 | **I** | /INT1: External interrupt 1 input pin |
| 56 | 44 | 29 | XT1_OUT | **O** | Crystal output pin |
| 57 | 45 | 30 | XT1_IN | **I** | Crystal input pin |
| 58 | 46 | 31 | /RESET | **I** | External reset input: Low active, set this pin low reset chip to initial state. With internal pull-up. |
| 59 | | 33 | VSS | **P** | Ground |
| 60 | | | VDD | **P** | Power supply for I/O ports |
| 61 | 47 | | PS2DAT | **I/O** | PS/2 data pin |
| 62 | 48 | | PS2CLK | **I/O** | PS/2 clock pin |
| 63 | 1 | 32 | PVSS | **P** | PLL Ground |
| 64 | | | PB.8 | **I/O** | General purpose input/output digital pin |
| | | | TM0 | **O** | TM0: Timer0 external counter input |

Note: Pin Type I=Digital Input, O=Digital Output; AI=Analog Input; P=Power Pin; AP=Analog Power

### 5.2.4 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick. SysTick provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used in several different ways, for example:

- An RTOS tick timer which fires at a programmable rate (for example 100Hz) and invokes a SysTick routine.
- A high speed alarm timer using Core clock.
- A variable rate alarm or signal timer – the duration range dependent on the reference clock used and the dynamic range of the counter.
- A simple counter. Software can use this to measure time to completion and time used.
- An internal clock source control based on missing/meeting durations. The COUNTFLAG bit-field in the control and status register can be used to determine if an action completed within a set duration, as part of a dynamic clock management control loop.

When enabled, the timer will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the documents “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

| | | | | |
|---|---|---|---|---|
| 28 | 12 | **Reserved** | Reserved | Reserved |
| 29 | 13 | **UART1_INT** | UART1 | UART1 interrupt |
| 30 | 14 | **SPI0_INT** | SPI0 | SPI0 interrupt |
| 31 | 15 | **SPI1_INT** | SPI1 | SPI1 interrupt |
| 32 | 16 | **Reserved** | Reserved | Reserved |
| 33 | 17 | **Reserved** | Reserved | Reserved |
| 34 | 18 | **Reserved** | Reserved | Reserved |
| 35 | 19 | **I2C1_INT** | $I^2C1$ | $I^2C1$ interrupt |
| 36 | 20 | **Reserved** | Reserved | Reserved |
| 37 | 21 | **Reserved** | Reserved | Reserved |
| 38 | 22 | **Reserved** | Reserved | Reserved |
| 39 | 23 | **USB_INT** | USBD | USB 2.0 FS Device interrupt |
| 40 | 24 | **PS2_INT** | PS/2 | PS/2 interrupt |
| 41 | 25 | **Reserved** | Reserved | Reserved |
| 42 | 26 | **Reserved** | Reserved | Reserved |
| 43 | 27 | **Reserved** | Reserved | Reserved |
| 44 | 28 | **PWRWU_INT** | CLKC | Power Down Wake-up interrupt |
| 45 | 29 | **Reserved** | Reserved | Reserved |
| 46 | 30 | **Reserved** | Reserved | Reserved |
| 47 | 31 | **RTC_INT** | RTC | Real time clock interrupt |

Table 5-2 System Interrupt Map

## 5.3 Clock Controller

### 5.3.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip will not enter power down mode until CPU sets the power down enable bit (PWR_DOWN_EN) and Cortex®-M0 core executes the WFI instruction. After that, chip enters power down mode and wait for wake-up interrupt source triggered to leave power down mode. In the power down mode, the clock controller turns off the external 4~24 MHz high speed crystal and internal 22.1184 MHz high speed oscillator to reduce the overall system power consumption.

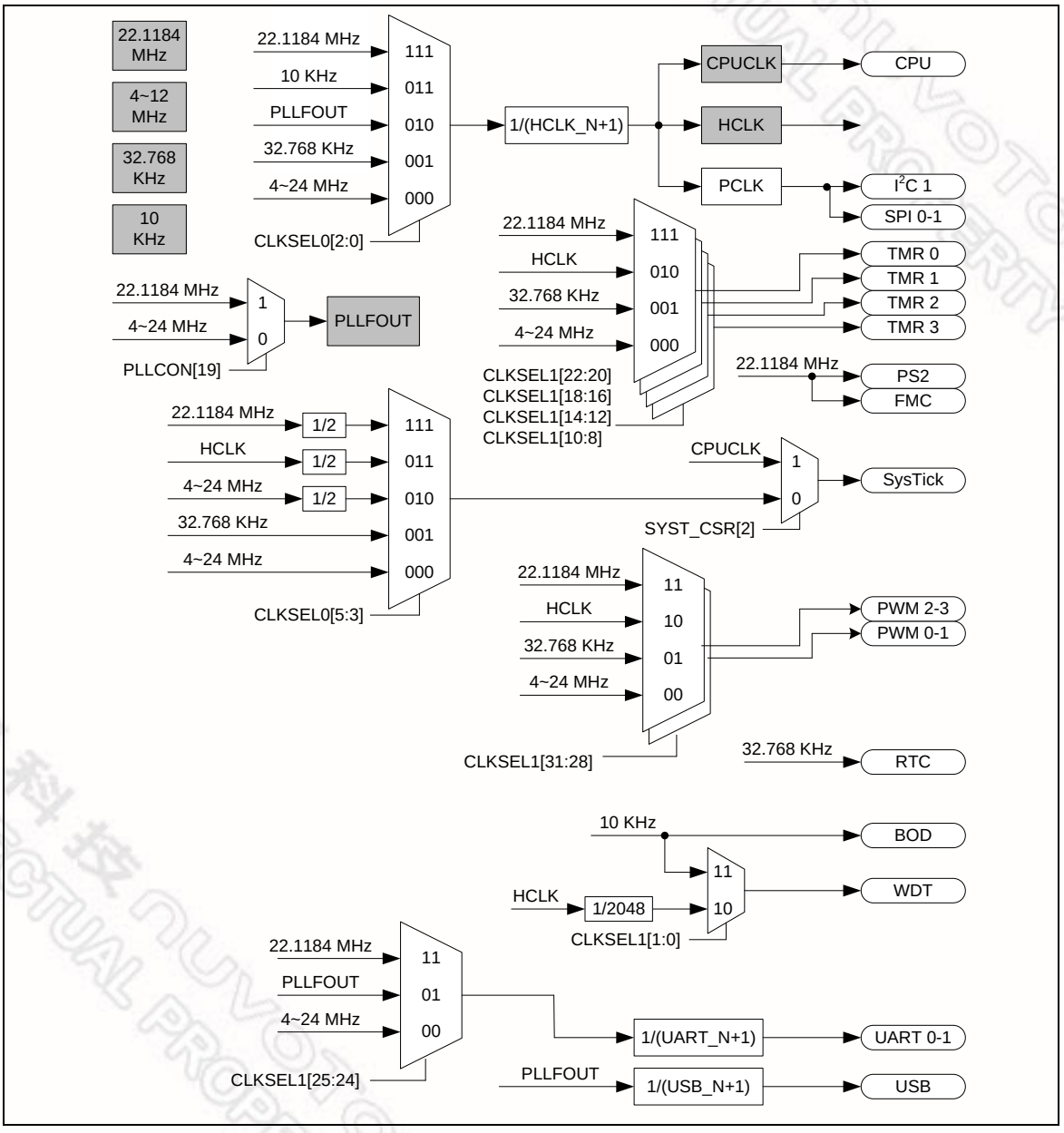


Figure 5-3 Clock Generator Global View Diagram

### 5.3.2 Clock Generator

The clock generator consists of 5 clock sources which are listed as below:

- One external 32.768 KHz low speed crystal
- One external 4~24 MHz high speed crystal
- One programmable PLL FOUT (PLL source consists of external 4~24 MHz high speed crystal and internal 22.1184 MHz high speed oscillator)
- One internal 22.1184 MHz high speed oscillator
- One internal 10 KHz low speed oscillator

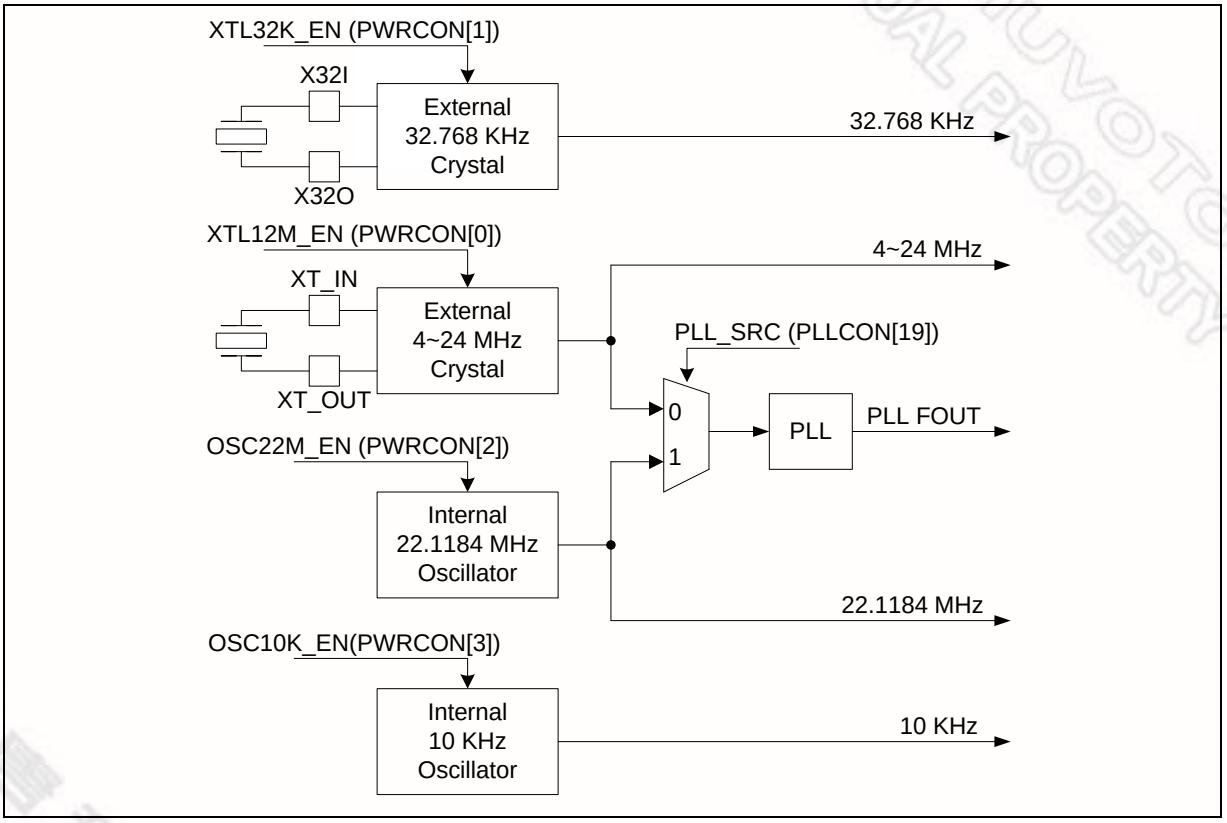


Figure 5-4 Clock Generator Block Diagram

## 5.5 General Purpose I/O (GPIO)

### 5.5.1 Overview and Features

NuMicro™ NUC122 has up to 41 General Purpose I/O pins can be shared with other function pins; it depends on the chip configuration. These 41 pins are arranged in 4 ports named with GPIOA, GPIOB, GPIOC and GPIOD. Each port equips maximum 16 pins. Each one of the 41 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as input, output, open-drain or quasi-bidirectional mode. After reset, the I/O type of all pins stay in quasi-bidirectional mode and port data register GPIOx_DOUT[15:0] resets to 0x0000_FFFF. Each I/O pin equips a very weakly individual pull-up resistor which is about 110KΩ~300KΩ for $V_{DD}$ is from 5.5 V to 2.5 V.

### 5.5.2 Function Description

*5.5.2.1 Input Mode Explanation*

**Set GPIOx_PMD** (PMDn[1:0]) to 00b the GPIOx port [n] pin is in Input mode and the I/O pin is in tri-state (high impedance) without output drive capability. **The GPIOx_PIN value reflects the status of the corresponding port pins.**

*5.5.2.2 Output Mode Explanation*

**Set GPIOx_PMD** (PMDn[1:0]) to 01b the GPIOx port [n] pin is in Output mode and the I/O pin supports digital output function with source/sink current capability. The bit value in the corresponding bit [n] of GPIOx_DOUT is driven on the pin.

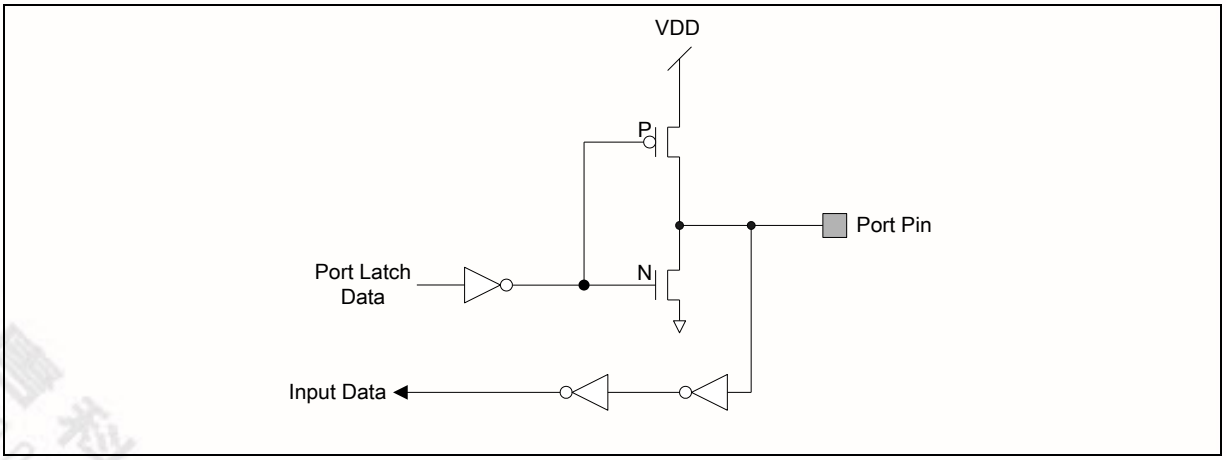


Figure 5-7 Push-Pull Output

## 5.14 USB Device Controller (USB)

### 5.14.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and support control/bulk/interrupt/isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 512 bytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. Users need to set the effective starting address of SRAM for each endpoint buffer through “buffer segmentation register (BUFSEGx)”.

There are six endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of ENDPOINT CONTROL is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status and data buffer status for each endpoint.

There are four different interrupt events in this controller. They are the wake-up function, device plug-in or plug-out event, USB events, like IN ACK, OUT ACK etc, and BUS events, like suspend and resume, etc. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USB_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USB_EPSTS) to acknowledge what kind of event occurring in this endpoint.

A software-disable function is also support for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables DRVSE0 bit (USB_DRVSE0), the USB controller will force the output of USB_DP and USB_DM to level low and its function is disabled. After disable the DRVSE0 bit, host will enumerate the USB device again.

Reference: Universal Serial Bus Specification Revision 1.1

### 5.14.2 Features

This Universal Serial Bus (USB) performs a serial interface with a single connector type for attaching all USB peripherals to the host system. Following is the feature listing of this USB.

- Compliant with USB 2.0 Full-Speed specification
- Provide 1 interrupt vector with 4 different interrupt events (WAKEUP, FLDET, USB and BUS)
- Support Control/Bulk/Interrupt/Isochronous transfer type
- Support suspend function when no bus activity existing for 3 ms
- Provide 6 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 512 bytes buffer size
- Provide remote wake-up capability

# 6 ELECTRICAL CHARACTERISTICS

## 6.1 Absolute Maximum Ratings

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| DC Power Supply | VDD–VSS | -0.3 | +7.0 | V |
| Input Voltage | VIN | VSS-0.3 | VDD+0.3 | V |
| Oscillator Frequency | $1/t_{CLCL}$ | 4 | 24 | MHz |
| Operating Temperature | TA | -40 | +85 | °C |
| Storage Temperature | TST | -55 | +150 | °C |
| Maximum Current into VDD | | - | 120 | mA |
| Maximum Current out of VSS | | | 120 | mA |
| Maximum Current sunk by a I/O pin | | | 35 | mA |
| Maximum Current sourced by a I/O pin | | | 35 | mA |
| Maximum Current sunk by total I/O pins | | | 100 | mA |
| Maximum Current sourced by total I/O pins | | | 100 | mA |

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

## 6.2 DC Electrical Characteristics

### 6.2.1 NuMicro™ NUC122 DC Electrical Characteristics

($V_{DD}$-$V_{SS}$=3.3 V, TA = 25 °C, FOSC = 60 MHz unless otherwise specified.)

| PARAMETER | SYM. | SPECIFICATION | | | | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| Operation voltage | $V_{DD}$ | 2.5 | | 5.5 | V | $V_{DD}$ =2.5 V ~ 5.5 V up to 60 MHz |
| LDO Output Voltage | $V_{LDO}$ | 1.6 | 1.8 | 2.1 | V | $V_{DD} \geqq$ 2.5 V |
| Analog Operating Voltage | $AV_{DD}$ | 0 | | $V_{DD}$ | V | |
| Operating Current Normal Run Mode @ 60 MHz | $I_{DD1}$ | | 26 | | mA | $V_{DD}$ = 5.5 V @ 60 MHz, enable all IP and PLL, XTAL=12 MHz |
| | $I_{DD2}$ | | 21 | | mA | $V_{DD}$ = 5.5 V @ 60 MHz, disable all IP and enable PLL, XTAL=12 MHz |
| | $I_{DD3}$ | | 24 | | mA | $V_{DD}$ = 3.3 V @ 60 MHz, enable all IP and PLL, XTAL=12 MHz |
| | $I_{DD4}$ | | 19 | | mA | $V_{DD}$ = 3.3 V @ 60 MHz, disable all IP and enable PLL, XTAL=12 MHz |
| Operating Current Normal Run Mode @ 12 MHz | $I_{DD5}$ | | 6.5 | | mA | $V_{DD}$ = 5.5 V @ 12MHz, enable all IP and disable PLL, XTAL=12 MHz |
| | $I_{DD6}$ | | 5 | | mA | $V_{DD}$ = 5.5 V @ 12 MHz, disable all IP and PLL, XTAL=12 MHz |
| | $I_{DD7}$ | | 4.5 | | mA | $V_{DD}$ = 3.3 V @ 12 MHz, enable all IP and disable PLL, XTAL=12 MHz |
| | $I_{DD8}$ | | 3.5 | | mA | $V_{DD}$ = 3.3 V @ 12 MHz, disable all IP and PLL, XTAL=12 MHz |
| Operating Current Normal Run Mode @ 4 MHz | $I_{DD9}$ | | 3.5 | | mA | $V_{DD}$ = 5.5 V @ 4 MHz, enable all IP and disable PLL, XTAL=4 MHz |
| | $I_{DD10}$ | | 3 | | mA | $V_{DD}$ = 5.5 V @ 4 MHz, |

| PARAMETER | SYM. | SPECIFICATION | | | | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| Sink Current PA, PB, PC, PD(Quasi-bidirectional and Push-pull Mode) | $I_{SK1}$ | 10 | 17 | 20 | mA | $V_{DD}$ = 4.5 V, $V_S$ = 0.45 V |
| | $I_{SK1}$ | 7 | 10 | 13 | mA | $V_{DD}$ = 2.7 V, $V_S$ = 0.45 V |
| | $I_{SK1}$ | 6 | 9 | 12 | mA | $V_{DD}$ = 2.5 V, $V_S$ = 0.45 V |
| Brownout voltage with BOV_VL [1:0] =00b | $V_{BO2.2}$ | 2.1 | 2.2 | 2.3 | V | |
| Brownout voltage with BOV_VL [1:0] =01b | $V_{BO2.7}$ | 2.6 | 2.7 | 2.8 | V | |
| Brownout voltage with BOV_VL [1:0] =10b | $V_{BO3.8}$ | 3.6 | 3.75 | 3.9 | V | |
| Brownout voltage with BOV_VL [1:0] =11b | $V_{BO4.5}$ | 4.2 | 4.4 | 4.6 | V | |
| Hysteresis range of BOD voltage | $V_{BH}$ | 30 | - | 150 | mV | $V_{DD}$ = 2.5 V ~ 5.5 V |

Note:

1. /RESET pin is a Schmitt trigger input.

2. Crystal Input is a CMOS input.

3. Pins of PA, PB, PC and PD can source a transition current when they are being externally driven from 1 to 0. In the condition of $V_{DD}$=5.5 V, the transition current reaches its maximum value when $V_{IN}$ approximates to 2 V.

## 6.4 Analog Characteristics

### 6.4.1 Specification of LDO & Power management

| PARAMETER | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|
| Input Voltage | 2.5 | 5 | 5.5 | V | $V_{DD}$ input voltage |
| Output Voltage | 1.6 | 1.8 | 2.1 | V | $V_{DD} \geq 2.5$ V |
| Temperature | -40 | 25 | 85 | ℃ | |
| Quiescent Current (PD=0) | - | 100 | - | μA | |
| Quiescent Current (PD=1) | - | 5 | - | μA | |
| Iload (PD=0) | - | - | 100 | mA | |
| Iload (PD=1) | - | - | 100 | μA | |
| Cbp | - | 4.7 | - | μF | Resr=1 ohm |

Note:

1. It is recommended that a 10 μF or higher capacitor and a 100 nF bypass capacitor are connected between VDD and the closest VSS pin of the device.

2. For ensuring power stability, a 4.7 μF or higher capacitor must be connected between LDO pin and the closest VSS pin of the device.

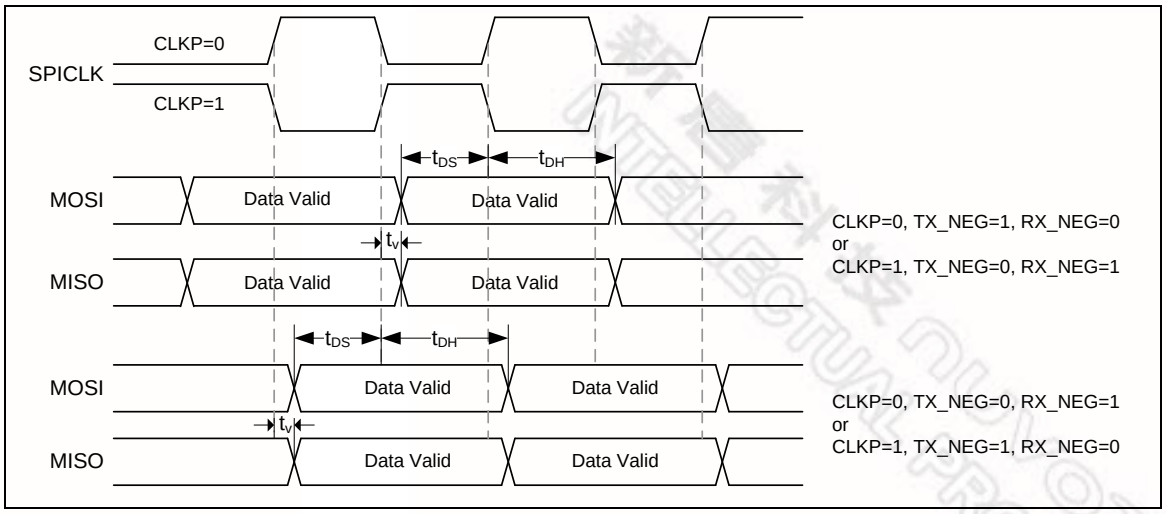


Figure 6-3 SPI Slave Mode Timing

| | | | |
|---|---|---|---|
| V1.11 | Jan. 09, 2015 | Chap. 2<br>Chap. 5 | 1. Corrected the UART FIFO to 14-byte.<br>2. Removed the GPIO PF.2 and PF.3 from Pin Diagram and Pin Description. |

## Important Notice

**Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".**

**Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.**

**All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.**