Nuvoton Technology Corporation - NUC122SD2AN Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PS2, PWM, WDT
Number of I/O	41
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc122sd2an

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1 GENERAL DESCRIPTION

The NuMicro™ NUC122 series are 32-bit microcontrollers with Cortex®-M0 core runs up to 60 MHz, up to 32K/64K-byte embedded flash, 4K/8K-byte embedded SRAM, and 4K-byte loader ROM for the In System Program (ISP) function. It also integrates Timers, Watchdog Timer, RTC, UART, SPI, I^2C, PWM Timer, GPIO, USB 2.0 Full Speed Device, Low Voltage Reset Controller and Brownout Detector.

Product Line	UART	SPI	I^2C	USB	PS/2
NUC122	Y	Y	Y	Y	Y

Table 1-1 Connectivity Supported Table

2 FEATURES

2.1 NuMicro™ NUC122 Features

- Core
  - ARM® Cortex®-M0 core runs up to 60 MHz
  - One 24-bit system timer
  - Support low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Wide operating voltage ranges from 2.5 V to 5.5 V
- Flash Memory
  - 32K/64K bytes Flash for program code
  - 4KB Flash for ISP loader
  - Support In System Program (ISP) function to update Application code
  - 512 bytes page erase for Flash
  - 4KB Data Flash
  - Support 2 wire In Circuit Program (ICP) function to update code through SWD/ICE interface
  - Support fast parallel programming mode by external programmer
- SRAM Memory
  - 4K/8K bytes embedded SRAM
- Clock Control
  - Flexible selection from different clock sources
  - Built-in 22.1184 MHz high speed OSC for system operation
    - Trimmed to ± 1 % at +25 ℃ and V_{DD} = 3.3 V
    - Trimmed to ± 5 % at -40 ℃ ~ +85 ℃ and V_{DD} = 2.5 V ~ 5.5 V
  - Built-in 10 KHz low speed OSC for Watchdog Timer and Wake-up operation
  - Support one PLL, up to 60 MHz, for high performance system operation
  - External 4~24 MHz high speed crystal input for USB and precise timing operation
  - External 32.768 KHz low speed crystal input for RTC function and low power system operation
- GPIO
  - Four I/O modes:
    - Quasi bi-direction
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin can be configured as interrupt source with edge/level setting
  - High driver and high sink IO mode support
- Timers
  - 4 sets of 32-bit timers with 24-bit counters and one 8-bit prescaler
  - Counter auto reload

- I^2C
  - One set of I^2C device
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow versatile rate control
  - I^2C-bus controller supports multiple address recognition (four slave address with mask option)
- USB 2.0 Full-Speed Device
  - One set of USB 2.0 FS Device 12Mbps
  - On-chip USB Transceiver
  - Provide 1 interrupt source with 4 interrupt events
  - Support Control, Bulk In/Out, Interrupt and Isochronous transfers
  - Auto suspend function when no bus signaling for 3 ms
  - Provide 6 programmable endpoints
  - Include 512 bytes internal SRAM as USB buffer
  - Provide remote wake-up capability
- Brownout Detector
  - With 4 levels: 4.5 V/3.8 V/2.7 V/2.2 V
  - Support Brownout Interrupt and Reset options
- One built-in LDO
- Low Voltage Reset
- Operating Temperature: -40 ℃ ~ 85 ℃
- Packages:
  - All Green package (RoHS)
  - LQFP 64-pin (7mmX7mm)
  - LQFP 48-pin
  - QFN 33-pin

3.2 NuMicro™ NUC122 Pin Diagram

3.2.1 NuMicro™ NUC122 LQFP 64-pin

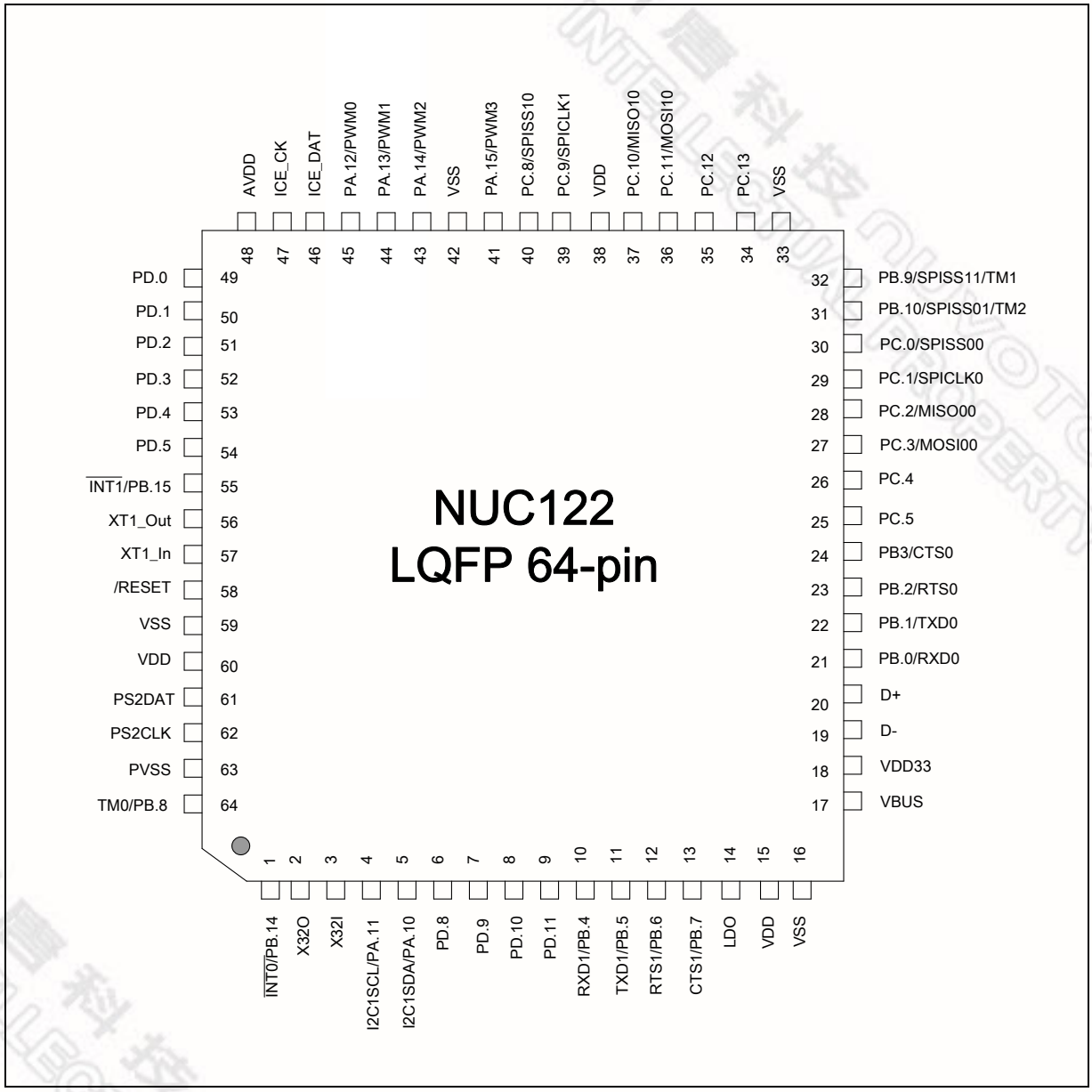


Figure 3-1 NuMicro™ NUC122 LQFP 64-pin Pin Diagram

3.2.2 NuMicro™ NUC122 LQFP 48-pin

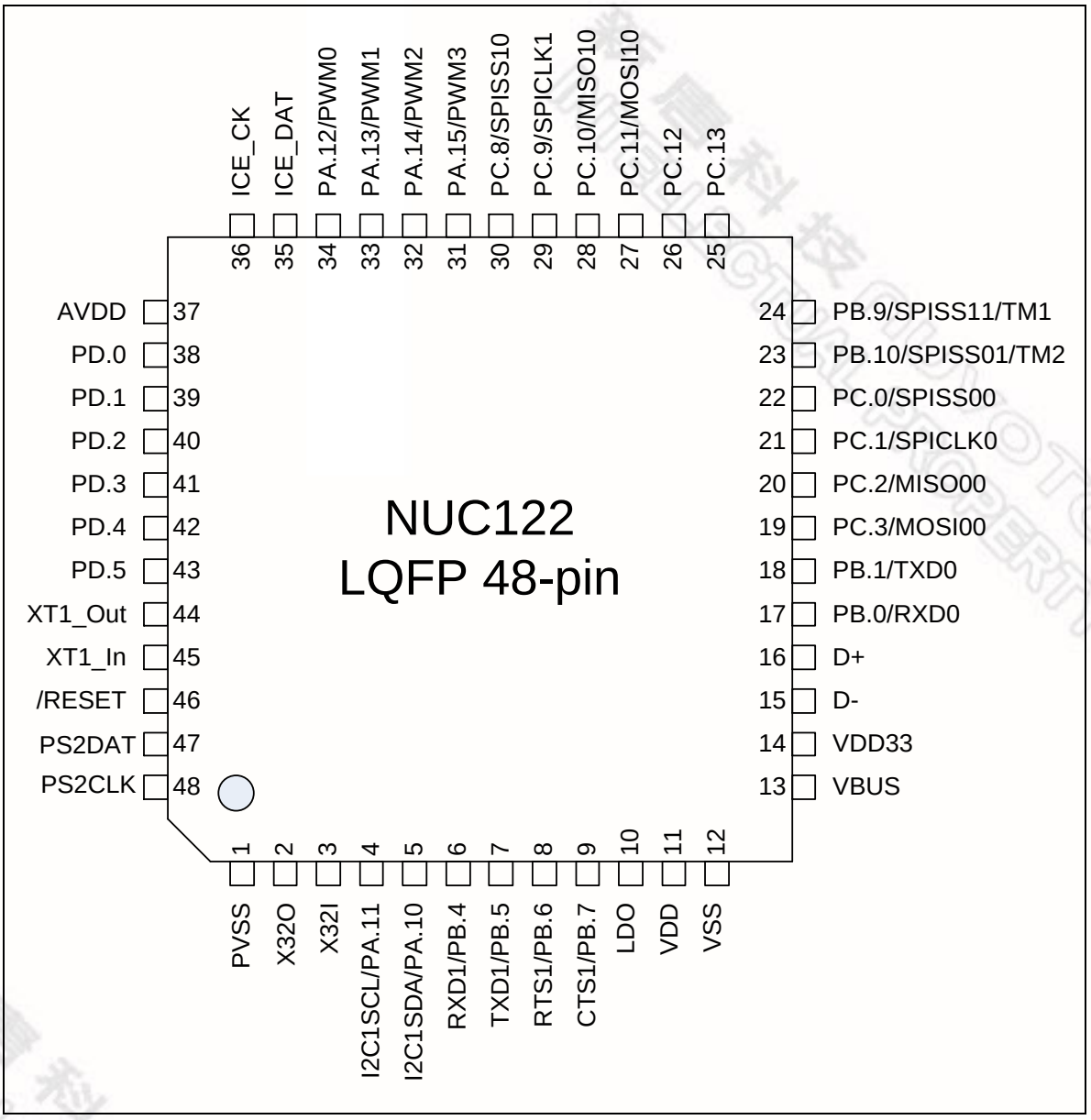


Figure 3-2 NuMicro™ NUC122 LQFP 48-pin Pin Diagram

3.2.3 NuMicro™ NUC122 QFN 33-pin

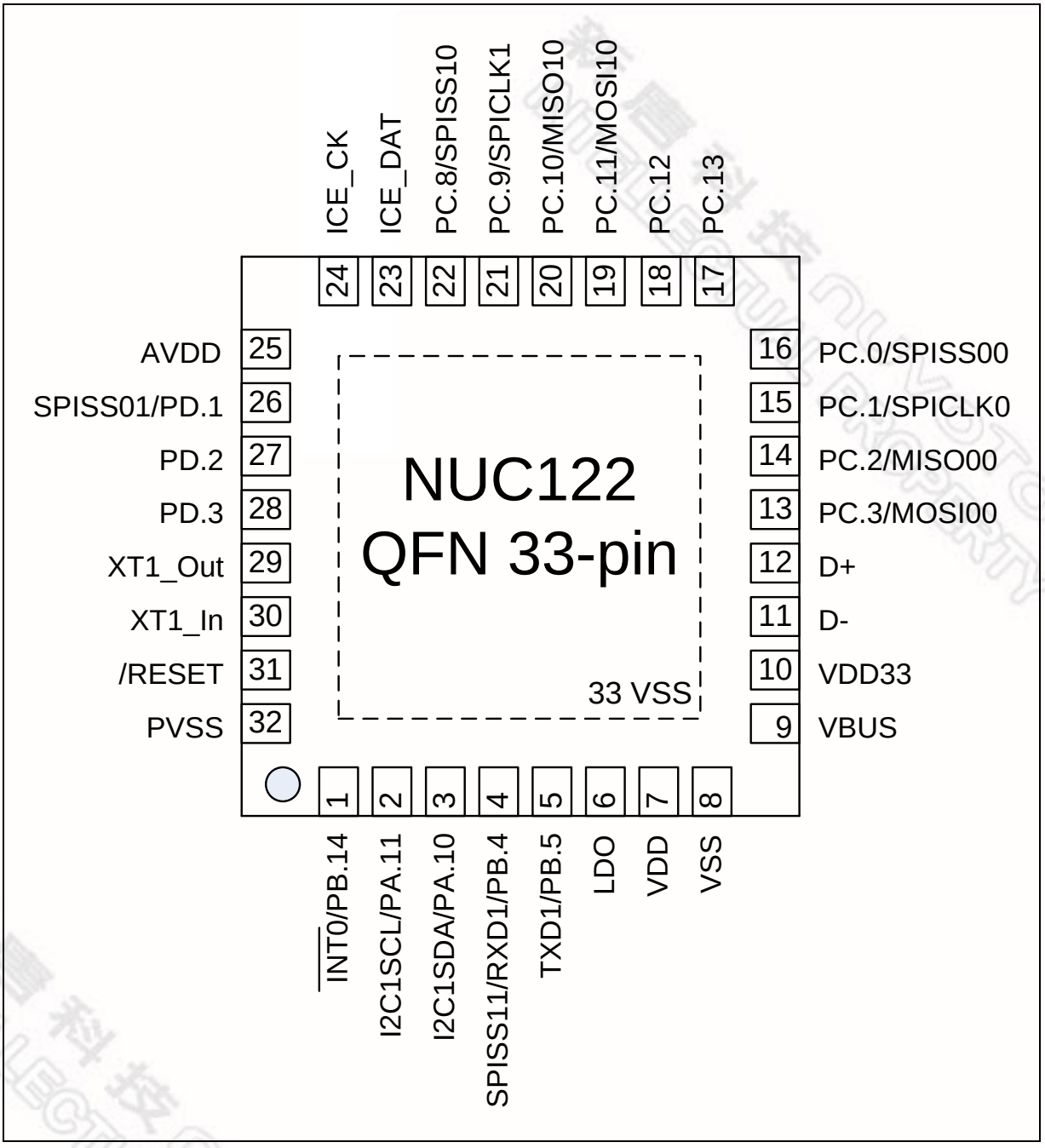


Figure 3-3 NuMicro™ NUC122 QFN 33-pin Pin Diagram

Pin No.			Pin Name	Pin Type	Description
LQFP 64	LQFP 48	QFN 33			
19	15	11	D-	**USB**	USB Differential Signal D-
20	16	12	D+	**USB**	USB Differential Signal D+
21	17		PB.0	**I/O**	General purpose input/output digital pin
			RXD0	**I**	RXD0: Data Receiver input pin for UART0
22	18		PB.1	**I/O**	General purpose input/output digital pin
			TXD0	**O**	TXD0: Data transmitter output pin for UART0
23			PB.2	**I/O**	General purpose input/output digital pin
			RTS0	**O**	RTS0: Request to Send output pin for UART0
24			PB.3	**I/O**	General purpose input/output digital pin
			CTS0	**I**	CTS0: Clear to Send input pin for UART0
25			PC.5	**I/O**	General purpose input/output digital pin
26			PC.4	**I/O**	General purpose input/output digital pin
27	19	13	PC.3	**I/O**	General purpose input/output digital pin
			MOSI00	**O**	MOSI00: SPI0 MOSI (Master Out, Slave In) pin
28	20	14	PC.2	**I/O**	General purpose input/output digital pin
			MISO00	**I**	MISO00: SPI0 MISO (Master In, Slave Out) pin
29	21	15	PC.1	**I/O**	General purpose input/output digital pin
			SPICLK0	**I/O**	SPICLK0: SPI0 serial clock pin
30	22	16	PC.0	**I/O**	General purpose input/output digital pin
			SPISS00	**I/O**	SPISS00: SPI0 slave select pin
31	23		PB.10	**I/O**	General purpose input/output digital pin
			TM2	**O**	TM2: Timer2 external counter input
			SPISS01	**I/O**	SPISS01: SPI0 2nd slave select pin
32	24		PB.9	**I/O**	General purpose input/output digital pin
			TM1	**O**	TM1: Timer1 external counter input
			SPISS11	**I/O**	SPISS11: SPI1 2nd slave select pin
33			VSS	**P**	Ground
34	25	17	PC.13	**I/O**	General purpose input/output digital pin
35	26	18	PC.12	**I/O**	General purpose input/output digital pin

5.2 System Manager

5.2.1 Overview

System management includes these following sections:

- System Resets
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

5.2.2 System Reset

The system reset can be issued by one of the below listed events. These reset event flags can be read from RSTSRC register.

- The Power-On Reset
- The low level on the /RESET pin
- Watchdog Timer Time-Out Reset
- Low Voltage Reset
- Brownout Detector Reset
- Cortex®-M0 Reset
- System Reset

Both System Reset and Power-On Reset can reset the whole chip including all peripherals. The difference between System Reset and Power-On Reset is external Crystal circuit and ISPCON.BS bit. System Reset doesn't reset external Crystal circuit and ISPCON.BS bit, but Power-On Reset does.

5.2.4 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick. SysTick provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used in several different ways, for example:

- An RTOS tick timer which fires at a programmable rate (for example 100Hz) and invokes a SysTick routine.
- A high speed alarm timer using Core clock.
- A variable rate alarm or signal timer – the duration range dependent on the reference clock used and the dynamic range of the counter.
- A simple counter. Software can use this to measure time to completion and time used.
- An internal clock source control based on missing/meeting durations. The COUNTFLAG bit-field in the control and status register can be used to determine if an action completed within a set duration, as part of a dynamic clock management control loop.

When enabled, the timer will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the documents “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

5.2.5 Nested Vectored Interrupt Controller (NVIC)

Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)". It is closely coupled to the processor kernel and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Dynamic priority changing
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When any interrupts is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the documents "ARM® Cortex®-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

5.2.5.1 Exception Model and System Interrupt Map

The following table lists the exception model supported by NuMicro™ NUC122. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0” and the lowest priority is denoted as “3”. The default priority of all the user-configurable interrupts is “0”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 5-1 Exception Model

Vector Number	Interrupt Number (Bit in Interrupt Registers)	Interrupt Name	Source IP	Interrupt description
0 ~ 15	-	-	-	System exceptions
16	0	**BOD_OUT**	Brownout	Brownout low voltage detected interrupt
17	1	**WDT_INT**	WDT	Watchdog Timer interrupt
18	2	**EINT0**	GPIO	External signal interrupt from PB.14 pin
19	3	**EINT1**	GPIO	External signal interrupt from PB.15 pin
20	4	**GPAB_INT**	GPIO	External signal interrupt from PA[15:0]/PB[13:0]
21	5	**GPCD_INT**	GPIO	External interrupt from PC[15:0]/PD[15:0]
22	6	**PWMA_INT**	PWM0~3	PWM0, PWM1, PWM2 and PWM3 interrupt
23	7	**Reserved**	Reserved	Reserved
24	8	**TMR0_INT**	TMR0	Timer 0 interrupt
25	9	**TMR1_INT**	TMR1	Timer 1 interrupt
26	10	**TMR2_INT**	TMR2	Timer 2 interrupt
27	11	**TMR3_INT**	TMR3	Timer 3 interrupt

5.5.2.3 Open-Drain Mode Explanation

Set GPIOx_PMD (PMDn[1:0]) to 10b the GPIOx port [n] pin is in Open-Drain mode and the digital output function of I/O pin supports only sink current capability, an additional pull-up resister is needed for driving high state. If the bit value in the corresponding bit [n] of GPIOx_DOUT is 0, the pin drive a "low" output on the pin. If the bit value in the corresponding bit [n] of GPIOx_DOUT is 1, the pin output drives high that is controlled by external pull high resistor.

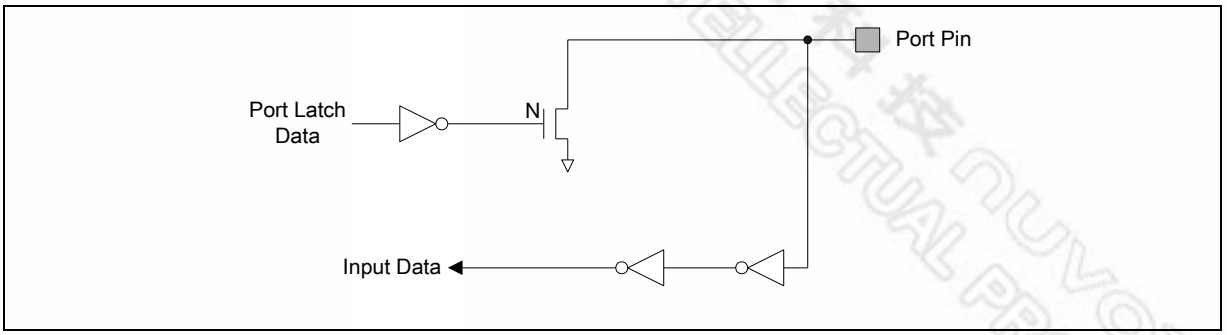


Figure 5-8 Open-Drain Output

5.5.2.4 Quasi-bidirectional Mode Explanation

Set GPIOx_PMD (PMDn[1:0]) to 11b the GPIOx port [n] pin is in Quasi-bidirectional mode and the I/O pin supports digital output and input function at the same time but the source current is only up to hundreds uA. Before the digital input function is performed the corresponding bit in GPIOx_DOUT must be set to 1. The quasi-bidirectional output is common on the 80C51 and most of its derivatives. If the bit value in the corresponding bit [n] of GPIOx_DOUT is 0, the pin drive a "low" output on the pin. If the bit value in the corresponding bit [n] of GPIOx_DOUT is 1, the pin will check the pin value. If pin value is high, no action takes. If pin state is low, then pin will drive strong high with 2 clock cycles on the pin and then disable the strong output drive and then the pin status is control by internal pull-up resistor. Note that the source current capability in quasi-bidirectional mode is only about 200 uA to 30 uA for VDD is form 5.0 V to 2.5 V.

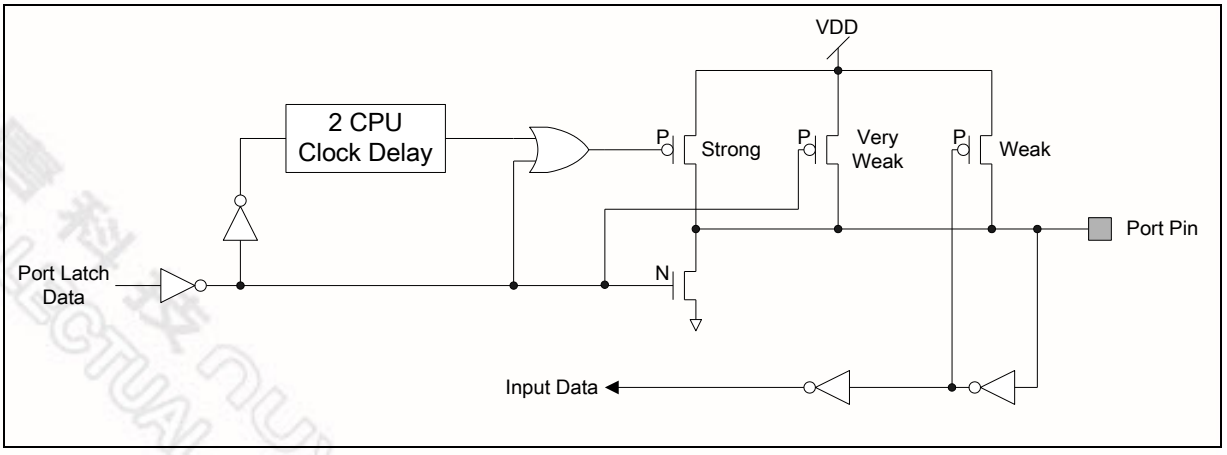


Figure 5-9 Quasi-bidirectional I/O Mode

38400	A=34	A=62,B=8 A=46,B=11 A=34,B=15	A=574
19200	A=70	A=126,B=8 A=94,B=11 A=70,B=15	A=1150
9600	A=142	A=254,B=8 A=190,B=11 A=142,B=15	A=2302
4800	A=286	A=510,B=8 A=382,B=11 A=286,B=15	A=4606

Table 5-6 UART Baud Rate Setting Table

The UART0/1 controllers support auto-flow control function that uses two low-level signals, /CTS (clear-to-send) and /RTS (request-to-send), to control the flow of data transfer between the UART and external devices (ex: Modem). When auto-flow is enabled, the UART is not allowed to receive data until the UART asserts /RTS to external device. When the number of bytes in the RX FIFO equals the value of RTS_TRI_LEV (UA_FCR [19:16]), the /RTS is de-asserted. The UART sends data out when UART controller detects /CTS is asserted from external device. If a valid asserted /CTS is not detected the UART controller will not send data out.

The UART controllers also provides Serial IrDA (SIR, Serial Infrared) function (User must set IrDA_EN (UA_FUN_SEL [1]) to enable IrDA function). The SIR specification defines a short-range infrared asynchronous serial transmission mode with one start bit, 8 data bits, and 1 stop bit. The maximum data rate is 115.2 Kbps (half duplex). The IrDA SIR block contains an IrDA SIR Protocol encoder/decoder. The IrDA SIR protocol is half-duplex only. So it cannot transmit and receive data at the same time. The IrDA SIR physical layer specifies a minimum 10 ms transfer delay between transmission and reception. This delay feature must be implemented by software.

For NuMicro™ NUC122, another alternate function of UART controllers is RS-485 9-bit mode function, and direction control provided by RTS pin or can program GPIO (PB.2 for RTS0 and PB.6 for RTS1) to implement the function by software. The RS-485 mode is selected by setting the UA_FUN_SEL register to select RS-485 function. The RS-485 driver control is implemented using the RTS control signal from an asynchronous serial port to enable the RS-485 driver. In RS-485 mode, many characteristics of the RX and TX are same as UART.

5.11 PS/2 Device Controller (PS2D)

5.11.1 Overview

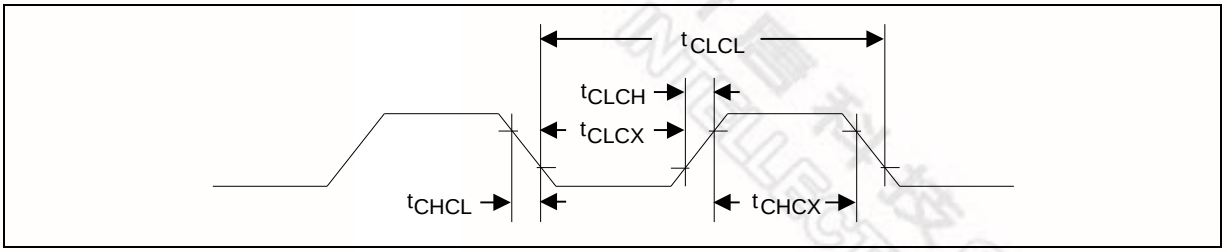
PS/2 device controller provides basic timing control for PS/2 communication. All communication between the device and the host is managed through the CLK and DATA pins. Unlike PS/2 keyboard or mouse device controller, the received/transmit code needs to be translated as meaningful code by firmware. The device controller generates the CLK signal after receiving a request to send, but host has ultimate control over communication. DATA sent from the host to the device is read on the rising edge and DATA sent from device to the host is change after rising edge. A 16 bytes FIFO is used to reduce CPU intervention. S/W can select 1 to 16 bytes for a continuous transmission.

5.11.2 Features

- Host communication inhibit and request to send detection
- Reception frame error detection
- Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
- Double buffer for data reception
- S/W override bus

6.3 AC Electrical Characteristics

6.3.1 External 4~24 MHz High Speed Crystal AC Electrical Characteristics



Note: Duty cycle is 50 %.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		20	-	-	nS
t_{CLCX}	Clock Low Time		20	-	-	nS
t_{CLCH}	Clock Rise Time		-	-	10	nS
t_{CHCL}	Clock Fall Time		-	-	10	nS

6.3.2 External 4~24 MHz High Speed Crystal

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	℃

6.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	without	without	without

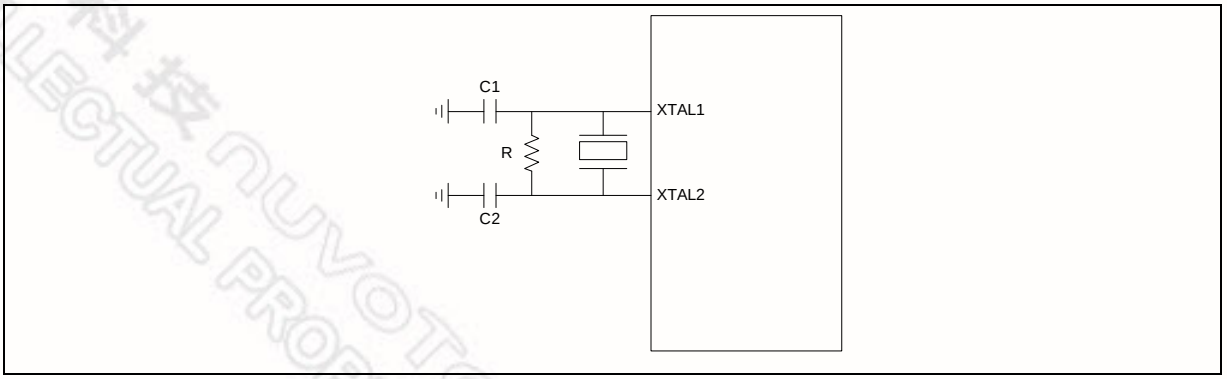


Figure 6-1 Typical Crystal Application Circuit

6.4 Analog Characteristics

6.4.1 Specification of LDO & Power management

PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
Input Voltage	2.5	5	5.5	V	V_{DD} input voltage
Output Voltage	1.6	1.8	2.1	V	$V_{DD} \geq 2.5$ V
Temperature	-40	25	85	℃	
Quiescent Current (PD=0)	-	100	-	μA	
Quiescent Current (PD=1)	-	5	-	μA	
Iload (PD=0)	-	-	100	mA	
Iload (PD=1)	-	-	100	μA	
Cbp	-	4.7	-	μF	Resr=1 ohm

Note:

1. It is recommended that a 10 μF or higher capacitor and a 100 nF bypass capacitor are connected between VDD and the closest VSS pin of the device.

2. For ensuring power stability, a 4.7 μF or higher capacitor must be connected between LDO pin and the closest VSS pin of the device.

6.5 SPI Dynamic Characteristics

6.5.1 Dynamic Characteristics of Data Input and Output Pin

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
SPI Master Mode (VDD = 4.5 V ~ 5.5 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	16	10	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	5	8	ns
SPI Master Mode (VDD = 3.0 V ~ 3.6 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	20	13	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	7	14	ns
SPI Slave Mode (VDD = 4.5 V ~ 5.5 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2*PCLK+4	-	-	ns
t_V	Data output valid time	-	2*PCLK+11	2*PCLK+20	ns
SPI Slave Mode (VDD = 3.0 V ~ 3.6 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2*PCLK+8	-	-	ns
t_V	Data output valid time	-	2*PCLK+20	2*PCLK+32	ns

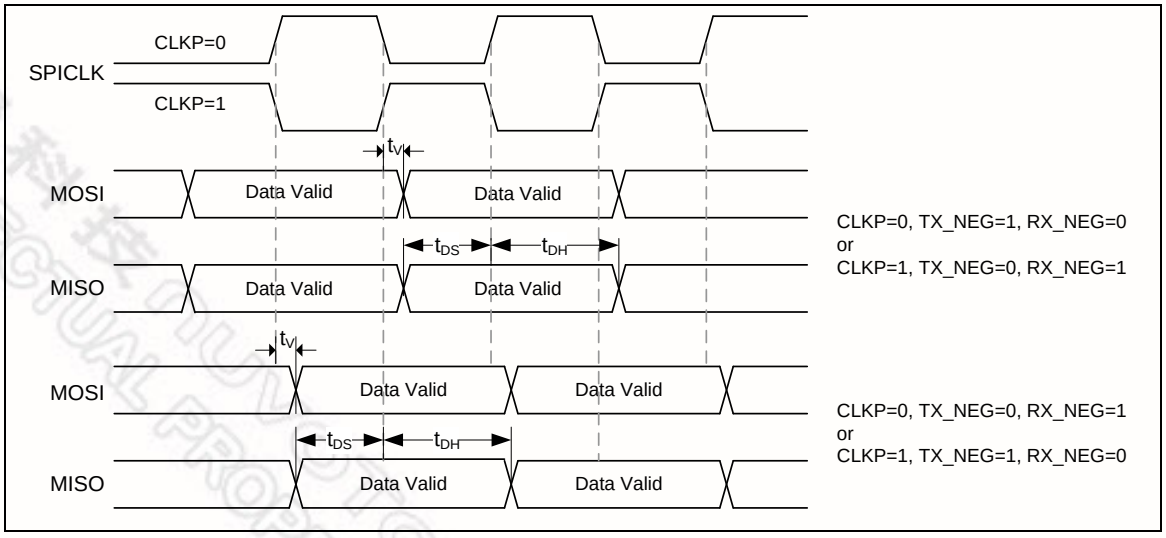
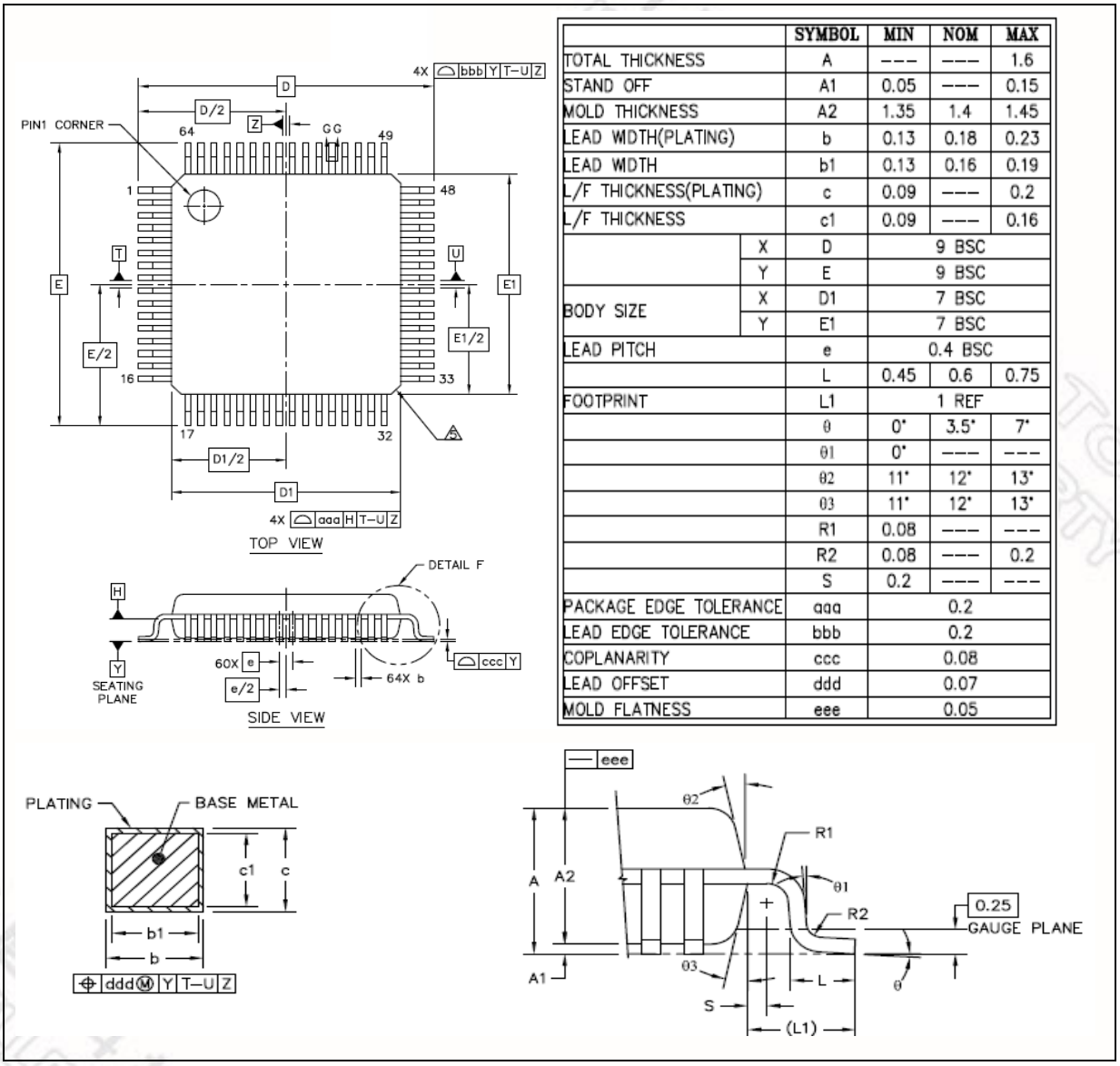


Figure 6-2 SPI Master Mode Timing

7 PACKAGE DIMENSIONS

7.1 64L LQFP (7x7x1.4mm footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		