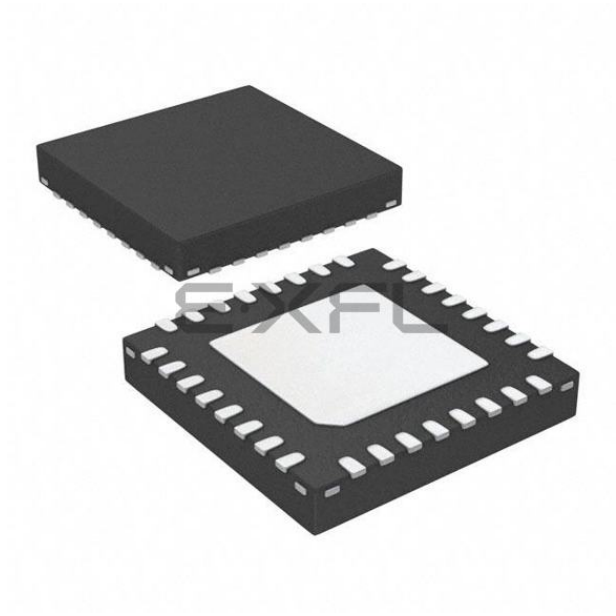

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PS2, WDT
Number of I/O	18
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc122zc1an

3.2.3 NuMicro™ NUC122 QFN 33-pin

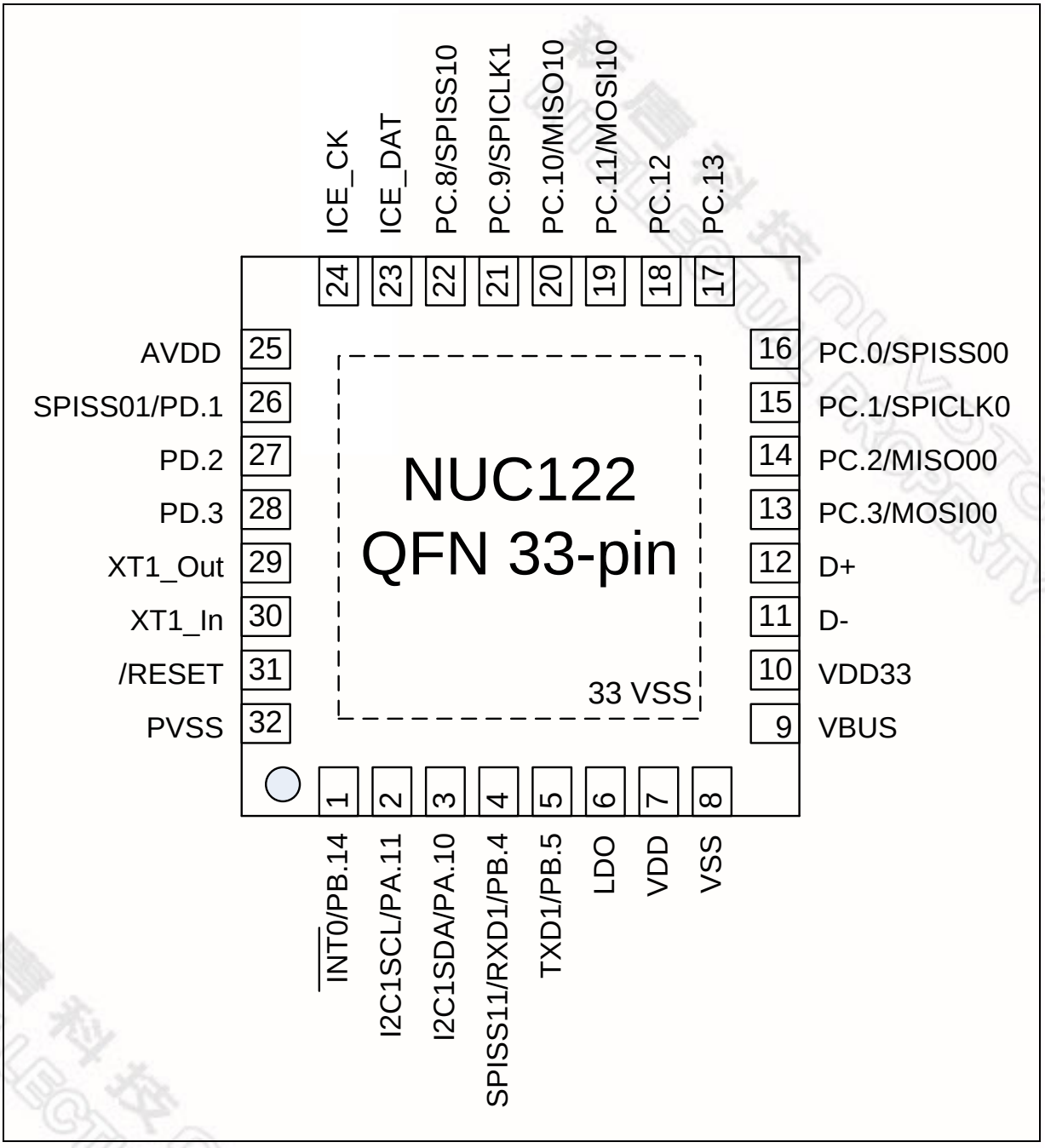

Figure 3-3 NuMicro™ NUC122 QFN 33-pin Pin Diagram

Pin No.			Pin Name	Pin Type	Description
LQFP 64	LQFP 48	QFN 33			
36	27	19	PC.11	I/O	General purpose input/output digital pin
			MOSI10	O	MOSI10: SPI1 MOSI (Master Out, Slave In) pin
37	28	20	PC.10	I/O	General purpose input/output digital pin
			MISO10	I	MISO10: SPI1 MISO (Master In, Slave Out) pin
38			VDD	P	Power supply for I/O ports
39	29	21	PC.9	I/O	General purpose input/output digital pin
			SPICLK1	I/O	SPICLK1: SPI1 serial clock pin
40	30	22	PC.8	I/O	General purpose input/output digital pin
			SPISS10	I/O	SPISS10: SPI1 slave select pin
41	31		PA.15	I/O	General purpose input/output digital pin
			PWM3	O	PWM3: PWM output pin
42			VSS	P	Ground
43	32		PA.14	I/O	General purpose input/output digital pin
			PWM2	O	PWM2: PWM output pin
44	33		PA.13	I/O	General purpose input/output digital pin
			PWM1	O	PWM1: PWM output pin
45	34		PA.12	I/O	General purpose input/output digital pin
			PWM0	O	PWM0: PWM output pin
46	35	23	ICE_DAT	I/O	Serial Wired Debugger Data pin
47	36	24	ICE_CK	I	Serial Wired Debugger Clock pin
48	37	25	AVDD	AP	Power supply for internal analog circuit
49	38		PD.0	I/O	General purpose input/output digital pin
50	39	26	PD.1	I/O	General purpose input/output digital pin
			SPISS01	I/O	SPISS01: SPI0 2nd slave select pin (for QFN33 only)
51	40	27	PD.2	I/O	General purpose input/output digital pin
52	41	28	PD.3	I/O	General purpose input/output digital pin
53	42		PD.4	I/O	General purpose input/output digital pin
54	43		PD.5	I/O	General purpose input/output digital pin
55			PB.15	I/O	General purpose input/output digital pin

Pin No.			Pin Name	Pin Type	Description
LQFP 64	LQFP 48	QFN 33			
			/INT1	**I**	/INT1: External interrupt 1 input pin
56	44	29	XT1_OUT	**O**	Crystal output pin
57	45	30	XT1_IN	**I**	Crystal input pin
58	46	31	/RESET	**I**	External reset input: Low active, set this pin low reset chip to initial state. With internal pull-up.
59		33	VSS	**P**	Ground
60			VDD	**P**	Power supply for I/O ports
61	47		PS2DAT	**I/O**	PS/2 data pin
62	48		PS2CLK	**I/O**	PS/2 clock pin
63	1	32	PVSS	**P**	PLL Ground
64			PB.8	**I/O**	General purpose input/output digital pin
			TM0	**O**	TM0: Timer0 external counter input

Note: Pin Type I=Digital Input, O=Digital Output; AI=Analog Input; P=Power Pin; AP=Analog Power

4 BLOCK DIAGRAM

4.1 NuMicro™ NUC122 Block Diagram

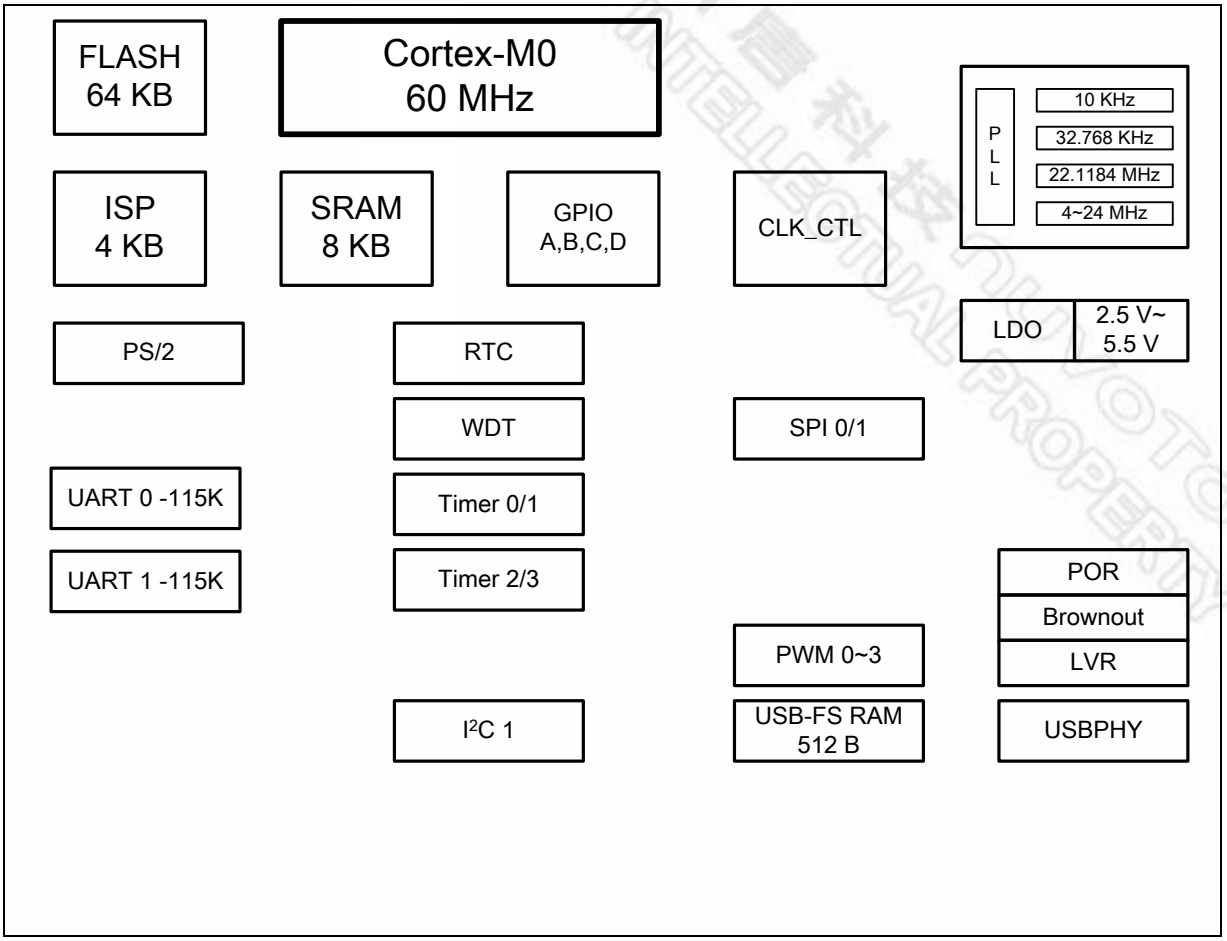

Figure 4-1 NuMicro™ NUC122 Block Diagram

5.2 System Manager

5.2.1 Overview

System management includes these following sections:

- System Resets
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

5.2.2 System Reset

The system reset can be issued by one of the below listed events. These reset event flags can be read from RSTSRC register.

- The Power-On Reset
- The low level on the /RESET pin
- Watchdog Timer Time-Out Reset
- Low Voltage Reset
- Brownout Detector Reset
- Cortex®-M0 Reset
- System Reset

Both System Reset and Power-On Reset can reset the whole chip including all peripherals. The difference between System Reset and Power-On Reset is external Crystal circuit and ISPCON.BS bit. System Reset doesn't reset external Crystal circuit and ISPCON.BS bit, but Power-On Reset does.

5.2.3 System Power Distribution

In this chip, the power distribution is divided into three segments.

- Analog power from AVDD and AVSS provides the power for analog components operation.
- Digital power from VDD and VSS supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.
- USB transceiver power from VBUS offers the power for operating the USB transceiver.

The outputs of internal voltage regulators, LDO and VDD33, require an external capacitor which should be located close to the corresponding pin. Analog power (AVDD) should be the same voltage level of the digital power (VDD). The following diagram shows the power distribution of this chip.

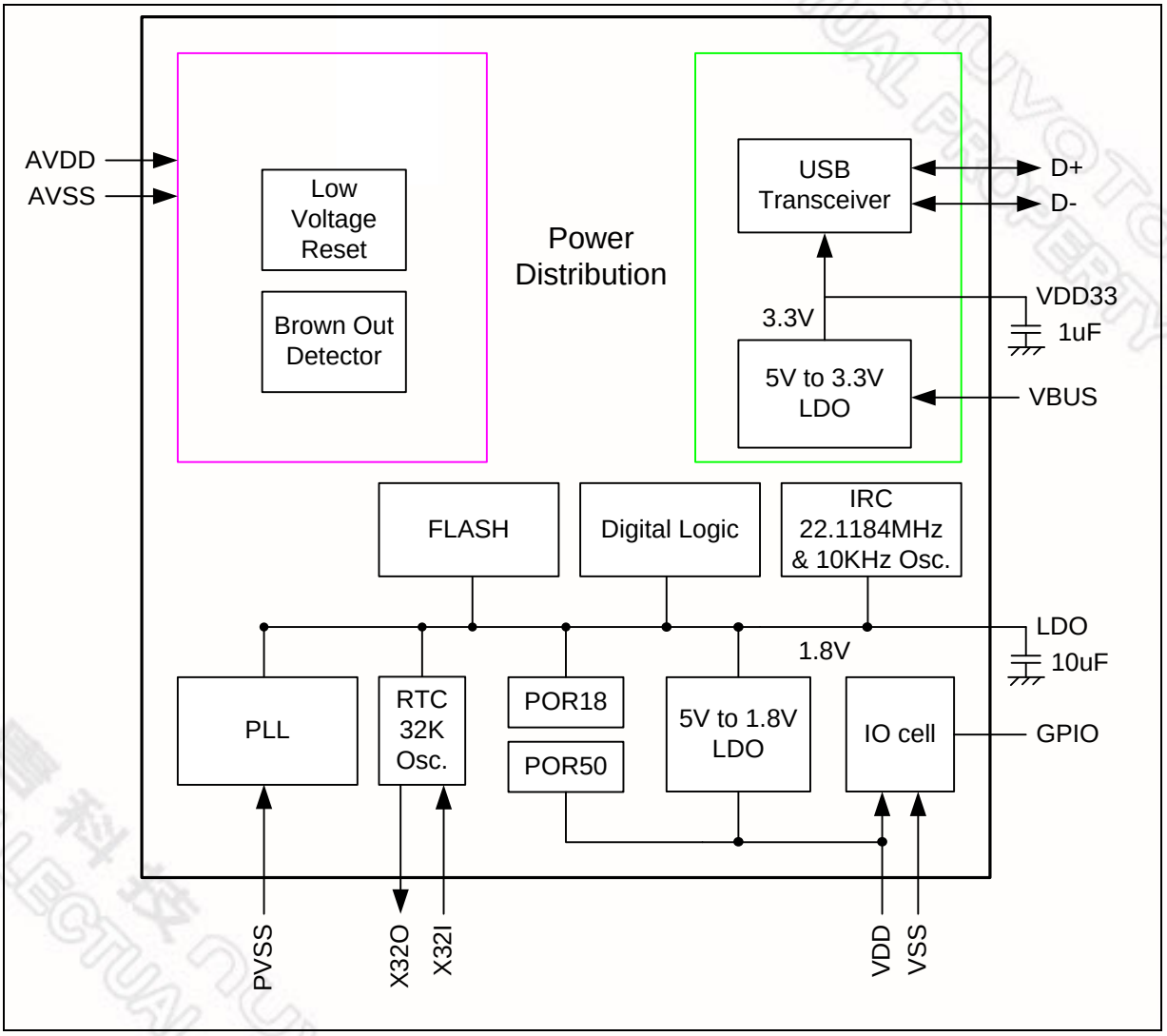

Figure 5-2 NuMicro™ NUC122 Power Distribution Diagram

5.2.5 Nested Vectored Interrupt Controller (NVIC)

Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)". It is closely coupled to the processor kernel and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Dynamic priority changing
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When any interrupts is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the documents "ARM® Cortex®-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

28	12	**Reserved**	Reserved	Reserved
29	13	**UART1_INT**	UART1	UART1 interrupt
30	14	**SPI0_INT**	SPI0	SPI0 interrupt
31	15	**SPI1_INT**	SPI1	SPI1 interrupt
32	16	**Reserved**	Reserved	Reserved
33	17	**Reserved**	Reserved	Reserved
34	18	**Reserved**	Reserved	Reserved
35	19	**I2C1_INT**	I^2C1	I^2C1 interrupt
36	20	**Reserved**	Reserved	Reserved
37	21	**Reserved**	Reserved	Reserved
38	22	**Reserved**	Reserved	Reserved
39	23	**USB_INT**	USBD	USB 2.0 FS Device interrupt
40	24	**PS2_INT**	PS/2	PS/2 interrupt
41	25	**Reserved**	Reserved	Reserved
42	26	**Reserved**	Reserved	Reserved
43	27	**Reserved**	Reserved	Reserved
44	28	**PWRWU_INT**	CLKC	Power Down Wake-up interrupt
45	29	**Reserved**	Reserved	Reserved
46	30	**Reserved**	Reserved	Reserved
47	31	**RTC_INT**	RTC	Real time clock interrupt

Table 5-2 System Interrupt Map

5.2.5.2 Vector Table

When any interrupts is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARM® v6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 5-3 Vector Table Format

5.2.5.3 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

5.3.3 System Clock & SysTick Clock

The system clock has 5 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is listed below.

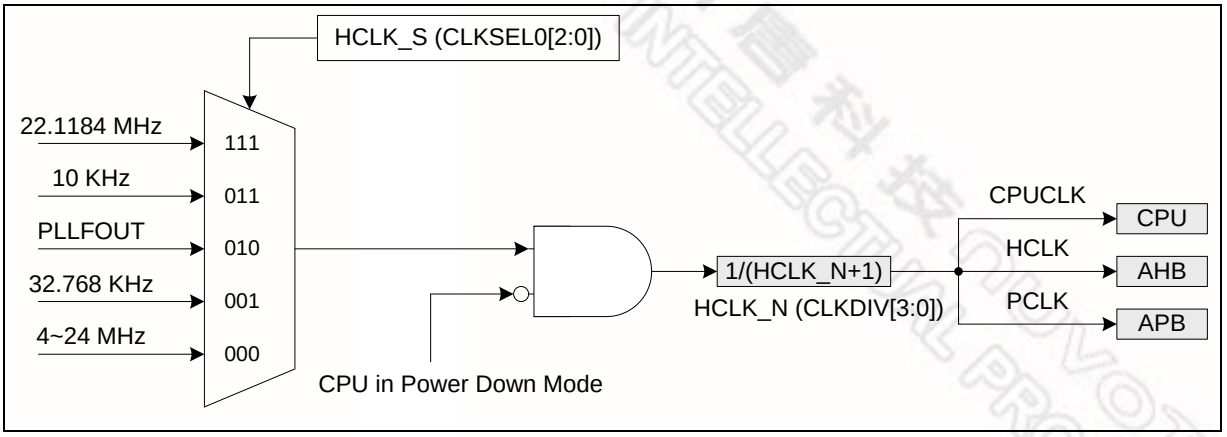

Figure 5-5 System Clock Block Diagram

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]. The block diagram is listed below.

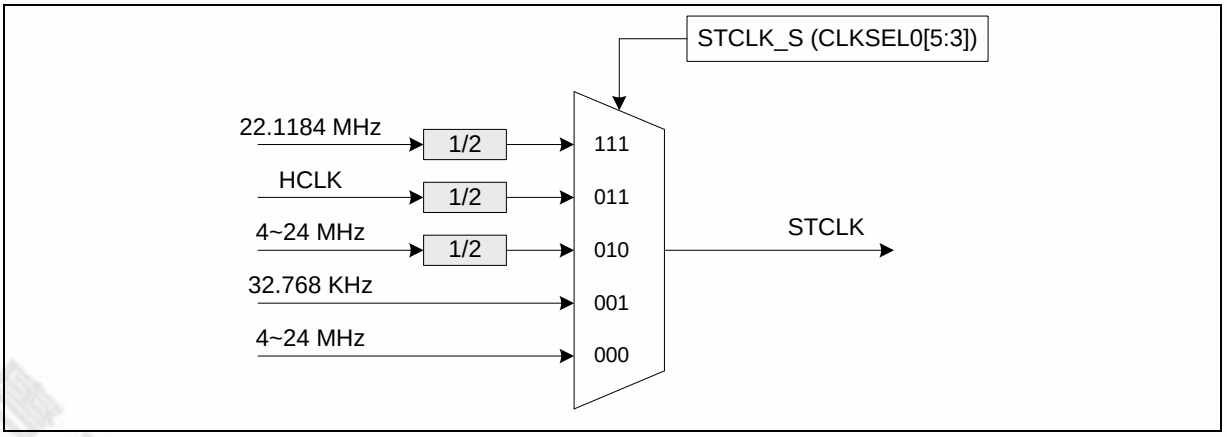

Figure 5-6 SysTick Clock Control Block Diagram

5.8 Watchdog Timer (WDT)

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports another function to wake-up chip from power down mode. The Watchdog Timer includes an 18-bit free running counter with programmable time-out intervals. Table 5-4 show the Watchdog Timer time-out interval selection and Figure 5-10 shows the timing of Watchdog interrupt signal and reset signal.

Setting WTE (WDTCR [7]) enables the watchdog timer and the WDT counter starts counting up. When the counter reaches the selected time-out interval, Watchdog timer interrupt flag WTIF will be set immediately to request a WDT interrupt if the watchdog timer interrupt enable bit WTIE is set, in the meanwhile, a specified delay time (1024 * T_{WDT}) follows the time-out event. User must set WTR (WDTCR [0]) (Watchdog timer reset) high to reset the 18-bit WDT counter to avoid chip from Watchdog timer reset before the delay time expires. WTR bit is cleared automatically by hardware after WDT counter is reset. There are eight time-out intervals with specific delay time which are selected by Watchdog timer interval select bits WTIS (WDTCR [10:8]). If the WDT counter has not been cleared after the specific delay time expires, the watchdog timer will set Watchdog Timer Reset Flag (WTRF) high and reset chip. This reset will last 63 WDT clocks (T_{RST}) then chip restarts executing program from reset vector (0x0000_0000). WTRF will not be cleared by Watchdog reset. User may poll WTRF by software to recognize the reset source. WDT also provides wake-up function. When chip is powered down and the Watchdog Timer Wake-up Function Enable bit (WDTR[4]) is set, if the WDT counter reaches the specific time interval defined by WTIS (WDTCR [10:8]) , the chip is woken-up from power down state. First example, if WTIS is set as 000, the specific time interval for chip to be woken-up from power down state is 2^4 * T_{WDT}. When power down command is set by software, then, chip enters power down state. After 2^4 * T_{WDT} time is elapsed, chip is woken-up from power down state. Second example, if WTIS (WDTCR [10:8]) is set as 111, the specific time interval for chip to be woken-up from power down state is 2^{18} * T_{WDT}. If power down command is set by software, then, chip enters power down state. After 2^{18} * T_{WDT} time is elapsed, chip is woken-up from power down state. Notice if WTRE (WDTCR [1]) is set to 1, after chip is woken-up, software should clear the Watchdog Timer counter by setting WTR(WDTCR [0]) to 1 as soon as possible. Otherwise, if the Watchdog Timer counter is not cleared by setting WTR (WDTCR [0]) to 1 before time starting from waking up to software clearing Watchdog Timer counter is over 1024 * T_{WDT} , the chip is reset by Watchdog Timer.

WTIS	Time-out Interval Selection T_{TIS}	Interrupt Period T_{INT}	WTR Time-out Interval (WDT_CLK=10 KHz) Min. T_{WTR} ~ Max. T_{WTR}
000	2^4 * T_{WDT}	1024 * T_{WDT}	1.6 ms ~ 104 ms
001	2^6 * T_{WDT}	1024 * T_{WDT}	6.4 ms ~ 108.8 ms
010	2^8 * T_{WDT}	1024 * T_{WDT}	25.6 ms ~ 128 ms
011	2^{10} * T_{WDT}	1024 * T_{WDT}	102.4 ms ~ 204.8 ms
100	2^{12} * T_{WDT}	1024 * T_{WDT}	409.6 ms ~ 512 ms
101	2^{14} * T_{WDT}	1024 * T_{WDT}	1.6384 s ~ 1.7408 s
110	2^{16} * T_{WDT}	1024 * T_{WDT}	6.5536 s ~ 6.656 s
111	2^{18} * T_{WDT}	1024 * T_{WDT}	26.2144 s ~ 26.3168 s

Table 5-4 Watchdog Timer Time-out Interval Selection

5.10 UART Interface Controller (UART)

NuMicro™ NUC122 provides two channels of Universal Asynchronous Receiver/Transmitters (UART0/1). Both of UART0 and UART1 perform Normal Speed UART, besides, UART0 and UART1 also support flow control function.

5.10.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART0/1) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function and RS-485 mode functions. Each UART channel supports seven types of interrupts including transmitter FIFO empty interrupt (INT_THRE), receiver threshold level reaching interrupt (INT_RDA), line status interrupt (parity error or framing error or break interrupt) (INT_RLS), receiver buffer time-out interrupt (INT_TOUT), MODEM/Wake-Up status interrupt (INT_MODEM), Buffer error interrupt (INT_BUF_ERR). Interrupt number 13 (vector number is 29) supports UART0/1 interrupt. Refer to Nested Vectored Interrupt Controller chapter for System Interrupt Map.

The UART0/1 are equipped 14-byte transmitter FIFO (TX_FIFO) and 14-byte receiver FIFO (RX_FIFO). The CPU can read the status of the UART at any time during the operation. The reported status information includes the type and condition of the transfer operations being performed by the UART, as well as 4 error conditions (parity error, framing error, break interrupt and buffer error) probably occur while receiving data. The UART includes a programmable baud rate generator that is capable of dividing clock input by divisors to produce the serial clock that transmitter and receiver need. The baud rate equation is Baud Rate = UART_CLK / M * [BRD + 2], where M and BRD are defined in Baud Rate Divider Register (UA_BAUD). Below table lists the equations in the various conditions and the UART baud rate setting table.

Mode	DIV_X_EN	DIV_X_ONE	Divider X	BRD	Baud rate equation
0	0	0	B	A	UART_CLK / [16 * (A+2)]
1	1	0	B	A	UART_CLK / [(B+1) * (A+2)] , B must >= 8
2	1	1	Don't care	A	UART_CLK / (A+2), A must >=3

Table 5-5 UART Baud Rate Equation

System clock = 22.1184 MHz high speed			
Baud rate	Mode0	Mode1	Mode2
921600	x	A=0,B=11	A=22
460800	A=1	A=1,B=15 A=2,B=11	A=46
230400	A=4	A=4,B=15 A=6,B=11	A=94
115200	A=10	A=10,B=15 A=14,B=11	A=190
57600	A=22	A=22,B=15 A=30,B=11	A=382

5.11 PS/2 Device Controller (PS2D)

5.11.1 Overview

PS/2 device controller provides basic timing control for PS/2 communication. All communication between the device and the host is managed through the CLK and DATA pins. Unlike PS/2 keyboard or mouse device controller, the received/transmit code needs to be translated as meaningful code by firmware. The device controller generates the CLK signal after receiving a request to send, but host has ultimate control over communication. DATA sent from the host to the device is read on the rising edge and DATA sent from device to the host is change after rising edge. A 16 bytes FIFO is used to reduce CPU intervention. S/W can select 1 to 16 bytes for a continuous transmission.

5.11.2 Features

- Host communication inhibit and request to send detection
- Reception frame error detection
- Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
- Double buffer for data reception
- S/W override bus

5.13 Serial Peripheral Interface (SPI)

5.13.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol which operates in full duplex mode. Devices communicate in master/slave mode with 4-wire bi-direction interface. The NuMicro™ NUC122 contains up to two sets of SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each set of SPI controller can be set as a master that can drive up to 2 external peripheral slave devices; it also can be configured as a slave device controlled by an off-chip master device.

This controller also supports a variable serial clock for special application.

5.13.2 Features

- Up to two sets of SPI controller for NuMicro™ NUC122
- Support master or slave mode operation
- Support 1-bit transfer mode
- Configurable bit length up to 32 bits of a transfer word and configurable word numbers up to 2 of a transaction, so the maximum bit length is 64 bits for each data transfer
- Provide burst mode operation, transmit/receive can be transferred up to two times word transaction in one transfer
- Support MSB or LSB first transfer
- 2 device/slave select lines in master mode, but 1 device/slave select line in slave mode
- Support byte reorder in data register
- Support byte or word suspend mode
- Variable output serial clock frequency in master mode
- Support two programmable serial clock frequencies in master mode

6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into VDD		-	120	mA
Maximum Current out of VSS			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

6.2 DC Electrical Characteristics

6.2.1 NuMicro™ NUC122 DC Electrical Characteristics

(V_{DD}-V_{SS}=3.3 V, TA = 25 °C, FOSC = 60 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} =2.5 V ~ 5.5 V up to 60 MHz
LDO Output Voltage	V_{LDO}	1.6	1.8	2.1	V	$V_{DD} \geqq$ 2.5 V
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
Operating Current Normal Run Mode @ 60 MHz	I_{DD1}		26		mA	V_{DD} = 5.5 V @ 60 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{DD2}		21		mA	V_{DD} = 5.5 V @ 60 MHz, disable all IP and enable PLL, XTAL=12 MHz
	I_{DD3}		24		mA	V_{DD} = 3.3 V @ 60 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{DD4}		19		mA	V_{DD} = 3.3 V @ 60 MHz, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Normal Run Mode @ 12 MHz	I_{DD5}		6.5		mA	V_{DD} = 5.5 V @ 12MHz, enable all IP and disable PLL, XTAL=12 MHz
	I_{DD6}		5		mA	V_{DD} = 5.5 V @ 12 MHz, disable all IP and PLL, XTAL=12 MHz
	I_{DD7}		4.5		mA	V_{DD} = 3.3 V @ 12 MHz, enable all IP and disable PLL, XTAL=12 MHz
	I_{DD8}		3.5		mA	V_{DD} = 3.3 V @ 12 MHz, disable all IP and PLL, XTAL=12 MHz
Operating Current Normal Run Mode @ 4 MHz	I_{DD9}		3.5		mA	V_{DD} = 5.5 V @ 4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{DD10}		3		mA	V_{DD} = 5.5 V @ 4 MHz,

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
						disable all IP and PLL, XTAL=4 MHz
	I_{DD11}		3		mA	V_{DD} = 3.3 V @ 4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{DD12}		2		mA	V_{DD} = 3.3 V @ 4 MHz, disable all IP and PLL, XTAL=4 MHz
Operating Current Idle Mode @ 60 MHz	I_{IDLE1}		17		mA	V_{DD} = 5.5 V @ 60 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{IDLE2}		12		mA	V_{DD} = 5.5 V @ 60 MHz, disable all IP and enable PLL, XTAL=12 MHz
	I_{IDLE3}		15		mA	V_{DD} = 3.3 V @ 60 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{IDLE4}		11		mA	V_{DD} = 3.3 V @ 60 MHz, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Idle Mode @ 12 MHz	I_{IDLE5}		4.5		mA	V_{DD} = 5.5 V @ 12 MHz, enable all IP and disable PLL, XTAL=12 MHz
	I_{IDLE6}		3.5		mA	V_{DD} = 5.5 V @ 12 MHz, disable all IP and PLL, XTAL=12 MHz
	I_{IDLE7}		3		mA	V_{DD} = 3.3 V @ 12 MHz, enable all IP and disable PLL, XTAL=12 MHz
	I_{IDLE8}		2		mA	V_{DD} = 3.3 V @ 12 MHz, disable all IP and PLL, XTAL=12 MHz
Operating Current Idle Mode @ 4 MHz	I_{IDLE9}		3		mA	V_{DD} = 5.5 V @ 4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{IDLE10}		2.5		mA	V_{DD} = 5.5 V @ 4 MHz, disable all IP and PLL, XTAL=4 MHz
	I_{IDLE11}		2		mA	V_{DD} = 3.3 V @ 4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{IDLE12}		1		mA	V_{DD} = 3.3 V @ 4 MHz, disable all IP and PLL, XTAL=4 MHz

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Standby Current Power Down Mode	I_{PWD1}		13		μA	V_{DD} = 5.5 V, RTC OFF, No load @ Disable BOV function
	I_{PWD2}		12		μA	V_{DD} = 3.3 V, RTC OFF, No load @ Disable BOV function
	I_{PWD3}		15		μA	V_{DD} = 5.5 V, RTC run , No load @ Disable BOV function
	I_{PWD4}		13		μA	V_{DD} = 3.3 V, RTC run , No load @ Disable BOV function
Input Current PA, PB, PC, PD (Quasi-bidirectional mode)	I_{IN1}	-60	-	+15	μA	V_{DD} = 5.5 V, V_{IN} = 0 V or V_{IN}=V_{DD}
Input Current at /RESET[1]	I_{IN2}	-55	-45	-30	μA	V_{DD} = 3.3 V, V_{IN} = 0.45 V
Input Leakage Current PA, PB, PC, PD	I_{LK}	-2	-	+2	μA	V_{DD} = 5.5 V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current PA~PD (Quasi-bidirectional mode)	I_{TL} [3]	-650	-	-200	μA	V_{DD} = 5.5 V, V_{IN}<2.0 V
Input Low Voltage PA, PB, PC, PD (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5 V
		-0.3	-	0.6		V_{DD} = 2.5 V
Input High Voltage PA, PB, PC, PD(TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5 V
		1.5	-	V_{DD} +0.2		V_{DD} = 3.0 V
Input Low Voltage PA, PB, PC, PD (Schmitt input)	V_{IL2}	-0.5		0.4 V_{DD}	V	
Input High Voltage PA, PB, PC, PD(Schmitt input)	V_{IH2}	0.6 V_{DD}		V_{DD}+0.5	V	
Hysteresis voltage of PA~PD (Schmitt input)	V_{HY}		0.2 V_{DD}		V	
Negative going threshold (Schmitt input), /RESET	V_{ILS}	-0.5	-	0.3 V_{DD}	V	
Positive going threshold (Schmitt input), /RESET	V_{IHS}	0.7 V_{DD}	-	V_{DD}+0.5	V	
Source Current PA, PB, PC, PD (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	V_{DD} = 4.5 V, V_S = 2.4 V
	I_{SR12}	-50	-70	-90	μA	V_{DD} = 2.7 V, V_S = 2.2 V
	I_{SR12}	-40	-60	-80	μA	V_{DD} = 2.5 V, V_S = 2.0 V
Source Current PA, PB, PC, PD (Push-pull Mode)	I_{SR21}	-22	-28	-32	mA	V_{DD} = 4.5 V, V_S = 2.4 V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7 V, V_S = 2.2 V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5 V, V_S = 2.0 V

6.4.5 Specification of USB PHY

6.4.5.1 USB DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input high (driven)		2.0			V
V_{IL}	Input low				0.8	V
V_{DI}	Differential input sensitivity	|PADP-PADM|	0.2			V
V_{CM}	Differential common-mode range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended receiver threshold		0.8		2.0	V
	Receiver hysteresis			200		mV
V_{OL}	Output low (driven)		0		0.3	V
V_{OH}	Output high (driven)		2.8		3.6	V
V_{CRS}	Output signal cross voltage		1.3		2.0	V
R_{PU}	Pull-up resistor		1.425		1.575	kΩ
R_{PD}	Pull-down resistor		14.25		15.75	kΩ
V_{TRM}	Termination Voltage for upstream port pull up (RPU)		3.0		3.6	V
Z_{DRV}	Driver output resistance	Steady state drive*		10		Ω
C_{IN}	Transceiver capacitance	Pin to GND			20	pF

*Driver output resistance doesn't include series resistor resistance.

6.4.5.2 USB Full-Speed Driver Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{FR}	Rise Time	C_L=50p	4		20	ns
T_{FF}	Fall Time	C_L=50p	4		20	ns
T_{FRFF}	Rise and fall time matching	$T_{FRFF}=T_{FR}/T_{FF}$	90		111.11	%

6.4.5.3 USB Power Dissipation

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{VDDREG} (Full Speed)	V_{DDD} and V_{DDREG} Supply Current (Steady State)	Standby		50		μA
		Input mode				μA
		Output mode				μA

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