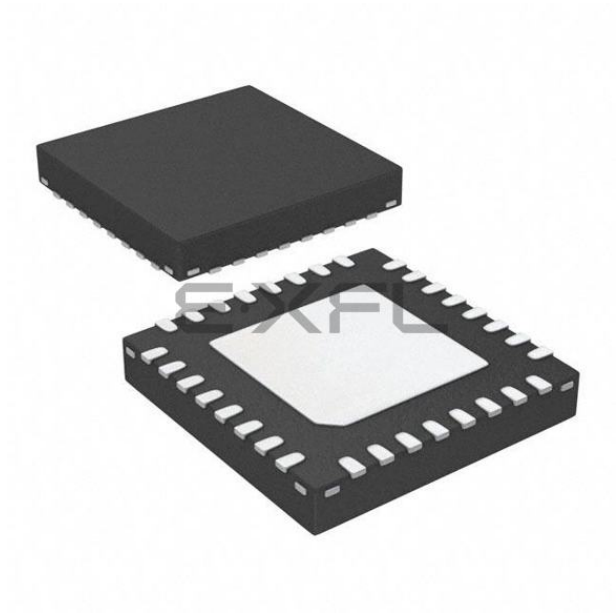

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PS2, WDT
Number of I/O	18
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc122zd2an

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2 FEATURES

2.1 NuMicro™ NUC122 Features

- Core
  - ARM® Cortex®-M0 core runs up to 60 MHz
  - One 24-bit system timer
  - Support low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Wide operating voltage ranges from 2.5 V to 5.5 V
- Flash Memory
  - 32K/64K bytes Flash for program code
  - 4KB Flash for ISP loader
  - Support In System Program (ISP) function to update Application code
  - 512 bytes page erase for Flash
  - 4KB Data Flash
  - Support 2 wire In Circuit Program (ICP) function to update code through SWD/ICE interface
  - Support fast parallel programming mode by external programmer
- SRAM Memory
  - 4K/8K bytes embedded SRAM
- Clock Control
  - Flexible selection from different clock sources
  - Built-in 22.1184 MHz high speed OSC for system operation
    - Trimmed to ± 1 % at +25 ℃ and V_{DD} = 3.3 V
    - Trimmed to ± 5 % at -40 ℃ ~ +85 ℃ and V_{DD} = 2.5 V ~ 5.5 V
  - Built-in 10 KHz low speed OSC for Watchdog Timer and Wake-up operation
  - Support one PLL, up to 60 MHz, for high performance system operation
  - External 4~24 MHz high speed crystal input for USB and precise timing operation
  - External 32.768 KHz low speed crystal input for RTC function and low power system operation
- GPIO
  - Four I/O modes:
    - Quasi bi-direction
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin can be configured as interrupt source with edge/level setting
  - High driver and high sink IO mode support
- Timers
  - 4 sets of 32-bit timers with 24-bit counters and one 8-bit prescaler
  - Counter auto reload

3.2.2 NuMicro™ NUC122 LQFP 48-pin

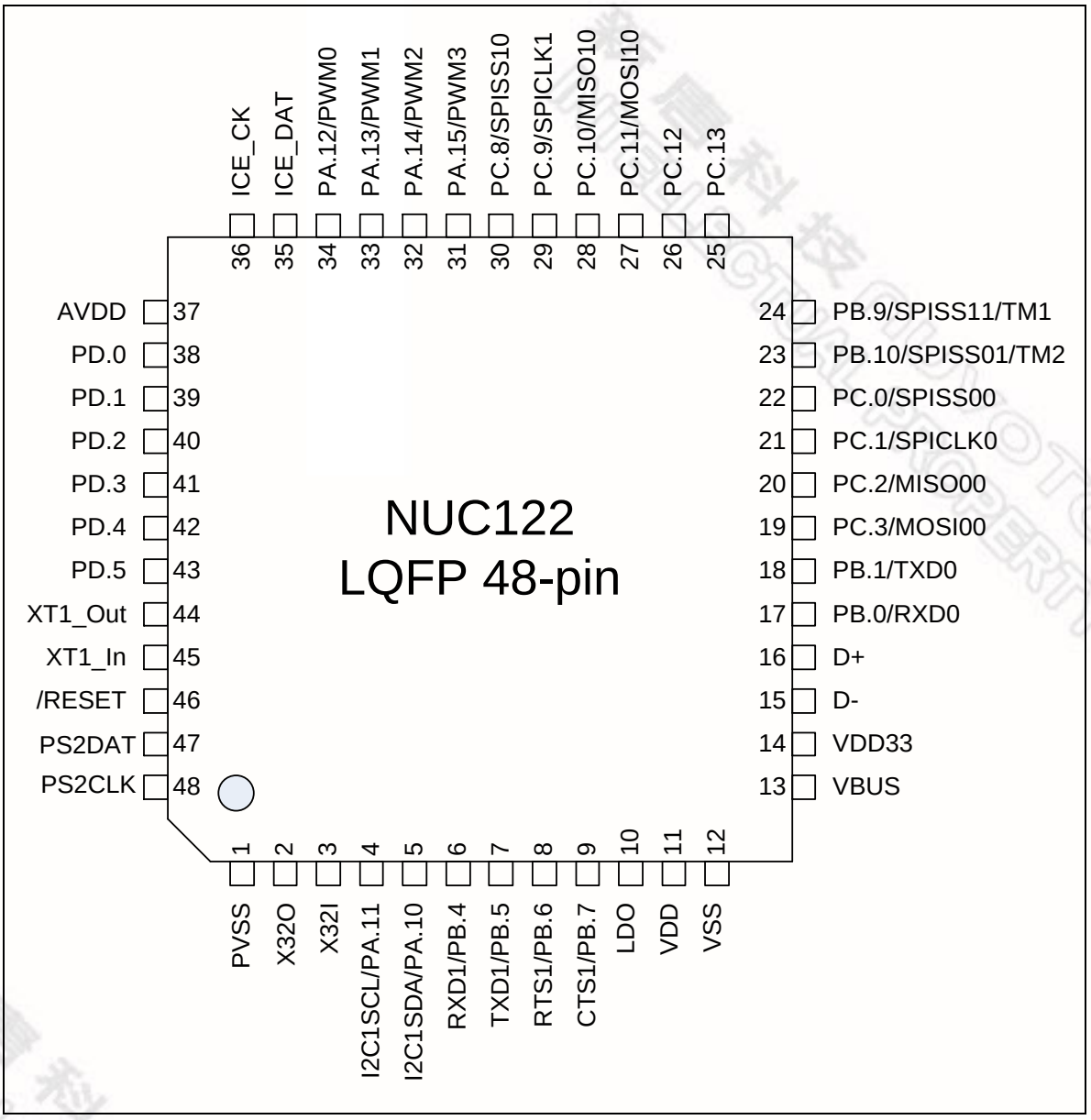


Figure 3-2 NuMicro™ NUC122 LQFP 48-pin Pin Diagram

3.2.3 NuMicro™ NUC122 QFN 33-pin

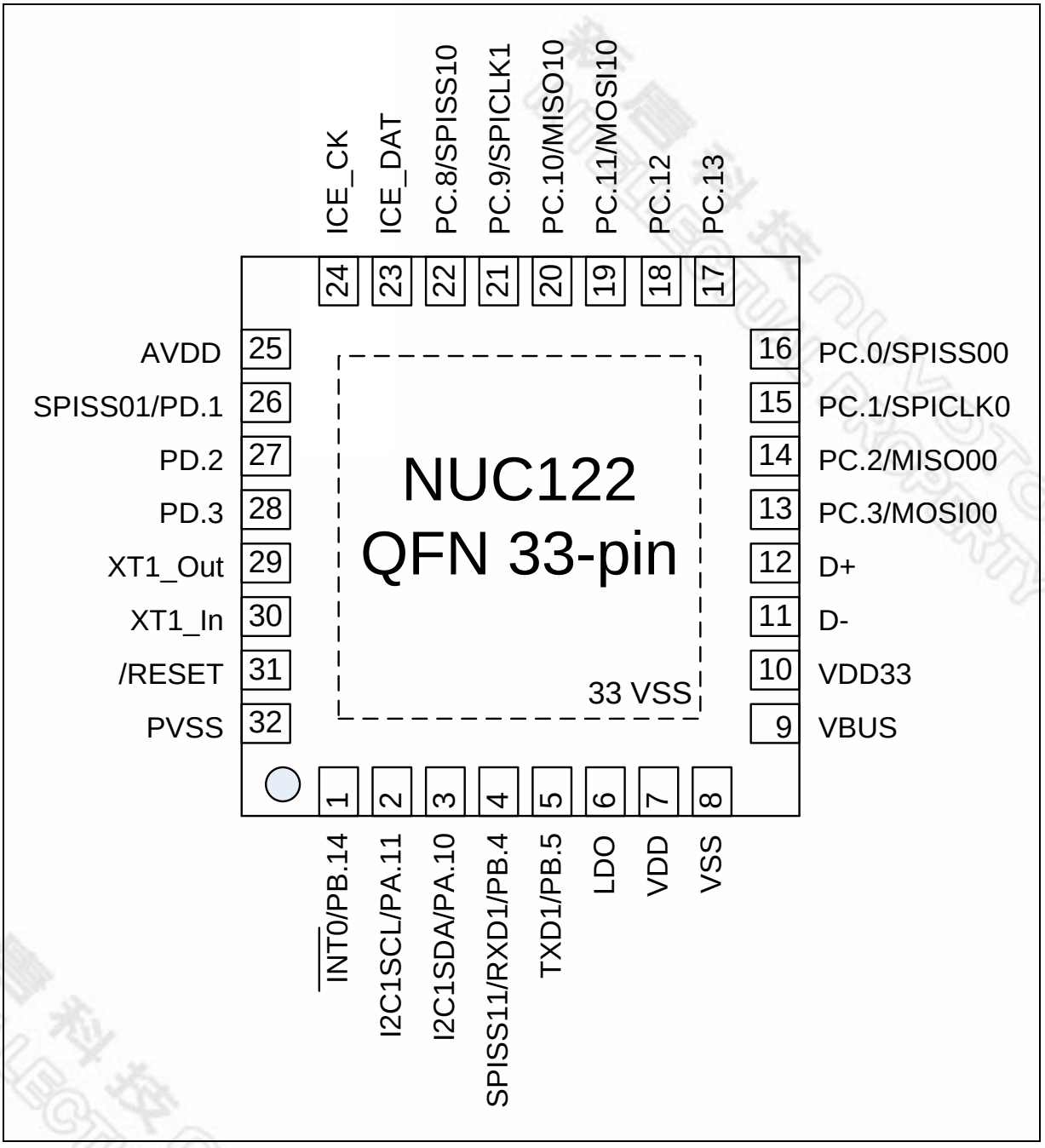


Figure 3-3 NuMicro™ NUC122 QFN 33-pin Pin Diagram

3.3 NuMicro™ NUC122 Pin Description

3.3.1 NuMicro™ NUC122 Pin Description for LQFP64/LQFP48/QFN33

Pin No.			Pin Name	Pin Type	Description
LQFP 64	LQFP 48	QFN 33			
1		1	PB.14	I/O	General purpose input/output digital pin
			/INT0	I	/INT0: External interrupt1 input pin
2	2		X32O	O	32.768 KHz low speed crystal output pin
3	3		X32I	I	32.768 KHz low speed crystal input pin
4	4	2	PA.11	I/O	General purpose input/output digital pin
			I2C1SCL	I/O	I2C1SCL: I^2C1 clock pin
5	5	3	PA.10	I/O	General purpose input/output digital pin
			I2C1SDA	I/O	I2C1SDA: I^2C1 data input/output pin
6			PD.8	I/O	General purpose input/output digital pin
7			PD.9	I/O	General purpose input/output digital pin
8			PD.10	I/O	General purpose input/output digital pin
9			PD.11	I/O	General purpose input/output digital pin
10	6	4	PB.4	I/O	General purpose input/output digital pin
			RXD1	I	RXD1: Data receiver input pin for UART1
			SPISS11	I/O	SPISS11: SPI1 slave select pin (for QFN33 only)
11	7	5	PB.5	I/O	General purpose input/output digital pin
			TXD1	O	TXD1: Data transmitter output pin for UART1
12	8		PB.6	I/O	General purpose input/output digital pin
			RTS1	O	RTS1: Request to Send output pin for UART1
13	9		PB.7	I/O	General purpose input/output digital pin
			CTS1	I	CTS1: Clear to Send input pin for UART1
14	10	6	LDO	P	LDO output pin
15	11	7	VDD	P	Power supply for I/O ports and LDO source for internal PLL and digital function
16	12	8	VSS	P	Ground
17	13	9	VBUS	P	POWER SUPPLY: From USB Host or HUB.
18	14	10	VDD33	P	Internal Power Regulator Output 3.3 V Decoupling Pin

5.2.3 System Power Distribution

In this chip, the power distribution is divided into three segments.

- Analog power from AVDD and AVSS provides the power for analog components operation.
- Digital power from VDD and VSS supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.
- USB transceiver power from VBUS offers the power for operating the USB transceiver.

The outputs of internal voltage regulators, LDO and VDD33, require an external capacitor which should be located close to the corresponding pin. Analog power (AVDD) should be the same voltage level of the digital power (VDD). The following diagram shows the power distribution of this chip.

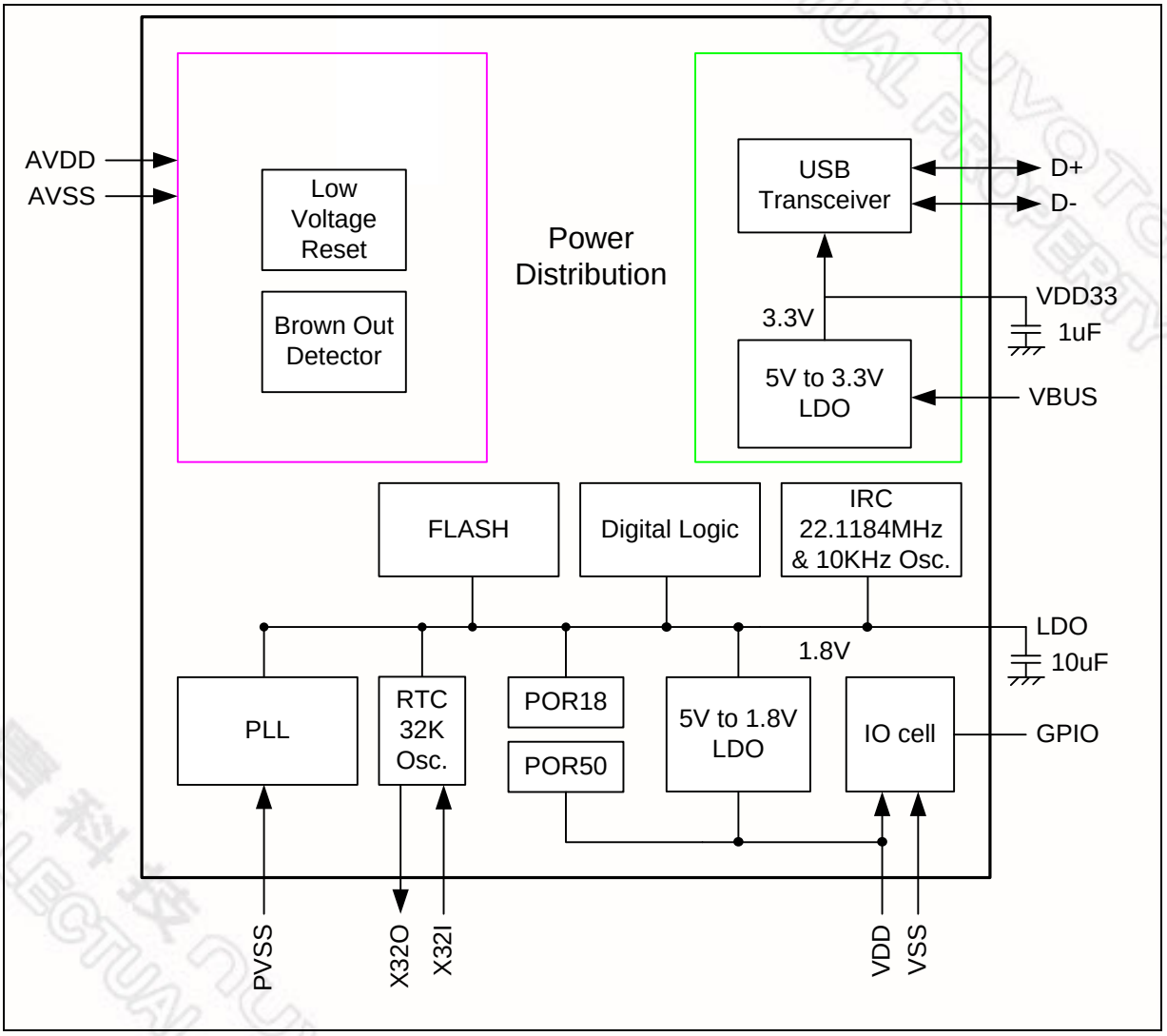


Figure 5-2 NuMicro™ NUC122 Power Distribution Diagram

5.3.3 System Clock & SysTick Clock

The system clock has 5 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is listed below.

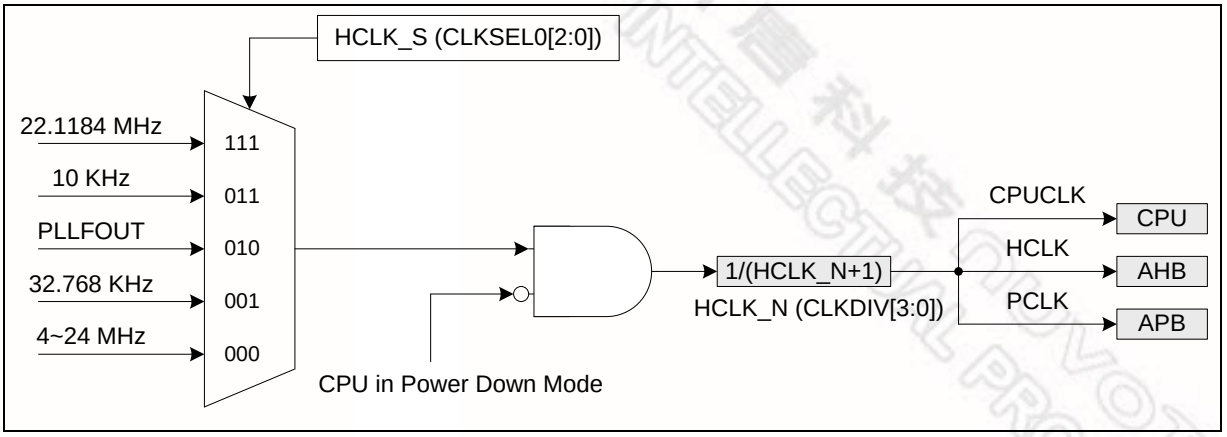


Figure 5-5 System Clock Block Diagram

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]. The block diagram is listed below.

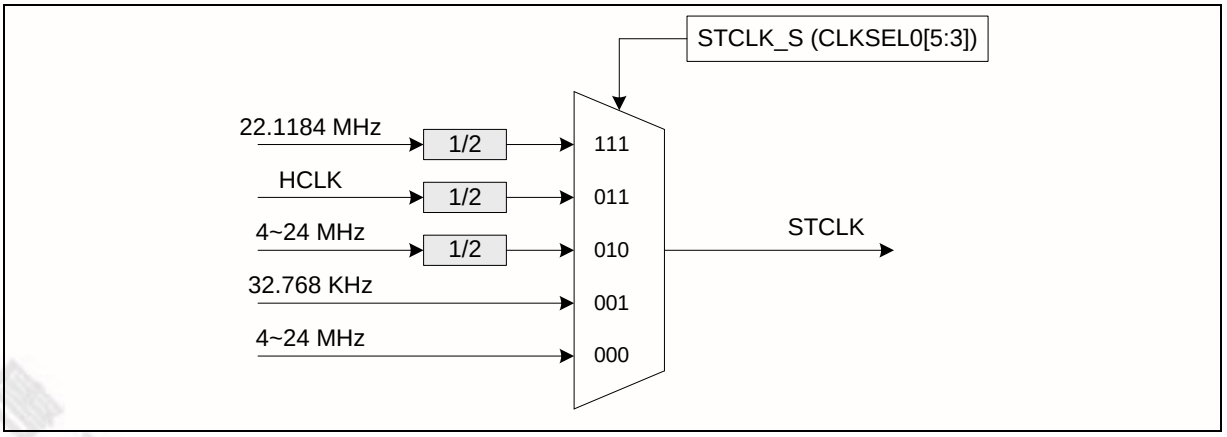


Figure 5-6 SysTick Clock Control Block Diagram

5.7 PWM Generator and Capture Timer (PWM)

5.7.1 Overview

NuMicro™ NUC122 only support 1 set of PWM group supports total 2 sets of PWM Generators which can be configured as 4 independent PWM outputs, PWM0~PWM3, or as 2 complementary PWM pairs, (PWM0, PWM1) and (PWM2, PWM3) with 2 programmable dead-zone generators.

Each PWM Generator has one 8-bit prescaler, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM down-counters for PWM period control, two 16-bit comparators for PWM duty control and one dead-zone generator. The 4 sets of PWM Generators provide eight independent PWM interrupt flags which are set by hardware when the corresponding PWM period down counter reaches zero. Each PWM interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

When PCR.DZEN01 is set, PWM0 and PWM1 perform complementary PWM paired function; the paired PWM period, duty and dead-time are determined by PWM0 timer and Dead-zone generator 0. Similarly, the complementary PWM pairs of (PWM2, PWM3), are controlled by PWM2, timer and Dead-zone generator 2. Refer to figures bellowed for the architecture of PWM Timers.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers the updated value will be load into the 16-bit down counter/ comparator at the time down counter reaching zero. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches zero, the interrupt request is generated. If PWM-timer is set as auto-reload mode, when the down counter reaches zero, it is reloaded with PWM Counter Register (CNRx) automatically then start decreasing, repeatedly. If the PWM-timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches zero.

The value of PWM counter comparator is used for pulse high width modulation. The counter control logic changes the output to high level when down-counter value matches the value of compare register.

The alternate feature of the PWM-timer is digital input Capture function. If Capture function is enabled the PWM output pin is switched as capture input mode. The Capture0 and PWM0 share one timer which is included in PWM0 and the Capture1 and PWM1 share PWM1 timer, and etc. Therefore user must setup the PWM-timer before enable Capture feature. After capture feature is enabled, the capture always latched PWM-counter to Capture Rising Latch Register (CRLR) when input channel has a rising transition and latched PWM-counter to Capture Falling Latch Register (CFLR) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CCR0.CRL_IE0[1] (Rising latch Interrupt enable) and CCR0.CFL_IE0[2]] (Falling latch Interrupt enable) to decide the condition of interrupt occur. Capture channel 1 has the same feature by setting CCR0.CRL_IE1[17] and CCR0.CFL_IE1[18]. And capture channel 2 to channel 3 on each group have the same feature by setting the corresponding control bits in CCR2. For each group, whenever Capture issues Interrupt 0/1/2/3, the PWM counter 0/1/2/3 will be reload at this moment.

The maximum captured frequency that PWM can capture is confined by the capture interrupt latency. When capture interrupt occurred, software will do at least three steps, they are: Read PIIRx to get interrupt source and Read CRLRx/CFLRx(x=0~3) to get capture value and finally write 1 to clear PIIRx to zero. If interrupt latency will take time T0 to finish, the capture signal mustn't transition during this interval (T0). In this case, the maximum capture frequency will be 1/T0. For example:

HCLK = 50 MHz, PWM_CLK = 25 MHz, Interrupt latency is 900 ns

So the maximum capture frequency will is 1/900 ns ≈ 1000 KHz

5.8 Watchdog Timer (WDT)

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports another function to wake-up chip from power down mode. The Watchdog Timer includes an 18-bit free running counter with programmable time-out intervals. Table 5-4 show the Watchdog Timer time-out interval selection and Figure 5-10 shows the timing of Watchdog interrupt signal and reset signal.

Setting WTE (WDTCR [7]) enables the watchdog timer and the WDT counter starts counting up. When the counter reaches the selected time-out interval, Watchdog timer interrupt flag WTIF will be set immediately to request a WDT interrupt if the watchdog timer interrupt enable bit WTIE is set, in the meanwhile, a specified delay time (1024 * T_{WDT}) follows the time-out event. User must set WTR (WDTCR [0]) (Watchdog timer reset) high to reset the 18-bit WDT counter to avoid chip from Watchdog timer reset before the delay time expires. WTR bit is cleared automatically by hardware after WDT counter is reset. There are eight time-out intervals with specific delay time which are selected by Watchdog timer interval select bits WTIS (WDTCR [10:8]). If the WDT counter has not been cleared after the specific delay time expires, the watchdog timer will set Watchdog Timer Reset Flag (WTRF) high and reset chip. This reset will last 63 WDT clocks (T_{RST}) then chip restarts executing program from reset vector (0x0000_0000). WTRF will not be cleared by Watchdog reset. User may poll WTRF by software to recognize the reset source. WDT also provides wake-up function. When chip is powered down and the Watchdog Timer Wake-up Function Enable bit (WDTR[4]) is set, if the WDT counter reaches the specific time interval defined by WTIS (WDTCR [10:8]) , the chip is woken-up from power down state. First example, if WTIS is set as 000, the specific time interval for chip to be woken-up from power down state is 2^4 * T_{WDT}. When power down command is set by software, then, chip enters power down state. After 2^4 * T_{WDT} time is elapsed, chip is woken-up from power down state. Second example, if WTIS (WDTCR [10:8]) is set as 111, the specific time interval for chip to be woken-up from power down state is 2^{18} * T_{WDT}. If power down command is set by software, then, chip enters power down state. After 2^{18} * T_{WDT} time is elapsed, chip is woken-up from power down state. Notice if WTRE (WDTCR [1]) is set to 1, after chip is woken-up, software should clear the Watchdog Timer counter by setting WTR(WDTCR [0]) to 1 as soon as possible. Otherwise, if the Watchdog Timer counter is not cleared by setting WTR (WDTCR [0]) to 1 before time starting from waking up to software clearing Watchdog Timer counter is over 1024 * T_{WDT} , the chip is reset by Watchdog Timer.

WTIS	Time-out Interval Selection T_{TIS}	Interrupt Period T_{INT}	WTR Time-out Interval (WDT_CLK=10 KHz) Min. T_{WTR} ~ Max. T_{WTR}
000	2^4 * T_{WDT}	1024 * T_{WDT}	1.6 ms ~ 104 ms
001	2^6 * T_{WDT}	1024 * T_{WDT}	6.4 ms ~ 108.8 ms
010	2^8 * T_{WDT}	1024 * T_{WDT}	25.6 ms ~ 128 ms
011	2^{10} * T_{WDT}	1024 * T_{WDT}	102.4 ms ~ 204.8 ms
100	2^{12} * T_{WDT}	1024 * T_{WDT}	409.6 ms ~ 512 ms
101	2^{14} * T_{WDT}	1024 * T_{WDT}	1.6384 s ~ 1.7408 s
110	2^{16} * T_{WDT}	1024 * T_{WDT}	6.5536 s ~ 6.656 s
111	2^{18} * T_{WDT}	1024 * T_{WDT}	26.2144 s ~ 26.3168 s

Table 5-4 Watchdog Timer Time-out Interval Selection

5.9 Real Time Clock (RTC)

5.9.1 Overview

Real Time Clock (RTC) controller provides user the real time and calendar message. The clock source of RTC is from an external 32.768 KHz low speed crystal connected at pins X32I and X32O (reference to pin descriptions) or from an external 32.768 KHz low speed oscillator output fed at pin X32I. The RTC controller provides the time message (second, minute, hour) in Time Loading Register (TLR) as well as calendar message (day, month, year) in Calendar Loading Register (CLR). The data message is expressed in BCD format. It also offers alarm function that user can preset the alarm time in Time Alarm Register (TAR) and alarm calendar in Calendar Alarm Register (CAR).

The RTC controller supports periodic Time Tick and Alarm Match interrupts. The periodic interrupt has 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second which are selected by TTR (TTR[2:0]). When RTC counter in TLR and CLR is equal to alarm setting time registers TAR and CAR, the alarm interrupt flag (RIIR.AIF) is set and the alarm interrupt is requested if the alarm interrupt is enabled (RIER.AIER=1). Both RTC Time Tick and Alarm Match can cause chip be woken-up from power down mode if wake-up function is enabled (TWKE (TTR[3])=1).

5.9.2 Features

- There is a time counter (second, minute, hour) and calendar counter (day, month, year) for user to check the time
- Alarm register (second, minute, hour, day, month, year)
- 12-hour or 24-hour mode is selectable
- Leap year compensation automatically
- Day of week counter
- Frequency compensate register (FCR)
- All time and calendar message is expressed in BCD code
- Support periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Support RTC Time Tick and Alarm Match interrupt
- Support wake-up chip from power down mode

5.12 I²C Serial Interface Controller (Master/Slave) (I²C)

5.12.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8 bits long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the following figure for more detail I²C BUS Timing.

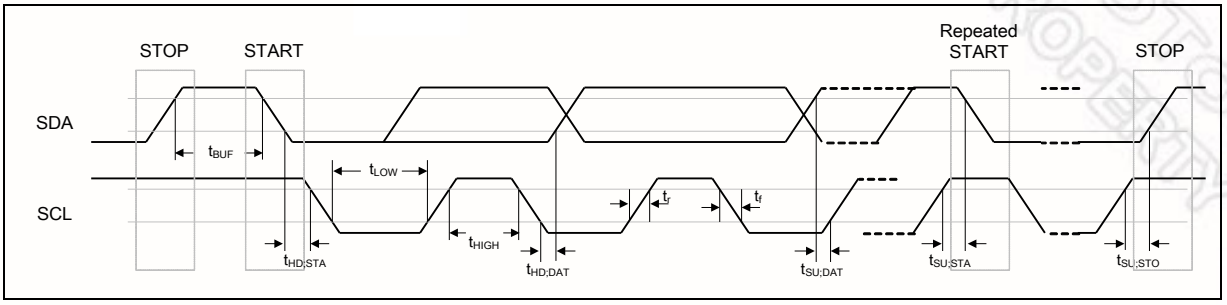


Figure 5-11 I²C Bus Timing

The device's on-chip I²C logic provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. To enable this port, the bit ENS1 in I2CON should be set to '1'. The I²C H/W interfaces to the I²C bus via two pins: SDA (PA10, serial data line) and SCL (PA11, serial clock line). Pull up resistor is needed for Pin PA10 and PA11 for I²C operation as these are open drain pins. When the I/O pins are used as I²C port, user must set the pins function to I²C in advance.

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus are:

- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Built-in a 14-bit time-out counter will request the I²C interrupt if the I²C bus hangs up and timer-out counter overflows.

5.13 Serial Peripheral Interface (SPI)

5.13.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol which operates in full duplex mode. Devices communicate in master/slave mode with 4-wire bi-direction interface. The NuMicro™ NUC122 contains up to two sets of SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each set of SPI controller can be set as a master that can drive up to 2 external peripheral slave devices; it also can be configured as a slave device controlled by an off-chip master device.

This controller also supports a variable serial clock for special application.

5.13.2 Features

- Up to two sets of SPI controller for NuMicro™ NUC122
- Support master or slave mode operation
- Support 1-bit transfer mode
- Configurable bit length up to 32 bits of a transfer word and configurable word numbers up to 2 of a transaction, so the maximum bit length is 64 bits for each data transfer
- Provide burst mode operation, transmit/receive can be transferred up to two times word transaction in one transfer
- Support MSB or LSB first transfer
- 2 device/slave select lines in master mode, but 1 device/slave select line in slave mode
- Support byte reorder in data register
- Support byte or word suspend mode
- Variable output serial clock frequency in master mode
- Support two programmable serial clock frequencies in master mode

6 ELECTRICAL CHARACTERISTICS

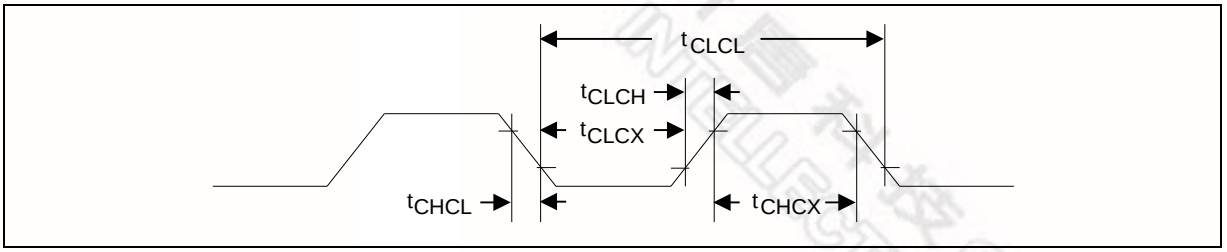
6.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into VDD		-	120	mA
Maximum Current out of VSS			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

6.3 AC Electrical Characteristics

6.3.1 External 4~24 MHz High Speed Crystal AC Electrical Characteristics



Note: Duty cycle is 50 %.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		20	-	-	nS
t_{CLCX}	Clock Low Time		20	-	-	nS
t_{CLCH}	Clock Rise Time		-	-	10	nS
t_{CHCL}	Clock Fall Time		-	-	10	nS

6.3.2 External 4~24 MHz High Speed Crystal

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	℃

6.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	without	without	without

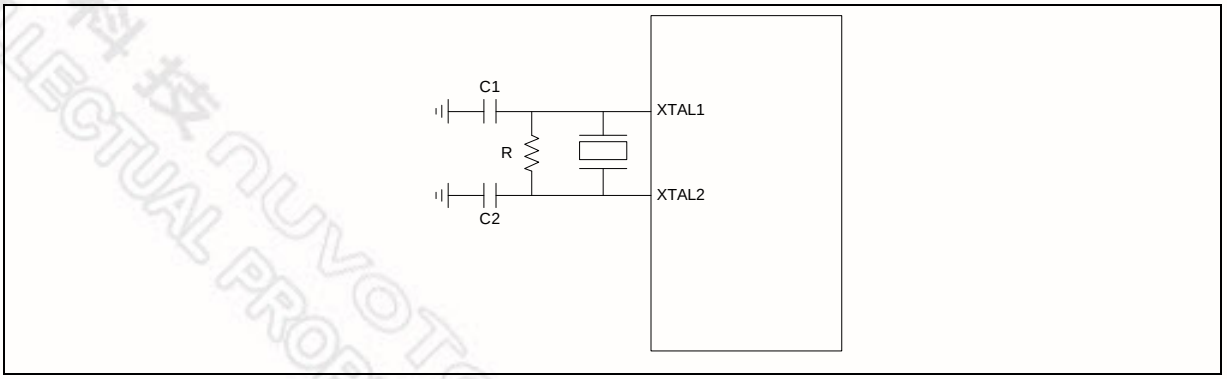


Figure 6-1 Typical Crystal Application Circuit

6.4 Analog Characteristics

6.4.1 Specification of LDO & Power management

PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
Input Voltage	2.5	5	5.5	V	V_{DD} input voltage
Output Voltage	1.6	1.8	2.1	V	$V_{DD} \geq 2.5$ V
Temperature	-40	25	85	℃	
Quiescent Current (PD=0)	-	100	-	μA	
Quiescent Current (PD=1)	-	5	-	μA	
Iload (PD=0)	-	-	100	mA	
Iload (PD=1)	-	-	100	μA	
Cbp	-	4.7	-	μF	Resr=1 ohm

Note:

1. It is recommended that a 10 μF or higher capacitor and a 100 nF bypass capacitor are connected between VDD and the closest VSS pin of the device.

2. For ensuring power stability, a 4.7 μF or higher capacitor must be connected between LDO pin and the closest VSS pin of the device.

6.4.5 Specification of USB PHY

6.4.5.1 USB DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input high (driven)		2.0			V
V_{IL}	Input low				0.8	V
V_{DI}	Differential input sensitivity	|PADP-PADM|	0.2			V
V_{CM}	Differential common-mode range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended receiver threshold		0.8		2.0	V
	Receiver hysteresis			200		mV
V_{OL}	Output low (driven)		0		0.3	V
V_{OH}	Output high (driven)		2.8		3.6	V
V_{CRS}	Output signal cross voltage		1.3		2.0	V
R_{PU}	Pull-up resistor		1.425		1.575	kΩ
R_{PD}	Pull-down resistor		14.25		15.75	kΩ
V_{TRM}	Termination Voltage for upstream port pull up (RPU)		3.0		3.6	V
Z_{DRV}	Driver output resistance	Steady state drive*		10		Ω
C_{IN}	Transceiver capacitance	Pin to GND			20	pF

*Driver output resistance doesn't include series resistor resistance.

6.4.5.2 USB Full-Speed Driver Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{FR}	Rise Time	C_L=50p	4		20	ns
T_{FF}	Fall Time	C_L=50p	4		20	ns
T_{FRFF}	Rise and fall time matching	$T_{FRFF}=T_{FR}/T_{FF}$	90		111.11	%

6.4.5.3 USB Power Dissipation

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{VDDREG} (Full Speed)	V_{DDD} and V_{DDREG} Supply Current (Steady State)	Standby		50		μA
		Input mode				μA
		Output mode				μA

6.5 SPI Dynamic Characteristics

6.5.1 Dynamic Characteristics of Data Input and Output Pin

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
SPI Master Mode (VDD = 4.5 V ~ 5.5 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	16	10	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	5	8	ns
SPI Master Mode (VDD = 3.0 V ~ 3.6 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	20	13	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	7	14	ns
SPI Slave Mode (VDD = 4.5 V ~ 5.5 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2*PCLK+4	-	-	ns
t_V	Data output valid time	-	2*PCLK+11	2*PCLK+20	ns
SPI Slave Mode (VDD = 3.0 V ~ 3.6 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2*PCLK+8	-	-	ns
t_V	Data output valid time	-	2*PCLK+20	2*PCLK+32	ns

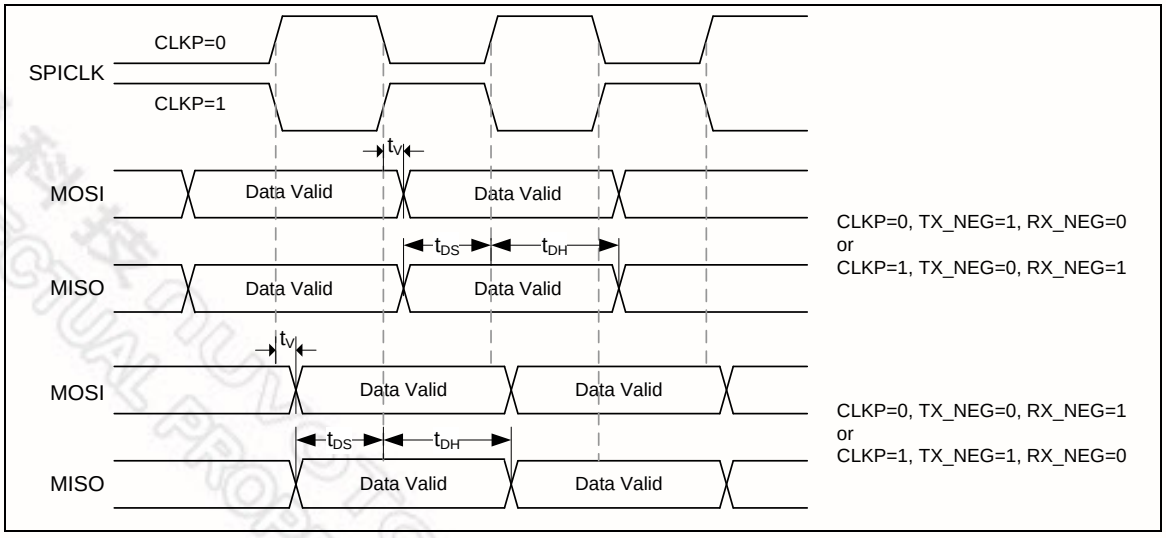
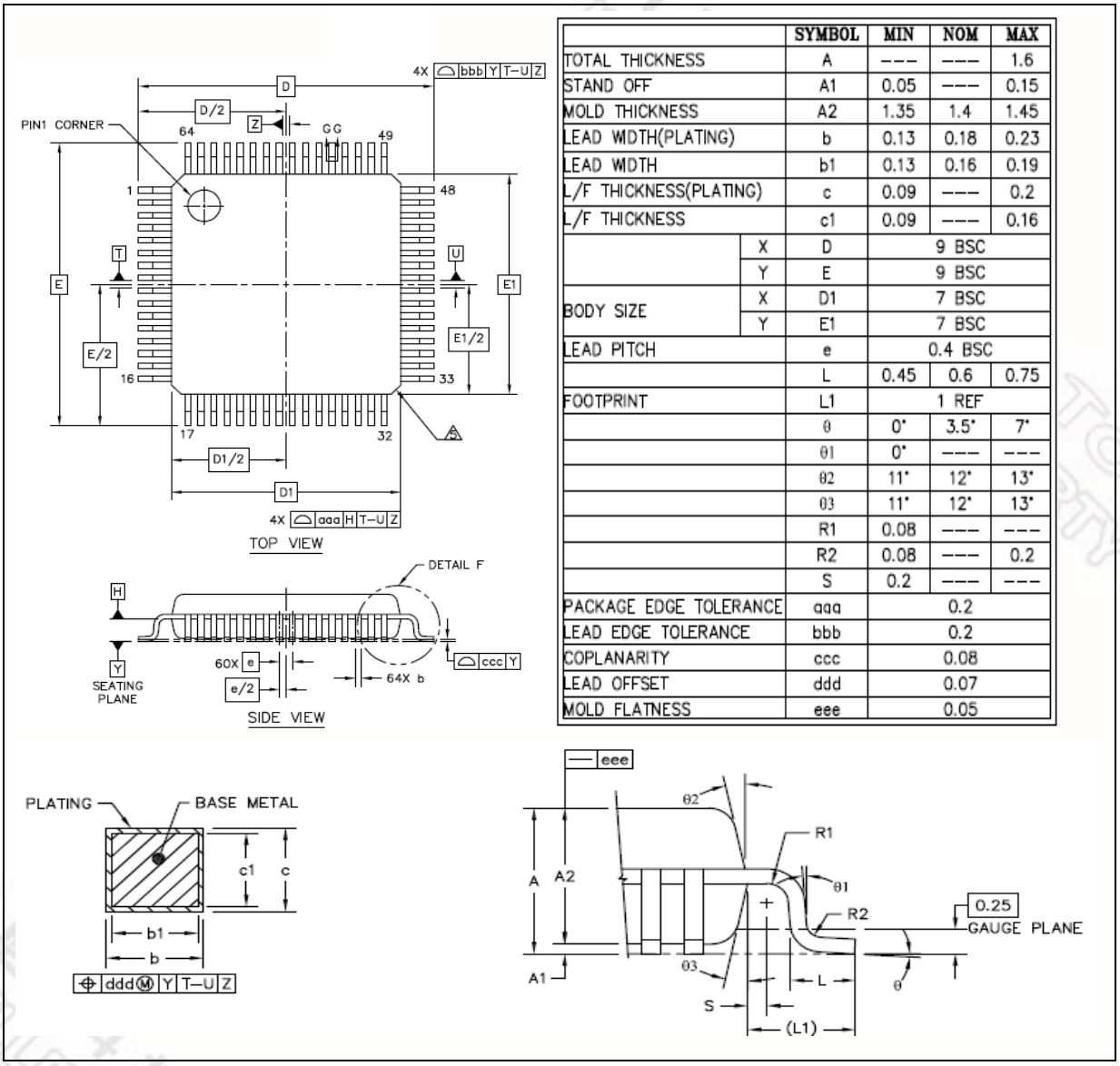


Figure 6-2 SPI Master Mode Timing

7 PACKAGE DIMENSIONS

7.1 64L LQFP (7x7x1.4mm footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

8 REVISION HISTORY

VERSION	DATE	PAGE/ CHAP.	DESCRIPTION
V1.00	Nov. 15, 2010	-	Preliminary version initial issued
V1.01	Dec. 7, 2010	Chap. 3	Corrected the Selection Guide Table for QFN33.
V1.02	Jan. 13, 2011	Chap. 5 Chap. 7	1. Corrected the Watchdog Timer Clock Source Selection 2. Corrected the Electrical Characteristics.
V1.03	March 14, 2011	Chap. 3 Chap. 7 Chap. 8	1. Added the LQFP 64-pin part number for 7x7x1.4mm package. (NUC122SD2AN, NUC122SC1AN) 2. Corrected the LQFP 64-pin Pin Diagram. 3. Updated DC and AC Electrical Characteristics and added the SPI Dynamic Characteristics. 4. Updated LQFN 48-pin package dimensions.
V1.04	March 31, 2011	Chap. 2 Chap. 3 Chap. 4 Chap. 5 Chap. 8	1. Removed the LQFP 64-pin part number for 10x10x1.4mm package. 2. Replaced “12 MHz” with “4~24 MHz” in some contents and block diagrams.
V1.05	Apr.29 , 2011	Chap. 1 Chap. 2 Chap. 3 Chap. 5 Chap. 7	1. Updated the table of specification of LDO and Power Management. 2. Removed the LIN function from UART controller. 3. Corrected the “PWM_CRLx/PWM_CFLx(x=0~3)” to “CRLRx/CFLRx(x=0~3)” in the Overview of PWM Generator and Capture Timer chapter. 4. Corrected the “1xx” to “111” in System Clock and SysTick Clock Control Block Diagram. 5. Added the Clock Generator Global View Diagram. 6. Corrected the “RX0/1” and “TX0/1” to “RXD0/1” and “TXD0/1” in Pin Configuration and Pin Description.
V1.06	May 30, 2011	Chap. 3 All	1. Corrected the Pin Description of pins 17 and 18 for LQFP 48-pin. 2. Corrected the typo of Year on the Footer.
V1.07	June 8, 2011	Chap. 2 Chap. 7	1. Corrected the trimmed condition for the internal 22.1184 MHz high speed oscillator in the “Clock Control” item of Feature list. 2. Corrected the specification of the “Internal 22.1184 MHz High Speed Oscillator”.
V1.08	June 21, 2011	Chap. 2	1. Added the condition and corrected the speed of SPI in Master/Slave mode in the “SPI” item of Feature list.
V1.09	May 16, 2014	Chap. 3 Chap. 8	1. Added the PF.2 and PF.3 function on PS2DAT and PS2CLK in Pin Diagram and Pin Description. 2. Corrected QFN33 package dimension.
V1.10	Dec. 22, 2014	Chap. 5	1. Corrected the 5.9.2 Features of SPI. 2. Rearranged the chapter 5 session sequence.

V1.11	Jan. 09, 2015	Chap. 2 Chap. 5	1. Corrected the UART FIFO to 14-byte. 2. Removed the GPIO PF.2 and PF.3 from Pin Diagram and Pin Description.