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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	740
Core Size	8-Bit
Speed	12.5MHz
Connectivity	SIO, UART/USART
Peripherals	LCD, LED, PWM, WDT
Number of I/O	51
Program Memory Size	16KB (16K x 8)
Program Memory Type	QzROM
EEPROM Size	-
RAM Size	640 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m38d24g4fp-u0

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Table 1 Performance overview

Parameter			Function
Number of basic instructions			71
Instruction execution time			0.32 μs (Minimum instruction, Oscillation frequency 12.5 MHz)
Oscillation frequency			16 MHz (Maximum)(1)
Memory sizes (QzROM version)	ROM		16 K to 60 K bytes
	RAM		640 to 2048 bytes
Memory sizes (Flash memory version)	ROM		60 K bytes
	RAM		2048 bytes
I/O port	P0-P5, P60-P62		8-bit × 6, 3-bit × 1 (24 pins sharing SEG)
Interrupt			18 sources, 16 vectors (includes key input interrupt)
Timer			8-bit × 4, 16-bit × 2
Serial Interface			8-bit × 2 (UART or Clock-synchronized)
PWM			10-bit × 2, 16-bit × 1 (common to IGBT output)
A/D converter			10-bit × 8 (operated in low-speed mode)
Watchdog timer			8-bit × 1
ROM correction function			32 bytes × 2 vectors
LED direct drive port			8 (average current: 15 mA, peak current: 30 mA, total current: 90 mA)
LCD drive control circuit	Bias		1/2, 1/3
	Duty		2, 3, 4
	Common output		4
	Segment output		24
Main clock generating circuits			Built-in (connect to external ceramic resonator or on-chip oscillator)
Sub-clock generating circuits			Built-in (connect to external quartz-crystal oscillator)
Power source voltage (QzROM version)	In frequency/2 mode (1)	f(XIN) ≤ 12.5 MHz	4.5 to 5.5 V
		f(XIN) ≤ 8 MHz	4.0 to 5.5 V
		f(XIN) ≤ 4 MHz	2.0 to 5.5 V
		f(XIN) ≤ 2 MHz	1.8 to 5.5 V
	In frequency/4 mode	f(XIN) ≤ 16 MHz	4.5 to 5.5 V
		f(XIN) ≤ 8 MHz	2.0 to 5.5 V
		f(XIN) ≤ 4 MHz	1.8 to 5.5 V
	In frequency/8 mode	f(XIN) ≤ 16 MHz	4.5 to 5.5 V
		f(XIN) ≤ 8 MHz	2.0 to 5.5 V
		f(XIN) ≤ 4 MHz	1.8 to 5.5 V
	In low-speed mode		1.8 to 5.5 V
Power source voltage (Flash memory version)	In frequency/2 mode (1)	f(XIN) ≤ 12.5 MHz	4.5 to 5.5 V
		f(XIN) ≤ 8 MHz	4.0 to 5.5 V
		f(XIN) ≤ 4 MHz	2.7 to 5.5 V
	In frequency/4 mode	f(XIN) ≤ 16 MHz	4.5 to 5.5 V
		f(XIN) ≤ 8 MHz	2.7 to 5.5 V
	In frequency/8 mode	f(XIN) ≤ 16 MHz	4.5 to 5.5 V
		f(XIN) ≤ 8 MHz	2.7 to 5.5 V
	In low-speed mode		2.7 to 5.5 V
Power dissipation (QzROM version)	In frequency/2 mode		Std. 32 mW (Vcc = 5 V, f(XIN) = 12.5 MHz, Ta = 25°C)
	In low-speed mode		Std. 18 μW (Vcc = 2.5 V, f(XIN) = stop, f(XCIN) = 32 kHz, Ta = 25°C)
Power dissipation (Flash memory version)	In frequency/2 mode		Std. 20 mW (Vcc = 5 V, f(XIN) = 12.5 MHz, Ta = 25°C)
	In low-speed mode		Std. 1.1 mW (Vcc = 2.7 V, f(XIN) = stop, f(XCIN) = 32 kHz, Ta = 25°C)
Input/Output characteristics	Input/Output withstand voltage		VCC
	Output current		10 mA
Operating temperature range			-20 to 85°C
Device structure			CMOS silicon gate
Package			64-pin plastic molded LQFP

NOTE:
1. 12.5 MHz < f(XIN) ≤ 16 MHz is not available in the frequency/2 mode.

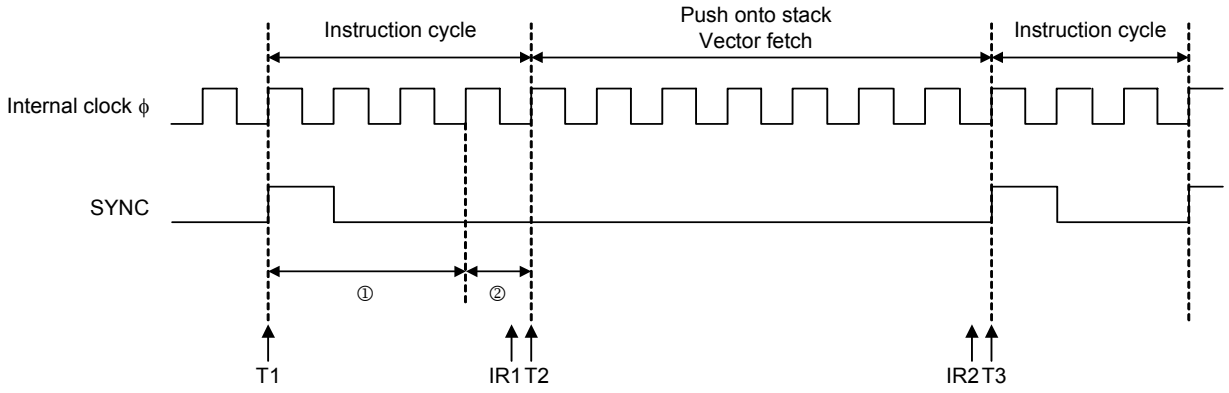
<Notes>

The interrupt request bit may be set to "1" in the following cases.

- When setting the external interrupt active edge
  Related bits: INT_0 interrupt edge selection bit
  (bit 0 of interrupt edge selection register
  (address $003A_{16}$))
  INT_1 interrupt edge selection bit
  (bit 1 of interrupt edge selection register)
  INT_2 interrupt edge selection bit
  (bit 2 of interrupt edge selection register)
  $CNTR_0$ activate edge switch bit
  (bits 6 and 7 of timer X control register 1
  (address $002E_{16}$))
  $CNTR_1$ activate edge switch bit
  (bits 6 of timer Y mode register
  (address 0038_{16}))
- When switching the interrupt sources of an interrupt vector address where two or more interrupt sources are assigned
  Related bit: Timer Y/$CNTR_1$ interrupt switch bit
  (bit 3 of interrupt edge selection register)

If it is not necessary to generate an interrupt synchronized with these settings, take the following sequence.

(1) Set the corresponding enable bit to "0" (disabled).
(2) Set the interrupt edge selection bit (the active edge switch bit) or the interrupt source bit.
(3) Set the corresponding interrupt request bit to "0" after one or more instructions have been executed.
(4) Set the corresponding interrupt enable bit to "1" (enabled).



T1 T2 T3 : Interrupt acceptance timing points
IR1 IR2 : Timings points at which the interrupt request bit is set to "1".

Note : Period 2 indicates the last φ cycle during one instruction cycle.

(1) The interrupt request bit for an interrupt request generated during period 1 is set to "1" at timing point IR1.
(2) The interrupt request bit for an interrupt request generated during period 2 is set to "1" at timing point IR1 or IR2. The timing point at which the bit is set to "1" varies depending on conditions. When two or more interrupt requests are generated during the period 2, each request bit may be set to "1" at timing point IR1 or IR2 separately.

Fig. 20 Timing of interrupt request generation, interrupt request bit, and interrupt acceptance

SERIAL INTERFACE

• SERIAL I/O

The 38D2 Group has two 8-bit serial I/O (serial I/O1 and serial I/O2).

Serial I/O can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O mode can be selected by setting the serial I/O mode selection bit of the serial I/O control register to "1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

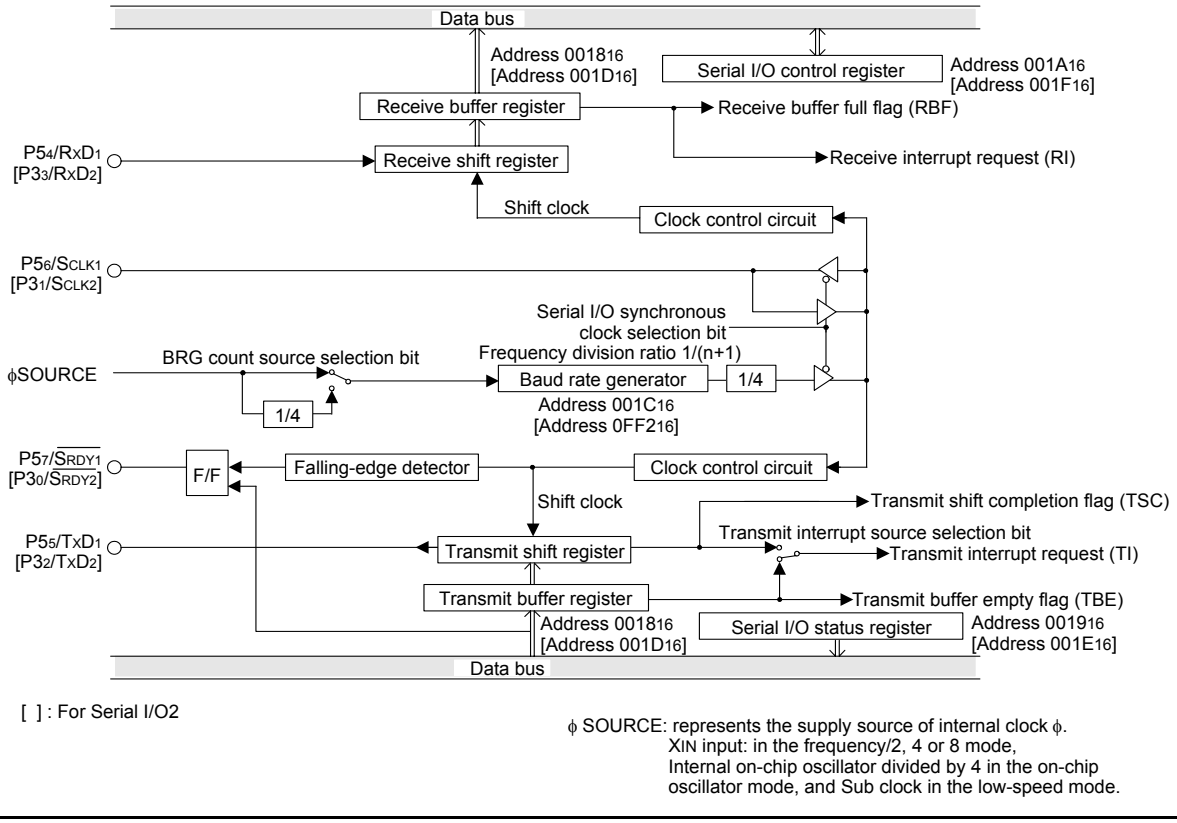
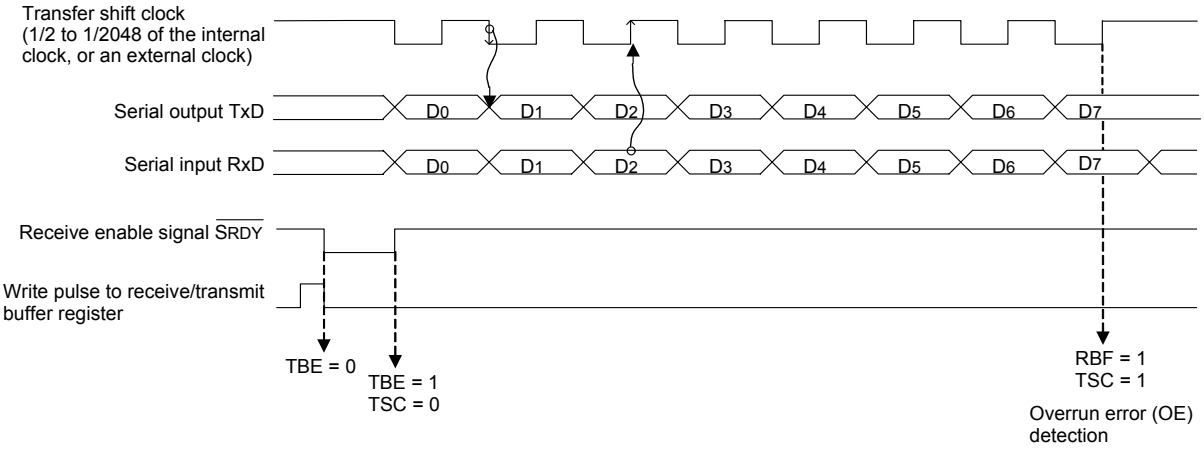


Fig. 31 Block diagram of clock synchronous serial I/O



Notes 1: As the transmit interrupt (TI) source, which can be selected, either when the transmit buffer has emptied (TBE = 1) or after the transmit shift operation has ended (TSC = 1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O control register.

2: If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.

3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1" .

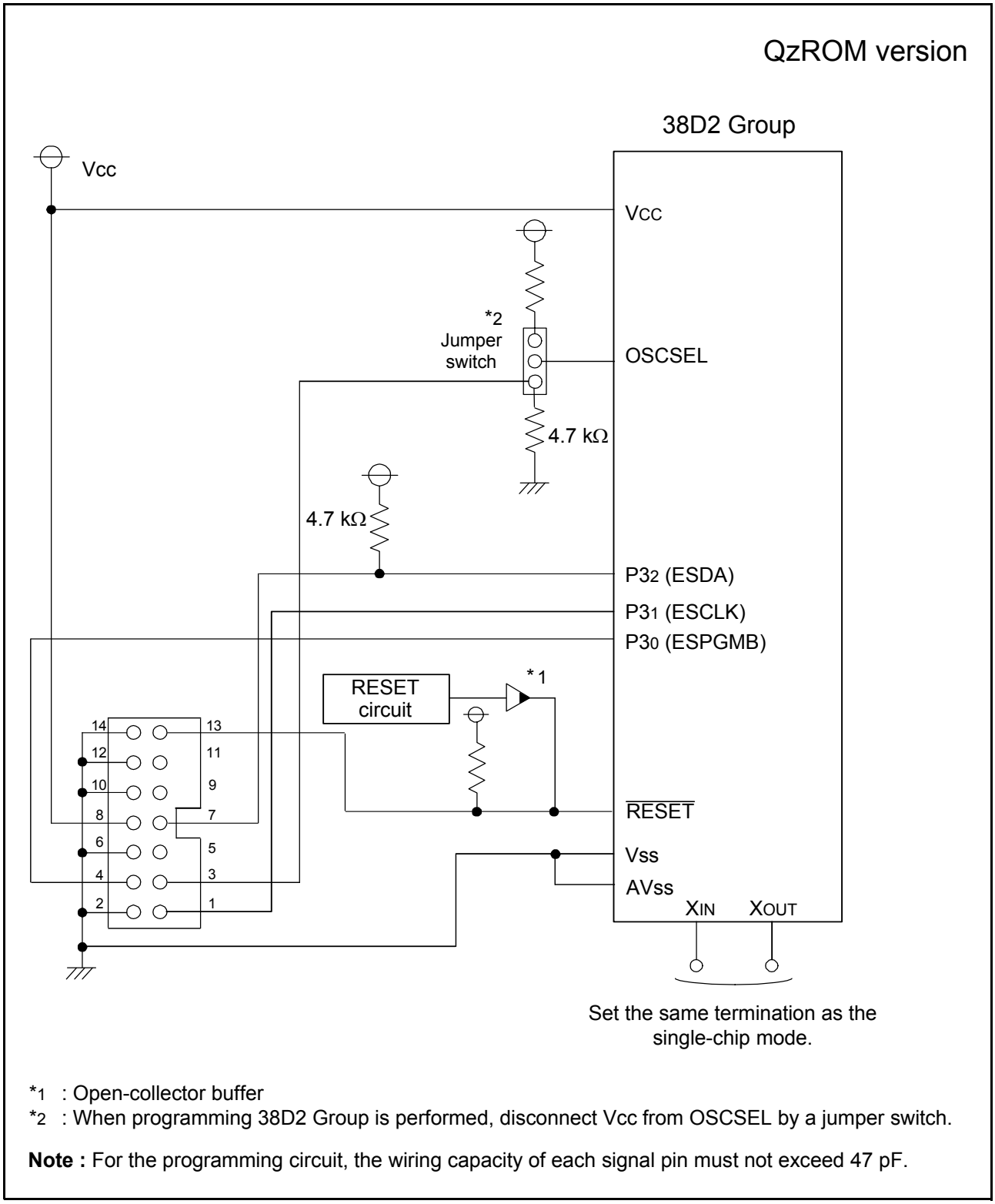
Fig. 32 Operation of clock synchronous serial I/O function

QzROM WRITING MODE

In the QzROM writing mode, the user ROM area can be rewritten while the microcomputer is mounted on-board by using a serial programmer which is applicable for this microcomputer.
Table 14 lists the pin description (QzROM writing mode) and Figure 65 shows the pin connection.
Refer to Figure 66 to Figure 69 for examples of a connection with a serial programmer.
Contact the manufacturer of your serial programmer for serial programmer. Refer to the user's manual of your serial programmer for details on how to use it.

Table 14 Pin description (QzROM writing mode)

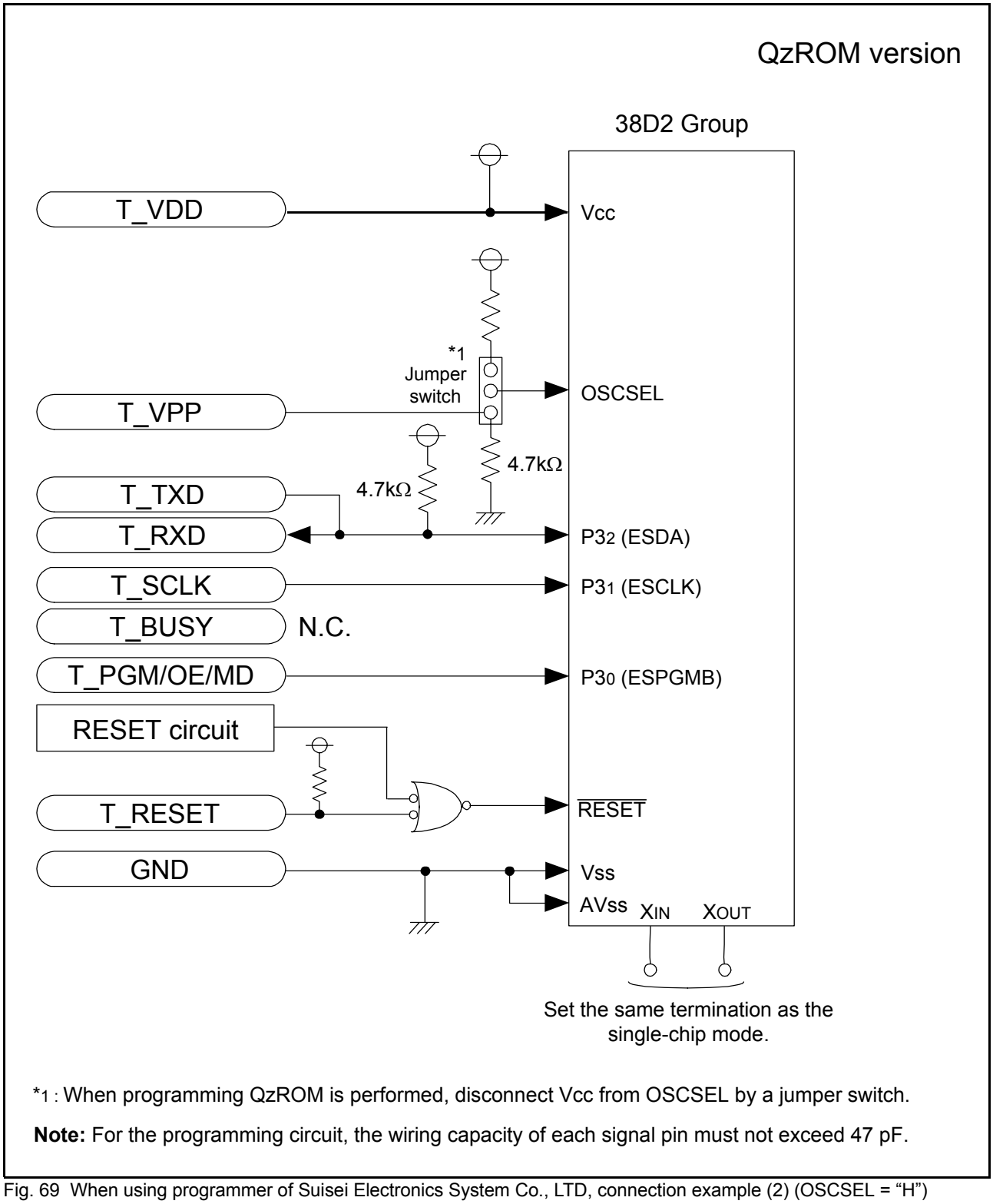
Pin	Name	I/O	Function
V_{CC}, V_{SS}	Power source	Input	• Apply 2.7 to 5.5 V to V_{CC}, and 0 V to V_{SS}.
$\overline{RESET}$	Reset input	Input	• Reset input pin for active "L". Reset occurs when $\overline{RESET}$ pin is held at an "L" level for 16 cycles or more of X_{IN}.
X_{IN}	Clock input	Input	• Set the same termination as the single-chip mode.
X_{OUT}	Clock output	Output	
V_{REF}	Analog reference voltage	Input	• Input the reference voltage of A/D converter to V_{REF}.
AVss	Analog power source	Input	• Connect AVss to Vss.
$P0_0$–$P0_7$ $P1_0$–$P1_7$ $P2_0$–$P2_7$ $P3_3$–$P3_7$ $P4_0$–$P4_7$ $P5_0$–$P5_7$ $P6_0$–$P6_2$	I/O port	I/O	• Input "H" or "L" level signal or leave the pin open.
OSCSEL	V_{PP} input	Input	• QzROM programmable power source pin.
$P3_2$	ESDA input/output	I/O	• Serial data I/O pin.
$P3_1$	ESCLK input	Input	• Serial clock input pin.
$P3_0$	ESPGMB input	Input	• Read/program pulse input pin.



*1 : Open-collector buffer
*2 : When programming 38D2 Group is performed, disconnect Vcc from OSCSEL by a jumper switch.

Note : For the programming circuit, the wiring capacity of each signal pin must not exceed 47 pF.

Fig. 67 When using E8 programmer, connection example (2) (OSCSEL = "H")



*1 : When programming QzROM is performed, disconnect Vcc from OSCSEL by a jumper switch.

Note: For the programming circuit, the wiring capacity of each signal pin must not exceed 47 pF.

Fig. 69 When using programmer of Suisei Electronics System Co., LTD, connection example (2) (OSCSEL = “H”)

Outline Performance

CPU rewrite mode is usable in the single-chip or Boot mode. The only User ROM area can be rewritten.
In CPU rewrite mode, the CPU erases, programs and reads the internal flash memory as instructed by software commands. This rewrite control program must be transferred to internal RAM area before it can be executed.
The MCU enters CPU rewrite mode by setting "1" to the CPU rewrite mode select bit (bit 1 of address 0FE0$_{16}$). Then, software commands can be accepted.
Use software commands to control program and erase operations. Whether a program or erase operation has terminated normally or in error can be verified by reading the status register.
Figure 71 shows the flash memory control register 0.
Bit 0 of the flash memory control register 0 is the RY/$\overline{\text{BY}}$ status flag used exclusively to read the operating status of the flash memory. During programming and erase operations, it is "0" (busy). Otherwise, it is "1" (ready).
Bit 1 of the flash memory control register 0 is the CPU rewrite mode select bit. When this bit is set to "1", the MCU enters CPU rewrite mode. And then, software commands can be accepted. In CPU rewrite mode, the CPU becomes unable to access the internal flash memory directly. Therefore, use the control program in the internal RAM for write to bit 1. To set this bit 1 to "1", it is necessary to write "0" and then write "1" in succession to bit 1. The bit can be set to "0" by only writing "0".
Bit 2 of the flash memory control register 0 is the user block 1 E/W enable bit. By setting combination of bit 4 (user block 0 E/W enable bit) of the flash memory control register 2 (address 0FE2$_{16}$) and this bit as shown in Table 16, E/W is disabled to user block in the CPU rewriting mode.
Bit 3 of the flash memory control register 0 is the flash memory reset bit used to reset the control circuit of internal flash memory. This bit is used when flash memory access has failed. When the CPU rewrite mode select bit is "1", setting "1" for this bit resets the control circuit. To release the reset, it is necessary to set this bit to "0".
Bit 5 of the flash memory control register 0 is the User ROM area select bit and is valid only in the boot mode. Setting this bit to "1" in the boot mode switches an accessible area from the boot ROM area to the user ROM area. To use the CPU rewrite mode in the boot mode, set this bit to "1". To rewrite bit 5, execute the user original reprogramming control software transferred to the internal RAM in advance.
Bit 6 of the flash memory control register 0 is the program status flag. This bit is set to "1" when writing to flash memory is failed. When program error occurs, the block cannot be used.
Bit 7 of the flash memory control register 0 is the erase status flag.
This bit is set to "1" when erasing flash memory is failed. When erase error occurs, the block cannot be used.
Figure 72 shows the flash memory control register 1.
Bit 0 of the flash memory control register 1 is the Erase suspend enable bit. By setting this bit to "1", the erase suspend mode to suspend erase processing temporary when block erase command is executed can be used. In order to set this bit 0 to "1", writing "0" and "1" in succession to bit 0. In order to set this bit to "0", write "0" only to bit 0.
Bit 1 of the flash memory control register 1 is the erase suspend request bit. By setting this bit to "1" when erase suspend enable bit is "1", the erase processing is suspended.
Bit 6 of the flash memory control register 1 is the erase suspend flag. This bit is cleared to "0" at the flash erasing.

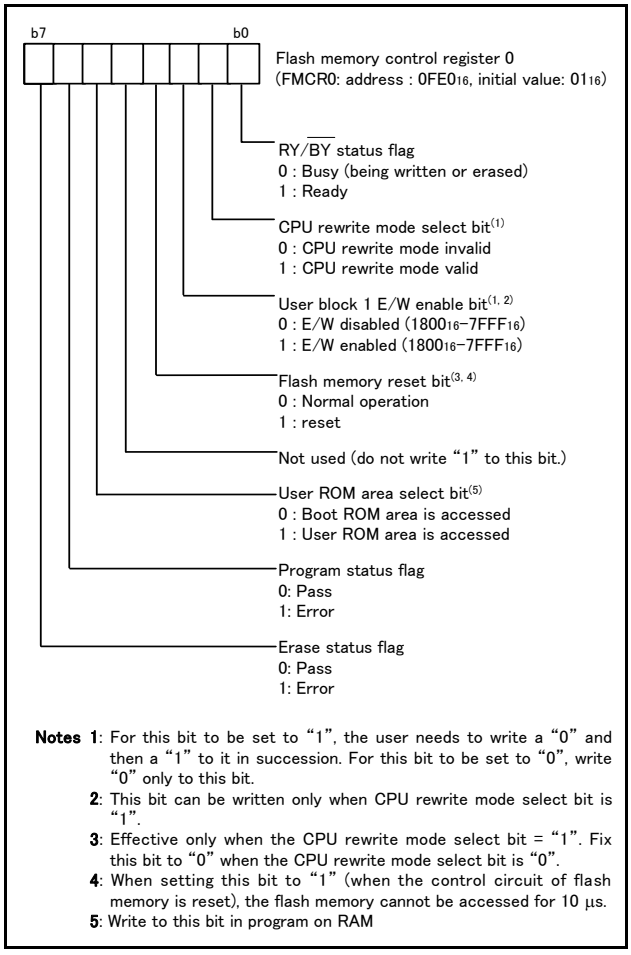


Fig 71. Structure of flash memory control register 0

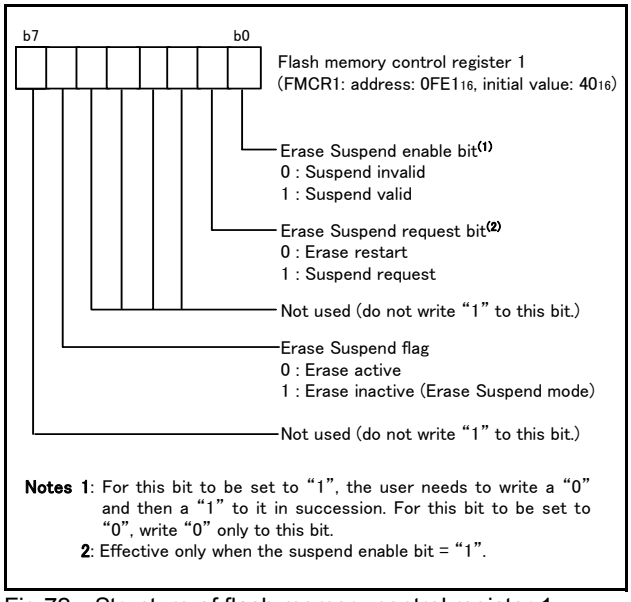


Fig 72. Structure of flash memory control register 1

Software Commands

Table 17 lists the software commands.
After setting the CPU rewrite mode select bit to "1", execute a software command to specify an erase or program operation.
Each software command is explained below.

• Read Array Command (FF_{16})
The read array mode is entered by writing the command code "FF_{16}" in the first bus cycle. When an address to be read is input in one of the bus cycles that follow, the contents of the specified address are read out at the data bus (D_0 to D_7).
The read array mode is retained until another command is written.

• Read Status Register Command (70_{16})
When the command code "70_{16}" is written in the first bus cycle, the contents of the status register are read out at the data bus (D_0 to D_7) by a read in the second bus cycle.
The status register is explained in the next section.

• Clear Status Register Command (50_{16})
This command is used to clear the bits SR4 and SR5 of the status register after they have been set. These bits indicate that operation has ended in an error. To use this command, write the command code "50_{16}" in the first bus cycle.

• Program Command (40_{16})
Program operation starts when the command code "40_{16}" is written in the first bus cycle. Then, if the address and data to program are written in the 2nd bus cycle, program operation (data programming and verification) will start.
Whether the write operation is completed can be confirmed by read status register or the RY/$\overline{BY}$ status flag. To read the status register, write the read status register command "70_{16}". The status register bit 7 (SR7) is set to "0" at the same time the program starts and returned to "1" upon completion of the program. The read status mode remains active until the read array command ("FF_{16}") is written.

The RY/$\overline{BY}$ status flag is set to "0" during program operation and "1" when the program operation is completed as is the status register bit 7 (SR7).
At program end, program results can be checked by reading the status register.

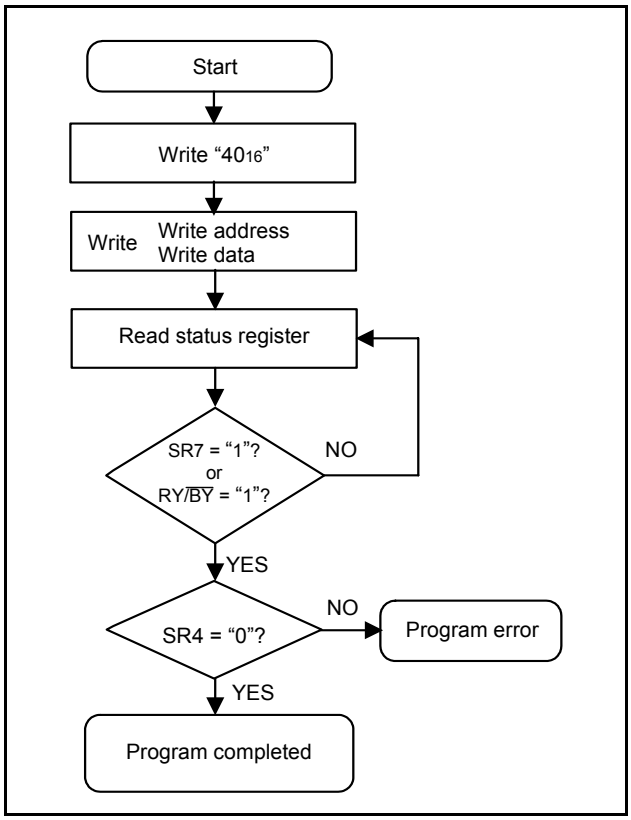


Fig 75. Program flowchart

Table 17 List of software commands (CPU rewrite mode)

Command	cycle number	First bus cycle			Second bus cycle		
		Mode	Address	Data (D_0 to D_7)	Mode	Address	Data (D_0 to D_7)
Read array	1	Write	X(4)	FF_{16}			
Read status register	2	Write	X	70_{16}	Read	X	SRD(1)
Clear status register	1	Write	X	50_{16}			
Program	2	Write	X	40_{16}	Write	WA(2)	WD(2)
Block erase	2	Write	X	20_{16}	Write	BA(3)	$D0_{16}$

NOTES:
1. SRD = Status Register Data
2. WA = Write Address, WD = Write Data
3. BA = Block Address to be erased (Input the maximum address of each block.)
4. X denotes a given address in the User ROM area.

• ID Code Check Function

Use this function in standard serial I/O mode. When the contents of the flash memory are not blank, the ID code sent from the programmer is compared with the ID code written in the flash memory to see if they match. If the ID codes do not match, the commands sent from the programmer are not accepted. The ID code consists of 8-bit data, and its areas are FFD4$_{16}$ to FFDA$_{16}$. Write a program which has had the ID code preset at these addresses to the flash memory.

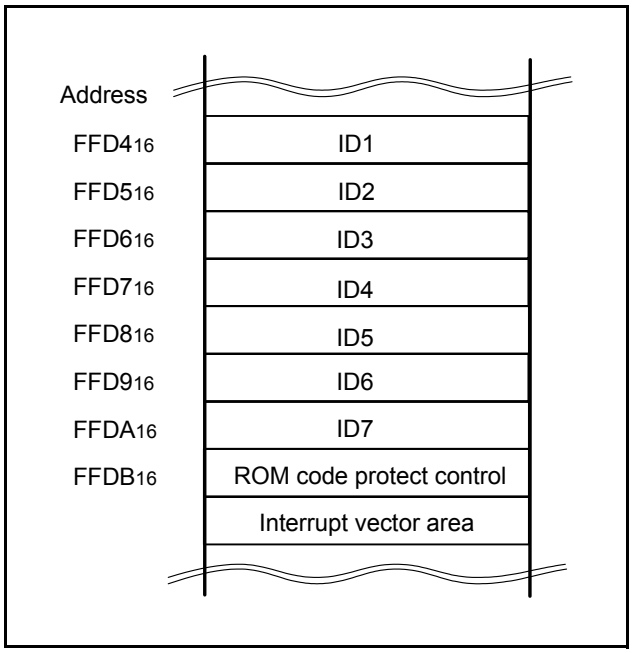


Fig 79. ID code store addresses

Standard serial I/O Mode

The standard serial I/O mode inputs and outputs the software commands, addresses and data needed to operate (read, program, erase, etc.) the internal flash memory. This I/O is clock synchronized serial. This mode requires a purpose-specific peripheral unit.

The standard serial I/O mode is different from the parallel I/O mode in that the CPU controls flash memory rewrite (uses the CPU rewrite mode), rewrite data input and so forth. The standard serial I/O mode is started by connecting "H" to the CNVSS pin and "H" to the P32 (BOOTENT) pin, and releasing the reset operation. (In the ordinary microcomputer mode, set CNVSS pin to "L" level.) This control program is written in the Boot ROM area when the product is shipped from Renesas. Accordingly, make note of the fact that the standard serial I/O mode cannot be used if the Boot ROM area is rewritten in parallel I/O mode. The standard serial I/ O mode has standard serial I/O mode 1 of the clock synchronous serial and standard serial I/O mode 2 of the clock asynchronous serial. Tables 19 and 20 show description of pin function (standard serial I/O mode). Figure 80 to 82 show the pin connections for the standard serial I/O mode.

In standard serial I/O mode, only the User ROM area shown in Figure 70 can be rewritten. The Boot ROM area cannot be written.

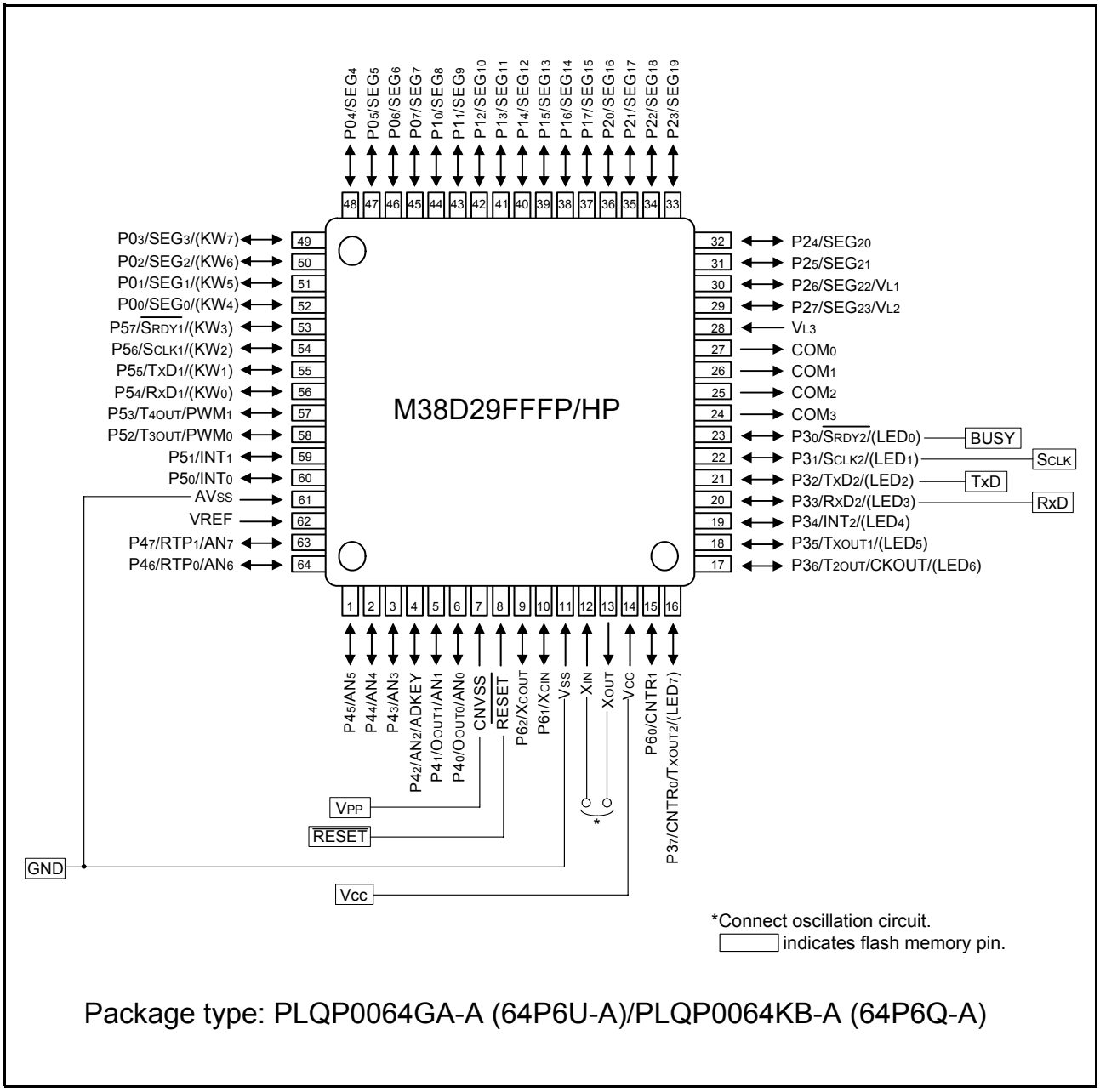
In standard serial I/O mode, a 7-byte ID code is used. When there is data in the flash memory, this function determines whether the ID code sent from the peripheral unit (programmer) and those written in the flash memory match. The commands sent from the peripheral unit (programmer) are not accepted unless the ID code matches.

Table 19 Description of pin function (Flash Memory Standard Serial I/O Mode 1)

Pin name	Signal name	I/O	Function
V_{CC},V_{SS}	Power supply	I	Apply 2.7 to 5.5 V to the V_{CC} pin and 0 V to the Vss pin.
CNV$_{SS}$	CNV$_{SS}$	I	After input of port is set, input “H” level.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin. To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an “L” level for 16 cycles or more of X_{IN}.
X_{IN}	Clock input	I	Connect an oscillation circuit between the X_{IN} and X_{OUT} pins. As for the connection method, refer to the “clock generating circuit”.
X_{OUT}	Clock output	O	
AV$_{SS}$	Analog power supply input		Connect AVss to V_{SS}.
V_{REF}	Reference voltage input	I	Apply reference voltage of A/D convertor to this pin.
$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_4$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$	I/O port	I/O	Input “L” or “H” level, or keep open.
$P3_3$	RxD input	I	Serial data input pin.
$P3_2$	TxD output	O	Serial data output pin.
$P3_1$	S_{CLK} input	I	Serial clock input pin.
$P3_0$	BUSY output	O	BUSY signal output pin.

Table 20 Description of pin function (Flash Memory Standard Serial I/O Mode 2)

Pin name	Signal name	I/O	Function
V_{CC},V_{SS}	Power supply	I	Apply 2.7 to 5.5 V to the Vcc pin and 0 V to the V_{SS} pin.
CNV$_{SS}$	CNV$_{SS}$	I	After input of port is set, input “H” level.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin. To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an “L” level for 16 cycles or more of X_{IN}.
X_{IN}	Clock input	I	Connect an oscillation circuit between the X_{IN} and X_{OUT} pins. As for the connection method, refer to the “clock generating circuit”.
X_{OUT}	Clock output	O	
AV$_{SS}$	Analog power supply input		Connect AVss to V_{SS}.
V_{REF}	Reference voltage input	I	Apply reference voltage of A/D convertor to this pin.
$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_4$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$	I/O port	I/O	Input “L” or “H” level, or keep open.
$P3_3$	RxD input	I	Serial data input pin.
$P3_2$	TxD output	O	Serial data output pin.
$P3_1$	S_{CLK} input	I	Input “L” level.
$P3_0$	BUSY output	O	BUSY signal output pin.



Package type: PLQP0064GA-A (64P6U-A)/PLQP0064KB-A (64P6Q-A)

Fig 80. Connection for standard serial I/O mode 1

Table 23 Recommended operating conditions (3)
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = −20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current (1) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			−40	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current (1) $P4_0$–4_7, $P5_0$–$P5_7$, $P6_0$–$P6_2$			−40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current (1) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$			40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current (1) $P4_0$–$P4_7$, $P5_0$, $P5_1$, $P5_4$–$P5_7$, $P6_0$–$P6_2$			40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current (1) $P3_0$–$P3_7$, $P5_2$, $P5_3$			110	mA
$\Sigma I_{OH(avg)}$	"H" total average output current (1) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			−20	mA
$\Sigma I_{OH(avg)}$	"H" total average output current (1) $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$			−20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current (1) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$			20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current (1) $P4_0$–$P4_7$, $P5_0$, $P5_1$, $P5_4$–$P5_7$, $P6_0$–$P6_2$			20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current (1) $P3_0$–$P3_7$, $P5_2$, $P5_3$			90	mA
$I_{OH(peak)}$	"H" peak output current (2) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$			−2.0	mA
$I_{OH(peak)}$	"H" peak output current (2) $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$			−5.0	mA
$I_{OL(peak)}$	"L" peak output current (2) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$			5.0	mA
$I_{OL(peak)}$	"L" peak output current (2) $P4_0$–$P4_7$, $P5_0$, $P5_1$, $P5_4$–$P5_7$, $P6_0$–$P6_2$			10	mA
$I_{OL(peak)}$	"L" peak output current (2) $P3_0$–$P3_7$, $P5_2$, $P5_3$			30	mA
$I_{OH(avg)}$	"H" average output current (3) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$			−1.0	mA
$I_{OH(avg)}$	"H" average output current (3) $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$			−2.5	mA
$I_{OL(avg)}$	"L" average output current (3) $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$			2.5	mA
$I_{OL(avg)}$	"L" average output current (3) $P4_0$–$P4_7$, $P5_0$, $P5_1$, $P5_4$–$P5_7$, $P6_0$–$P6_2$			5.0	mA
$I_{OL(avg)}$	"L" average output current (3) $P3_0$–$P3_7$, $P5_2$, $P5_3$			15	mA

NOTES:
1. The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2. The peak output current is the peak current flowing in each port.
3. The average output current is average value measured over 100 ms.

Table 26 Electrical characteristics (2)
(Vcc = 1.8 to 5.5 V, Vss = 0 V, Ta = –20 to 85°C, f(XCIN) = 32.768 kHz, output transistors in the cut-off state, A/D converter stopped, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Unit
					Min.	Typ.	Max.	
VRAM	RAM hold voltage	When clock is stopped			1.8		5.5	V
ICC	Power source current	Frequency/2 mode	VCC=5.0V	f(XIN)=12.5MHz		6.4	13	mA
				f(XIN)=12.5MHz (in WIT state)		1.5	3.0	mA
				f(XIN)=4MHz		2.2	3.0	mA
			VCC=2.5V	f(XIN)=4MHz		0.6	1.2	mA
				f(XIN)=4MHz (in WIT state)		0.3	0.6	mA
				f(XIN)=2MHz		0.4	0.8	mA
		Frequency/4 mode	VCC=5.0V	f(XIN)=12.5MHz		3.5	10	mA
				f(XIN)=12.5MHz (in WIT state)		1.5	3.0	mA
				f(XIN)=4MHz		1.5	2.5	mA
			VCC=2.5V	f(XIN)=8MHz		0.8	2.5	mA
				f(XIN)=8MHz (in WIT state)		0.3	0.6	mA
				f(XIN)=4MHz		0.5	1.0	mA
		Frequency/8 mode	VCC=5.0V	f(XIN)=12.5MHz		2.5	5.0	mA
				f(XIN)=12.5MHz (in WIT state)		1.5	3.0	mA
				f(XIN)=4MHz		1.2	1.6	mA
			VCC=2.5V	f(XIN)=8MHz		0.5	1.0	mA
				f(XIN)=8MHz (in WIT state)		0.3	0.6	mA
				f(XIN)=4MHz		0.3	0.6	mA
		Low-speed mode	VCC=5.0V	f(XIN)=stop		17	26	µA
				in WIT state		5.5	11	µA
			VCC=2.5V	f(XIN)=stop		7.0	14	µA
				in WIT state		3.5	7.0	µA
		On-chip oscillator mode f(XIN), f(XCIN) = stop		VCC=5.0V		270	540	µA
				VCC=2.5V		35	90	µA
				VCC=2.5V (in WIT state)		25	75	µA
		All oscillations stopped (in STP state)		Ta=25°C		0.1	1.0	µA
				Ta=85°C			10	µA
		Current increased at A/D converter operating		f(XIN)=12.5 MHz, VCC=5 V in frequency/2, 4 or 8 mode		0.5		mA
				f(XIN)= stop, VCC = 5 V in on-chip oscillator operating		0.5		mA
				f(XIN) = stop, VCC = 5 V in low-speed mode		0.4		mA

A/D Converter Characteristics

Table 27 A/D converter recommended operating condition
(Vcc = 2.0 to 5.5 V, Vss = 0V, Ta = –20 to 85°C, output transistors in cut-off state, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VCC	Power source voltage		2.0	5.0	5.5	V
VIH	"H" input voltage ADKEY		0.9VCC		VCC	V
VIL	"L" input voltage ADKEY		0		0.7 × VCC–0.5	V
f(φAD)	AD converter clock frequency (1) (Low-speed • on-chip oscillator mode excluded)	4.5V < VCC ≤ 5.5V			6.25	MHz
		4.0V < VCC ≤ 4.5V			4.0	MHz
		2.0V < VCC ≤ 4.0V			VCC	MHz

NOTE:
1. Confirm the recommended operating condition for main clock input frequency.

Table 32 Switching characteristics (1)
(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = −20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ	Max.	
t_{WH}(SCLK)	Serial I/O1, 2 clock output “H” pulse width	tc(SCLK)/2-30			ns
t_{WL}(SCLK)	Serial I/O1, 2 clock output “L” pulse width	tc(SCLK)/2-30			ns
td(SCLK-TxD)	Serial I/O1, 2 output delay time (1)			140	ns
tv(SCLK-TxD)	Serial I/O1, 2 output valid time (1)	−30			ns
tr(SCLK)	Serial I/O1, 2 clock output rising time			30	ns
tf(SCLK)	Serial I/O1, 2 clock output falling time			30	ns

NOTE:
1. The $P5_5$/TxD_1 [$P3_2$/TxD_2] P-channel output disable bit (bit 4 of address $001B_{16}$ [$001F_{16}$]) of UART control register is “0”.

Table 33 Switching characteristics (2)
(Vcc = 1.8 to 4.0 V, Vss = 0 V, Ta = −20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ	Max.	
t_{WH}(SCLK)	Serial I/O1, 2 clock output “H” pulse width	tc(SCLK)/2-80			ns
t_{WL}(SCLK)	Serial I/O1, 2 clock output “L” pulse width	tc(SCLK)/2-80			ns
td(SCLK-TxD)	Serial I/O1, 2 output delay time (1)			350	ns
tv(SCLK-TxD)	Serial I/O1, 2 output valid time (1)	-30			ns
tr(SCLK)	Serial I/O1, 2 clock output rising time			80	ns
tf(SCLK)	Serial I/O1, 2 clock output falling time			80	ns

NOTE:
1. The $P5_5$/TxD_1 [$P3_2$/TxD_2] P-channel output disable bit (bit 4 of address $001B_{16}$ [$001F_{16}$]) of UART control register is “0”.

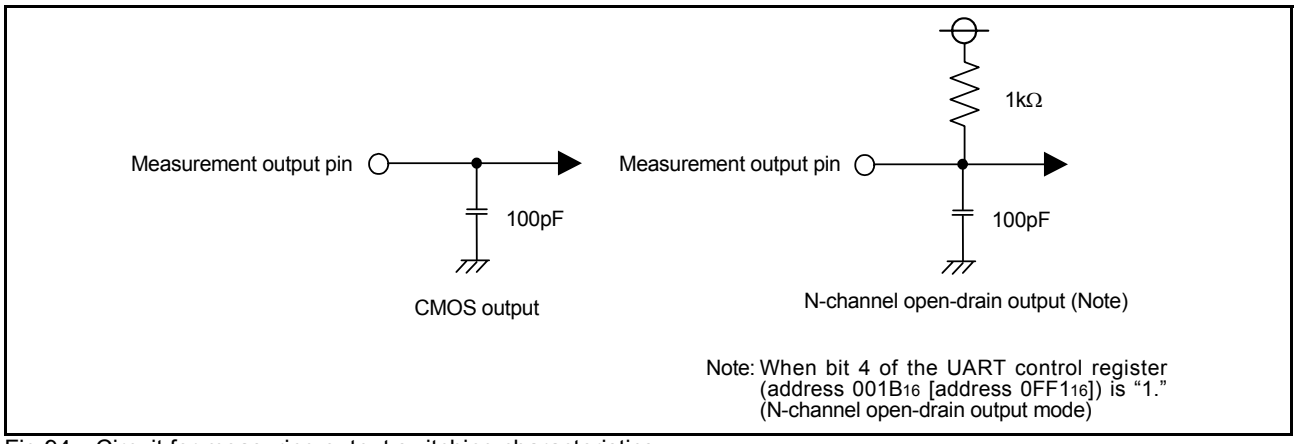


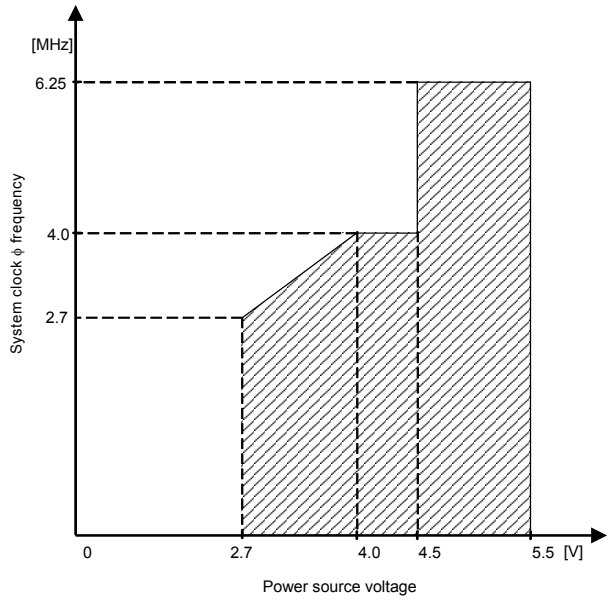
Fig 94. Circuit for measuring output switching characteristics

Table 37 Recommended operating conditions (4)
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
f(CNTR0) f(CNTR1)	Timer X and Timer Y Input frequency (duty cycle 50%)	4.5V ≤ V_{CC} ≤ 5.5V			6.25	MHz
		4.0V ≤ V_{CC} < 4.5V			2×Vcc–4	MHz
		2.7V ≤ V_{CC} < 4.0V			Vcc	MHz
f(Tclk)	Timer X, Timer Y, Timer 1, Timer 2, Timer 3, Timer 4 clock input frequency (Count source frequency of each timer)	4.5V ≤ V_{CC} ≤ 5.5V			16	MHz
		4.0V ≤ V_{CC} < 4.5V			4×Vcc–8	MHz
		2.7V ≤ V_{CC} < 4.0V			2×Vcc	MHz
f(ϕ)	System clock ϕ frequency (1)	4.5V ≤ V_{CC} ≤ 5.5V			6.25	MHz
		4.0V ≤ V_{CC} < 4.5V			4	MHz
		2.7V ≤ V_{CC} < 4.0V			Vcc	MHz
f(X_{IN})	Main clock input frequency (duty cycle 50%) (2)(3)	4.5V ≤ V_{CC} ≤ 5.5V	1.0		16	MHz
		2.7V ≤ V_{CC} < 4.5V	1.0		8.0	MHz
f(X_{CIN})	Sub-clock oscillation frequency (duty cycle 50%) (4)(5)			32.768	80	kHz

NOTES:
1. Relationship between system clock ϕ frequency and power source voltage is shown in the graph below.
2. When the A/D converter is used, refer to the recommended operating conditions of the A/D converter.
3. 12.5 MHz < f(X_{IN}) ≤ 16 MHz is not available in the frequency/2 mode.
4. The oscillation start voltage and the oscillation start time differ depending on factors such as the oscillator, circuit constants, and operating temperature range. Note that oscillation start may be particularly difficult at low voltage when using a high-frequency oscillator.
5. When using the microcomputer in low-speed mode, set the clock input oscillation frequency on condition that f(X_{CIN}) < f(X_{IN})/3.

<System clock ϕ frequency>



<Main clock X_{IN} frequency>

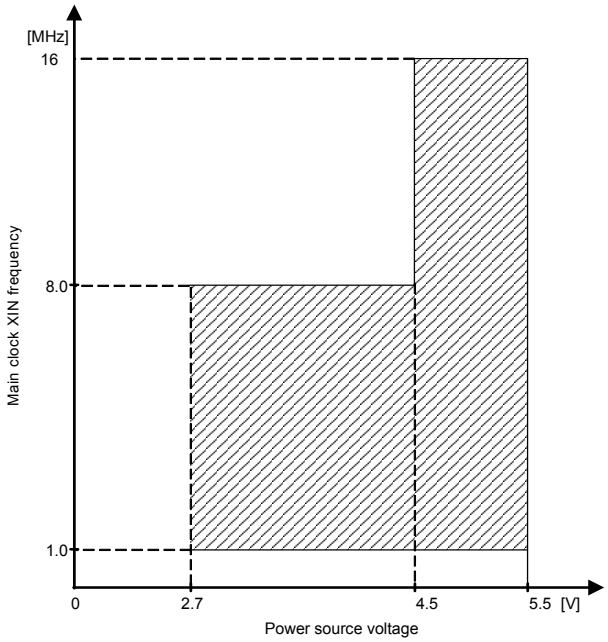


Table 39 Electrical characteristics (2)
(Vcc = 2.7 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85°C, f(X_{CIN}) = 32.768 kHz, output transistors in the cut-off state, A/D converter stopped, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Unit
					Min.	Typ.	Max.	
V_{RAM}	RAM hold voltage	When clock is stopped			2.2		5.5	V
I_{CC}	Power source current	Frequency/2 mode	Vcc=5.0V	f(X_{IN})=12.5MHz		4.0	7.0	mA
				f(X_{IN})=12.5MHz (in WIT state)		2.0	3.5	mA
				f(X_{IN})=4MHz		2.0	3.5	mA
			Vcc=2.7V	f(X_{IN})=4MHz		1.5	3	mA
				f(X_{IN})=4MHz (in WIT state)		1.0	2.5	mA
				f(X_{IN})=2MHz		1.0	2.5	mA
		Frequency/4 mode	Vcc=5.0V	f(X_{IN})=12.5MHz		3.2	5.6	mA
				f(X_{IN})=12.5MHz (in WIT state)		1.6	3.2	mA
				f(X_{IN})=4MHz		1.6	3.2	mA
			Vcc=2.7V	f(X_{IN})=8MHz		1.6	3.2	mA
				f(X_{IN})=8MHz (in WIT state)		1.0	2.5	mA
				f(X_{IN})=4MHz		1.0	2.5	mA
		Frequency/8 mode	Vcc=5.0V	f(X_{IN})=12.5MHz		2.5	5	mA
				f(X_{IN})=12.5MHz (in WIT state)		1.5	3	mA
				f(X_{IN})=4MHz		1.5	3	mA
			Vcc=2.7V	f(X_{IN})=8MHz		1.5	3	mA
				f(X_{IN})=8MHz (in WIT state)		1.0	2.5	mA
				f(X_{IN})=4MHz		1.0	2.5	mA
		Low-speed mode	Vcc=5.0V	f(X_{IN})=stop		400	800	µA
				in WIT state Ta=25°C		4.0	10	µA
				in WIT state Ta=85°C			20	µA
			Vcc=2.7V	f(X_{IN})=stop		300	600	µA
				in WIT state Ta=25°C		3.7	9	µA
				in WIT state Ta=85°C			18	µA
		On-chip oscillator mode f(X_{IN}), f(X_{CIN}): stop		Vcc=5.0V		600	1200	µA
				Vcc=2.7V		500	1000	µA
				Vcc=2.7V (in WIT state)		500	1000	µA
		All oscillations are stopped (in STP state)		Ta=25°C		0.6	3.0	µA
				Ta=85°C		1.0		µA
		Current increased at A/D converter operating		f(X_{IN})=12.5MHz, V_{CC}=5V in frequency/2, 4 or 8 mode		1.0		mA
				f(X_{IN})=stop, V_{CC}=5V in on-chip oscillator operating		1.0		mA
				f(X_{IN})=stop, V_{CC}=5V in low-speed mode		0.8		mA

A/D Converter Characteristics

Table 40 A/D converter recommended operating condition
(Vcc = 2.7 to 5.5 V, Ta = –20 to 85°C, output transistors in cut-off state, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage		2.7	5.0	5.5	V
V_{IH}	"H" input voltage ADKEY		0.9Vcc		Vcc	V
V_{IL}	"L" input voltage ADKEY		0		0.7 × Vcc – 0.5	V
f(ϕ_{AD})	AD converter clock frequency (1) (Low-speed・on-chip oscillator mode excluded)	4.5V < Vcc ≤ 5.5V			6.25	MHz
		4.0V < Vcc ≤ 4.5V			4.0	MHz
		2.7V < Vcc ≤ 4.0V			Vcc	MHz

NOTE:
1. Confirm the recommended operating condition for main clock input frequency.

Notes on QzROM Version

Wiring to OSCSEL pin

(1) OSCSEL = L

Connect the OSCSEL pin the shortest possible to the GND pattern which is supplied to the VSS pin of the microcomputer. In addition connecting an approximately 5 kΩ resistor in series to the GND could improve noise immunity. In this case as well as the above mention, connect the pin the shortest possible to the GND pattern which is supplied to the VSS pin of the microcomputer.

(2) OSCSEL = H

Connect the OSCSEL pin the shortest possible to the VCC pattern which is supplied to the VCC pin of the microcomputer. In addition connecting an approximately 5 kΩ resistor in series to the VCC could improve noise immunity. In this case as well as the above mention, connect the pin the shortest possible to the VCC pattern which is supplied to the VCC pin of the microcomputer.

<Reason>

The OSCSEL pin is the power source input pin for the built-in QzROM.

When programming in the QzROM, the impedance of the OSCSEL pin is low to allow the electric current for writing to flow into the built-in QzROM. Because of this, noise can enter easily. If noise enters the OSCSEL pin, abnormal instruction codes or data are read from the QzROM, which may cause a program runaway.

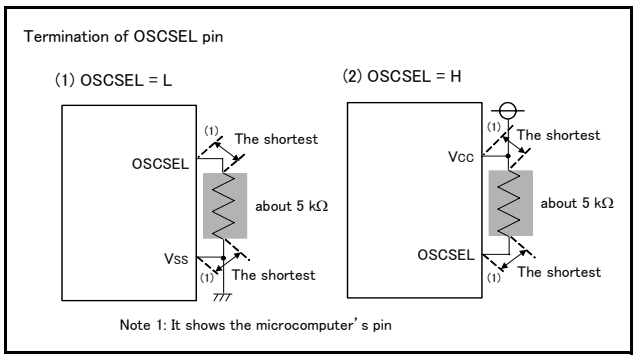


Fig. 106 Wiring for OSCSEL pin

Overvoltage in QzROM Version

Make sure that voltage exceeding the VCC pin voltage is not applied to other pins. In particular, ensure that the state indicated by bold lines in figure below does not occur for pin OSCSEL pin (VPP power source pin for QzROM) during power-on or power-off. Otherwise the contents of QzROM could be rewritten.

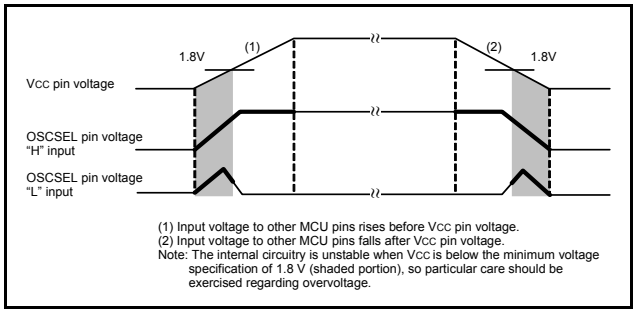


Fig. 107 Timing Diagram (Bold-lined periods are applicable)

QzROM Version Product Shipped in Blank

As for the product shipped in blank, Renesas does not perform the writing test to user ROM area after the assembly process though the QzROM writing test is performed enough before the assembly process. Therefore, a writing error of approximate 0.1% may occur.

Moreover, please note the contact of cables and foreign bodies on a socket, etc. because a writing environment may cause some writing errors.

Ordering QzROM Writing

1. Notes On QzROM Writing Orders

When ordering the QzROM product shipped after writing, submit the mask file (extension: .msk) which is made by the mask file converter MM.

- Be sure to set the ROM option data* setup when making the mask file by using the mask file converter MM.. The ROM code protect is specified according to the ROM option data* in the mask file which is submitted at ordering. Note that the mask file which has nothing at the ROM option data* or has the data other than "00$_{16}$", "FE$_{16}$" and "FF$_{16}$" can not be accepted.
- Set "FF$_{16}$" to the ROM code protect address in ROM data regardless of the presence or absence of a protect. When data other than "FF$_{16}$" is set, we may ask that the ROM data be submitted again.

* ROM option data: mask option noted in MM

2. Data Required for QzROM Ordering

The following are necessary when ordering a QzROM product shipped after writing:

- QzROM Writing Confirmation Form*
- Mark Specification Form*
- ROM data: Mask file

* For the QzROM writing confirmation form and the mark specification form, refer to the "Renesas Technology Corp." Homepage (http://www.renesas.com/homepage.jsp).

Note that we cannot deal with special font marking (customer's trademark etc.) in QzROM microcomputer.

3. QzROM Product Receiving Procedure

When writing to QzROM is performed by user side, the receiving inspection by the following flow is necessary.

REVISION HISTORY	38D2 Group Datasheet

Rev.	Date	Description	
		Page	Summary
3.01	Sep.18, 2007	118-131	Appendix is added
3.02	Apr. 09, 2008	2	Fig. 1: Revised
		3	Table 1: Revised
		5	Table 2: Revised
		18	“Direction Registers”: Peripheral output name is added and deleted
		21	Fig. 14: Revised
		23	Table 9: Revised
		25	“External Interrupt Pin Selection” is deleted
		26	Fig. 17:Revised
		29	Port name is revised
		34	Fig. 26: Revised
		38	“Timer Y” is revised
		44	Fig. 36: Revised
		49	Fig. 41: Revised
		57	Fig. 53 and 54 are revised
		58	Fig. 56: Revised
		63	Fig. 63: Revised
		64	Fig. 63: Revised
		65	Table 14: Revised
		66	Fig. 65: Revised
		74	Fig. 73: Revised
		85	Fig. 80: Revised
		86	Fig. 81: Revised
		90	Notes On ROM Code Protect is revised
		95	Table 22: Revised
		99	Table 27: Revised
		102	Table 30: Revised
		109	NOTE of Table 38: Revised
		110	Table 40: Revised
		129	Notes On ROM Code Protect is revised