Renesas Electronics America Inc - R5F2120AKFP#U0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	5K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2120akfp-u0

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Table 1.4 Product Information for R8C/21 Group **Current of Aug. 2008**

Type No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data Flash				
R5F21216JFP	32 Kbytes	1 Kbyte X 2	2 Kbytes	PLQP0048KB-A	J version	Flash memory version
R5F21217JFP	48 Kbytes	1 Kbyte X 2	2.5 Kbytes	PLQP0048KB-A		
R5F21218JFP	64 Kbytes	1 Kbyte X 2	3 Kbytes	PLQP0048KB-A		
R5F2121AJFP	96 Kbytes	1 Kbyte X 2	5 Kbytes	PLQP0048KB-A		
R5F2121CJFP	128 Kbytes(1)	1 Kbyte X 2	6 Kbytes	PLQP0048KB-A		
R5F21216KFP	32 Kbytes	1 Kbyte X 2	2 Kbytes	PLQP0048KB-A	K version	
R5F21217KFP	48 Kbytes	1 Kbyte X 2	2.5 Kbytes	PLQP0048KB-A		
R5F21218KFP	64 Kbytes	1 Kbyte X 2	3 Kbytes	PLQP0048KB-A		
R5F2121AKFP	96 Kbytes	1 Kbyte X 2	5 Kbytes	PLQP0048KB-A		
R5F2121CKFP	128 Kbytes(1)	1 Kbyte X 2	6 Kbytes	PLQP0048KB-A		

NOTE:
1. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **23. Notes on Emulator Debugger** of Hardware Manual.

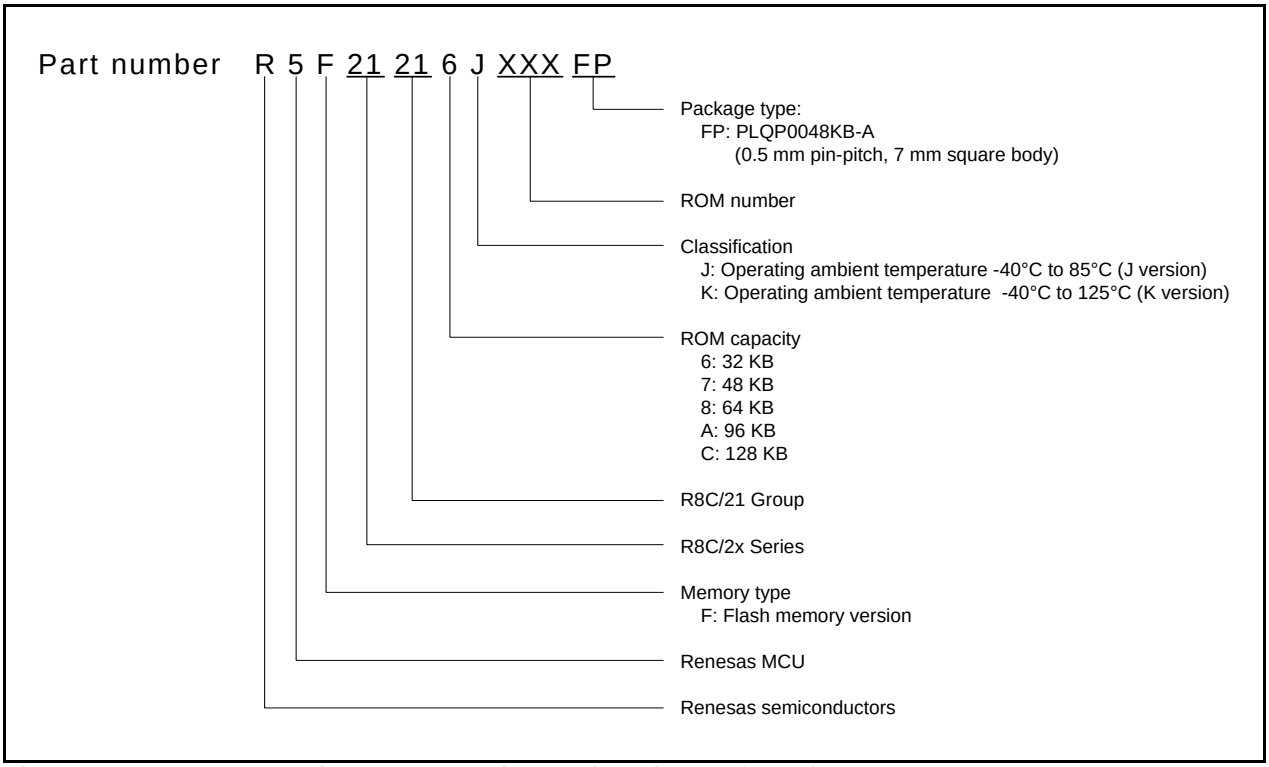
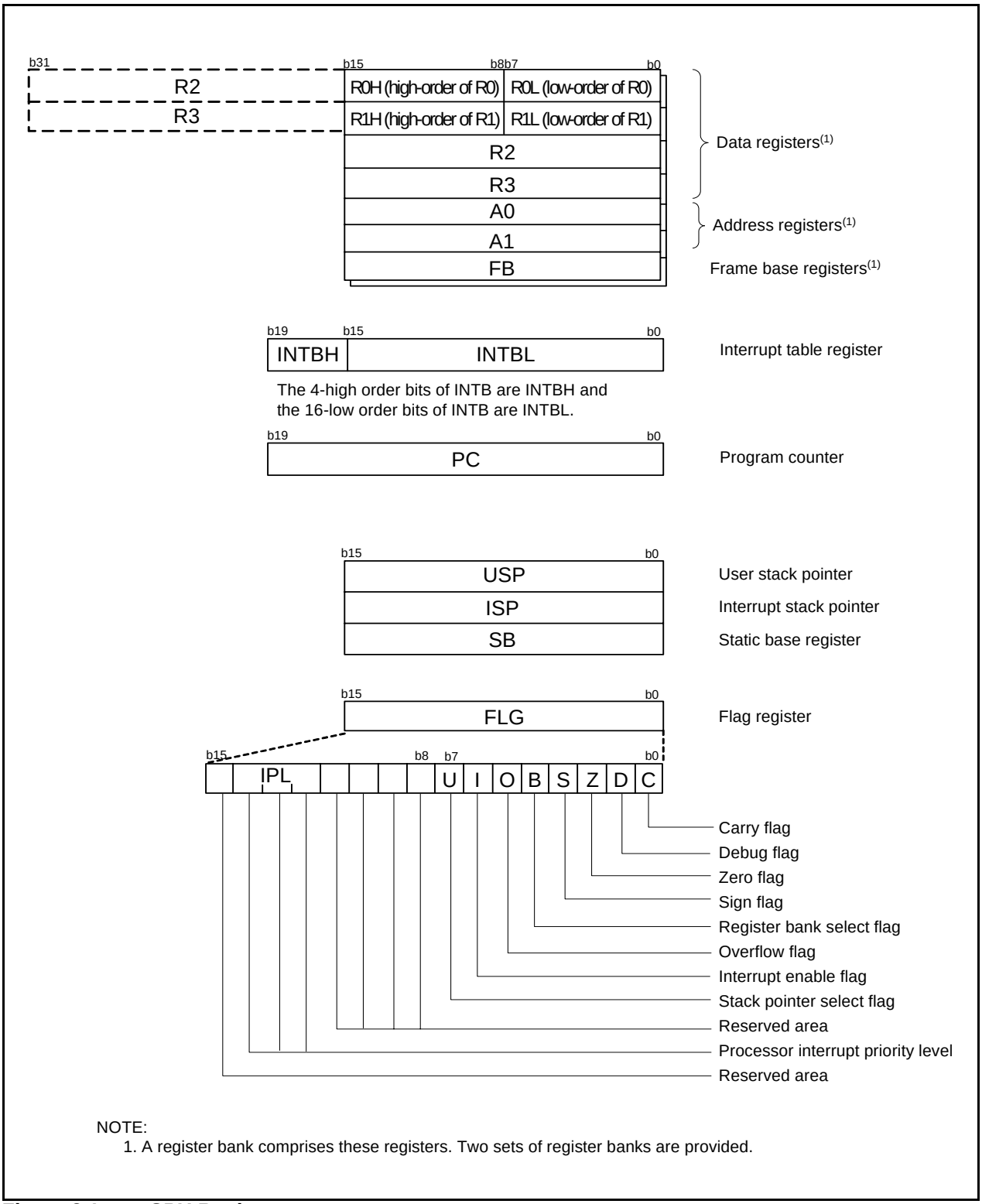


Figure 1.3 Type Number, Memory Size, and Package of R8C/21 Group

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. Of these, R0, R1, R2, R3, A0, A1, and FB comprise a register bank. Two sets of register banks are provided.



NOTE:
1. A register bank comprises these registers. Two sets of register banks are provided.

Figure 2.1 CPU Registers

2.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.
An interrupt is disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has greater priority than IPL, the interrupt is enabled.

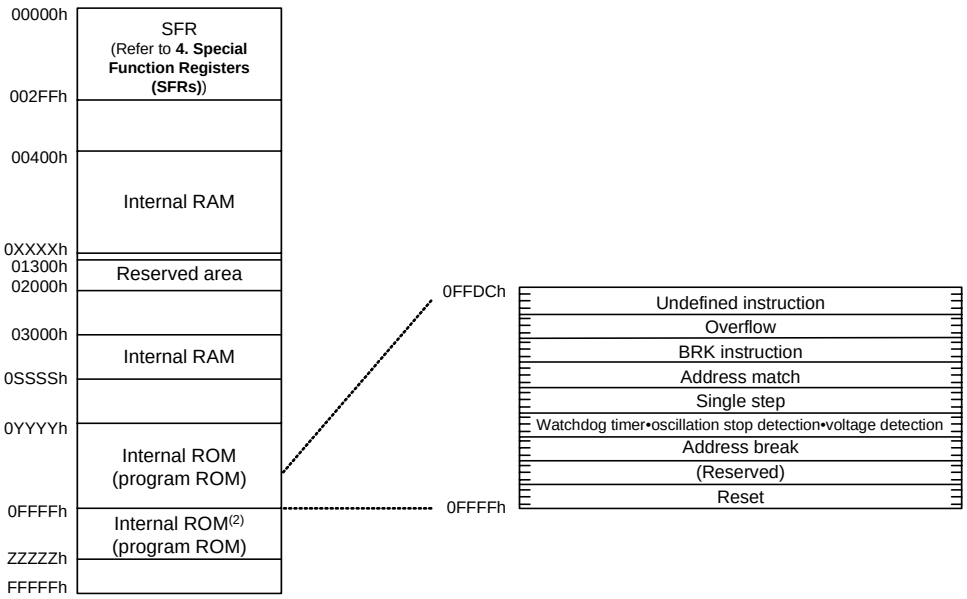
2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

3.1 R8C/20 Group

Figure 3.1 shows a Memory Map of R8C/20 Group. The R8C/20 Group has 1 Mbyte of address space from address 00000h to FFFFFh.
The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFR) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future user and cannot be accessed by users.



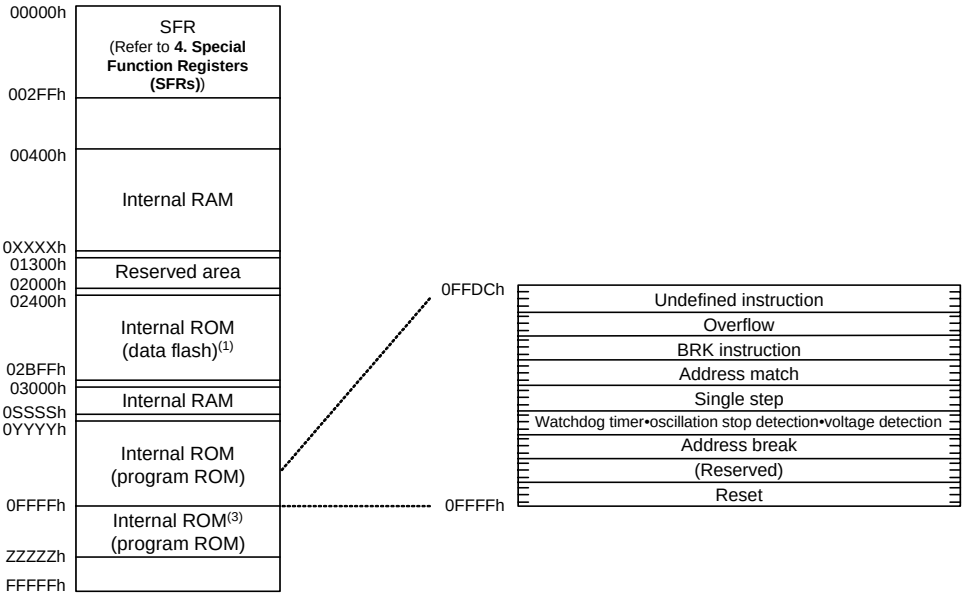
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **23. Notes on Emulator Debugger** of Hardware Manual.

Part Number	Internal ROM			Internal RAM		
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh	Address 0SSSSh
R5F21206JFP, R5F21206KFP	32 Kbytes	08000h	-	2 Kbytes	00BFFh	-
R5F21207JFP, R5F21207KFP	48 Kbytes	04000h	-	2.5 Kbytes	00DFFh	-
R5F21208JFP, R5F21208KFP	64 Kbytes	04000h	13FFFh	3 Kbytes	00FFFh	-
R5F2120AJFP, R5F2120AKFP	96 Kbytes	04000h	1BFFFh	5 Kbytes	00FFFh	037FFh
R5F2120CJFP, R5F2120CKFP	128 Kbytes	04000h	23FFFh	6 Kbytes	00FFFh	03BFFh

Figure 3.1 Memory Map of R8C/20 Group

3.2 R8C/21 Group

Figure 3.2 shows a Memory Map of R8C/21 Group. The R8C/21 Group has 1 Mbyte of address space from address 00000h to FFFFFh.
The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFR) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated them. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTES:
1. Data flash block A (1 Kbyte) and B (1 Kbyte) are shown.
2. The blank regions are reserved. Do not access locations in these regions.
3. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **23. Notes on Emulator Debugger** of Hardware Manual.

Part Number	Internal ROM			Internal RAM		
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh	Address 0SSSSh
R5F21216JFP, R5F21216KFP	32 Kbytes	08000h	-	2 Kbytes	00BFFh	-
R5F21217JFP, R5F21217KFP	48 Kbytes	04000h	-	2.5 Kbytes	00DFFh	-
R5F21218JFP, R5F21218KFP	64 Kbytes	04000h	13FFFh	3 Kbytes	00FFFh	-
R5F2121AJFP, R5F2121AKFP	96 Kbytes	04000h	1BFFFh	5 Kbytes	00FFFh	037FFh
R5F2121CJFP, R5F2121CKFP	128 Kbytes	04000h	23FFFh	6 Kbytes	00FFFh	03BFFh

Figure 3.2 Memory Map of R8C/21 Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function.
Table 4.1 to Table 4.6 list the SFR Information.

Table 4.1 SFR Information (1)[1]

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protect Mode Register	CSPR	00h 10000000b[8]
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0030h			
0031h	Voltage Detection Register 1[2]	VCA1	00001000b
0032h	Voltage Detection Register 2[6]	VCA2	00h[3] 01000000b[4]
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register[7]	VW1C	0000X000b[3] 0100X001b[4]
0037h	Voltage Monitor 2 Circuit Control Register[5]	VW2C	00h
0038h			
0039h			
003Fh			

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect this register.
3. The LVD0ON bit in the OFS register is set to 1.
4. Power-on reset, voltage monitor 1 reset or the LVD0ON bit in the OFS register is set to 0.
5. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect b2 and b3.
6. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect b7.
7. Software reset, the watchdog timer rest, and the voltage monitor 2 reset do not affect other than the b0 and b6.
8. The CSPROINI bit in the OFS register is 0.

Table 4.2 SFR Information (2)(1)

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h			
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register/IIC Bus Interrupt Control Register(2)	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.6 SFR Information (6)(1)

Address	Register	Symbol	After reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIORA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIORA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			
FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
V_{CC}/AV_{CC}	Supply voltage		-0.3 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC}+0.3	V
V_O	Output voltage		-0.3 to V_{CC}+0.3	V
P_d	Power dissipation	-40°C ≤ Topr ≤ 85°C	300	mW
		85°C < Topr ≤ 125°C	125	mW
T_{opr}	Operating ambient temperature		-40 to 85 (J version) / -40 to 125 (K version)	°C
T_{stg}	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage			2.7	–	5.5	V
V_{SS}/AV_{CC}	Supply voltage			–	0	–	V
V_{IH}	Input “H” voltage			0.8V_{CC}	–	V_{CC}	V
V_{IL}	Input “L” voltage			0	–	0.2V_{CC}	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all Pins $I_{OH\ (peak)}$		–	–	-60	mA
$I_{OH(peak)}$	Peak output “H” current			–	–	-10	mA
$I_{OH(avg)}$	Average output “H” current			–	–	-5	mA
$I_{OL(sum)}$	Peak sum output “L” currents	Sum of all Pins $I_{OL\ (peak)}$		–	–	60	mA
$I_{OL(peak)}$	Peak output “L” currents			–	–	10	mA
$I_{OL(avg)}$	Average output “L” current			–	–	5	mA
$f_{(XIN)}$	XIN clock input oscillation frequency		3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	0	–	20	MHz
			3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 125°C	0	–	16	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
–	System clock	OCD2 = 0 When XIN clock is selected.	3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	0	–	20	MHz
			3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 125°C	0	–	16	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
		OCD2 = 1 When on-chip oscillator clock is selected.	FRA01 = 0 When low-speed on-chip oscillator clock is selected.	–	125	–	kHz
			FRA01 = 1 When high-speed on-chip oscillator clock is selected. 3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	–	–	20	MHz
			FRA01 = 1 When high-speed on-chip oscillator clock is selected.	–	–	10	MHz

NOTES:
1. V_{CC} = 2.7 to 5.5 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

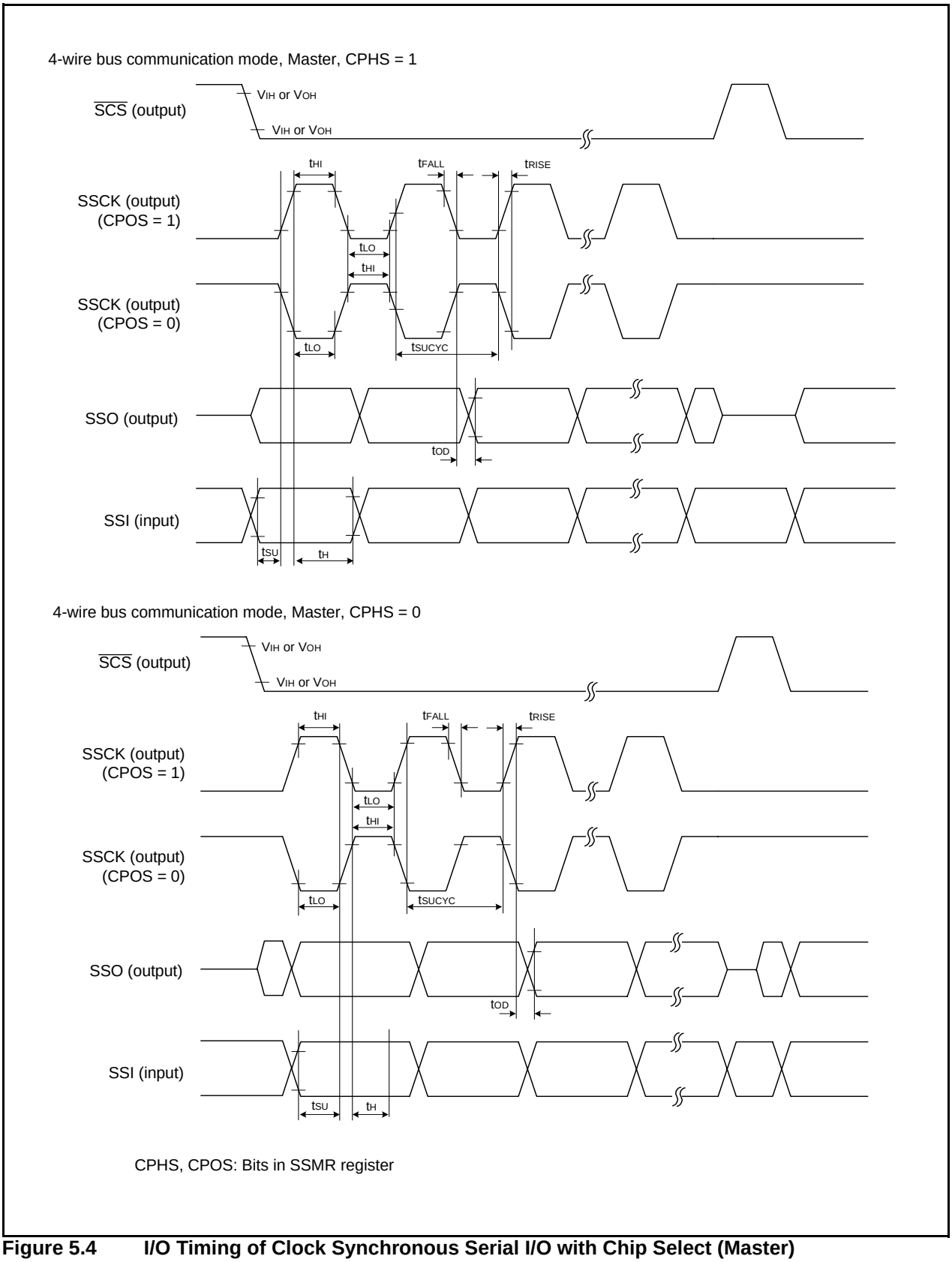


Figure 5.4 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

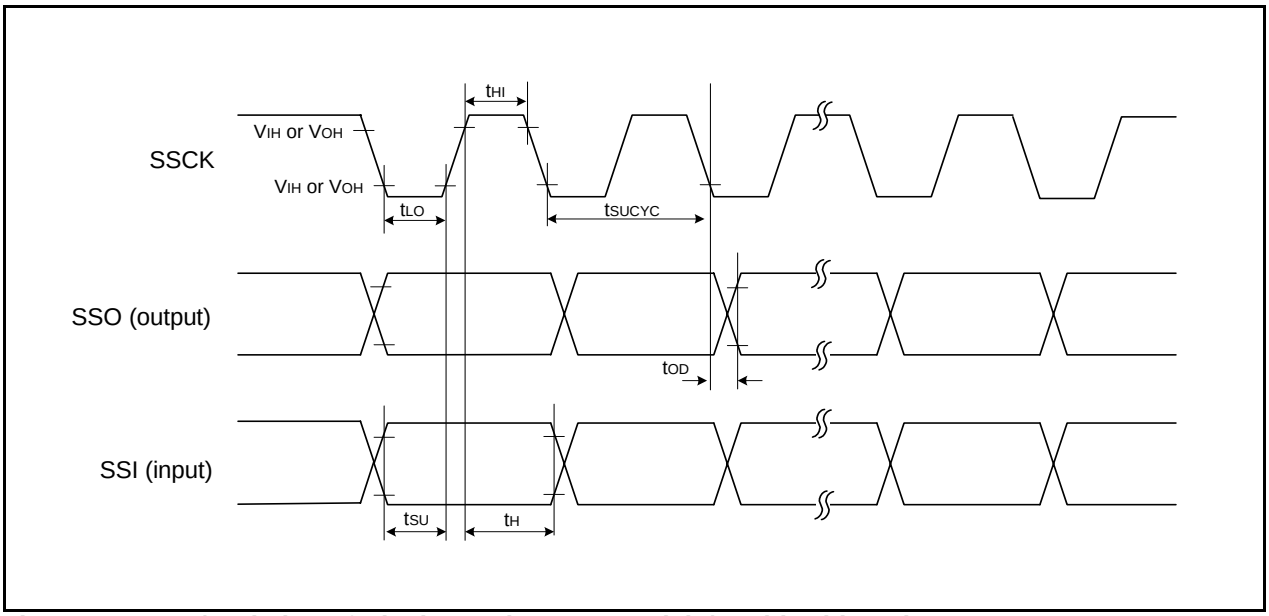
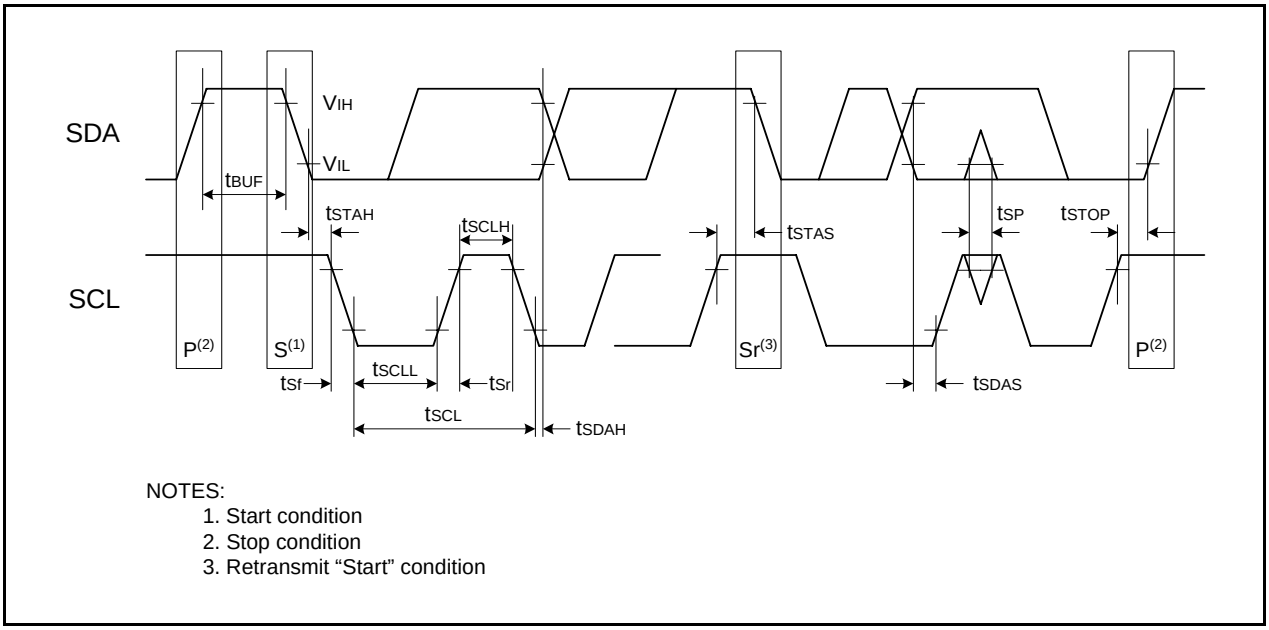


Figure 5.6 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

Table 5.13 Timing Requirements of I²C Bus Interface(1)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC}$ + 600(2)	–	–	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC}$ + 300(2)	–	–	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC}$ + 300(2)	–	–	ns
t_{sf}	SCL, SDA input falling time		–	–	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		–	–	$1t_{CYC}$(2)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$(2)	–	–	ns
t_{STAH}	Start condition input hole time		$3t_{CYC}$(2)	–	–	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$(2)	–	–	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$(2)	–	–	ns
t_{SOAS}	Data input setup time		$1t_{CYC}$ + 20(2)	–	–	ns
t_{SDAH}	Data input hold time		0	–	–	ns

NOTES:
1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. $1t_{CYC}$ = 1/f1(s)



NOTES:
1. Start condition
2. Stop condition
3. Retransmit “Start” condition

Figure 5.7 I/O Timing of I²C Bus Interface

Table 5.14 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” Voltage	Except XOUT	I_{OH} = -5 mA		V_{CC} – 2.0	–	V_{CC}	V
			I_{OH} = -200 μA		V_{CC} – 0.3	–	V_{CC}	V
		XOUT	Drive capacity HIGH	I_{OH} = -1 mA	V_{CC} – 2.0	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -500 μA	V_{CC} – 2.0	–	V_{CC}	V
V_{OL}	Output “L” Voltage	Except XOUT	I_{OL} = 5 mA		–	–	2.0	V
			I_{OL} = 200 μA		–	–	0.45	V
		XOUT	Drive capacity HIGH	I_{OL} = 1 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 500 μA	–	–	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, SSI, SCL, SDA, SSO			0.1	0.5	–	V
		$\overline{RESET}$			0.1	1.0	–	V
I_{IH}	Input “H” current		VI = 5 V, V_{CC} = 5 V		–	–	5.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 5 V		–	–	-5.0	μA
R_{PULLUP}	Pull-Up Resistance		VI = 0 V, V_{CC} = 5 V		30	50	167	kΩ
R_{fXIN}	Feedback Resistance	XIN			–	1.0	–	MΩ
V_{RAM}	RAM Hold Voltage		During stop mode		2.0	–	–	V

NOTE:
1. V_{CC} = 4.2 to 5.5 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), f(XIN) = 20 MHz, unless otherwise specified.

Timing Requirements (Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C) [Vcc = 5 V]

Table 5.16 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	25	–	ns
$t_{WL(XIN)}$	XIN input “L” width	25	–	ns

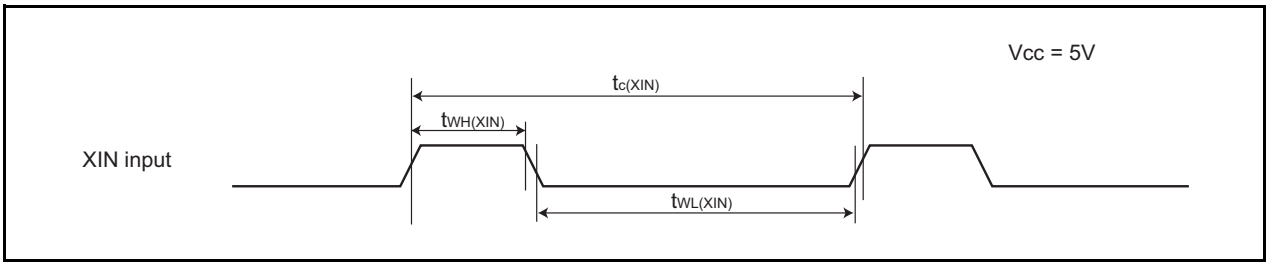


Figure 5.8 XIN Input Timing Diagram when Vcc = 5 V

Table 5.17 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

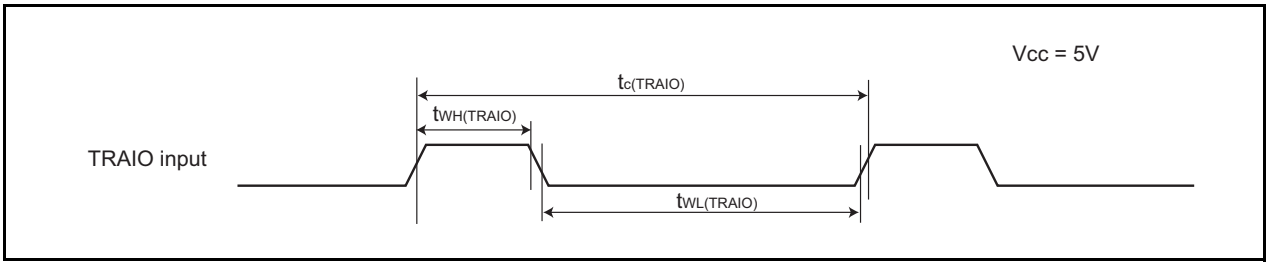


Figure 5.9 TRAIO Input Timing Diagram when Vcc = 5 V

Table 5.20 Electrical Characteristics (3) [Vcc = 3 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except XOUT	I_{OH} = -1 mA		V_{CC} – 0.5	–	V_{CC}	V
		XOUT	Drive capacity HIGH	I_{OH} = -0.1 mA	V_{CC} – 0.5	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -50 μA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage	Except XOUT	I_{OL} = 1 mA		–	–	0.5	V
		XOUT	Drive capacity HIGH	I_{OL} = 0.1 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 50 μA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, SSI, SCL, SDA, SSO			0.1	0.3	–	V
		$\overline{RESET}$			0.1	0.4	–	V
I_{IH}	Input “H” current		VI = 3 V, V_{CC} = 3 V		–	–	4.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 3 V		–	–	-4.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 3 V		66	160	500	kΩ
R_{fXIN}	Feedback resistance	XIN			–	3.0	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		2.0	–	–	V

NOTE:
1. V_{CC} = 2.7 to 3.3 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), f(XIN) = 10 MHz, unless otherwise specified.

Timing Requirements (Unless Otherwise Specified: Vcc = 3 V, Vss = 0V at Topr = 25°C) [Vcc = 3 V]

Table 5.22 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input “H” width	40	–	ns
$t_{WL(XIN)}$	XIN input “L” width	40	–	ns

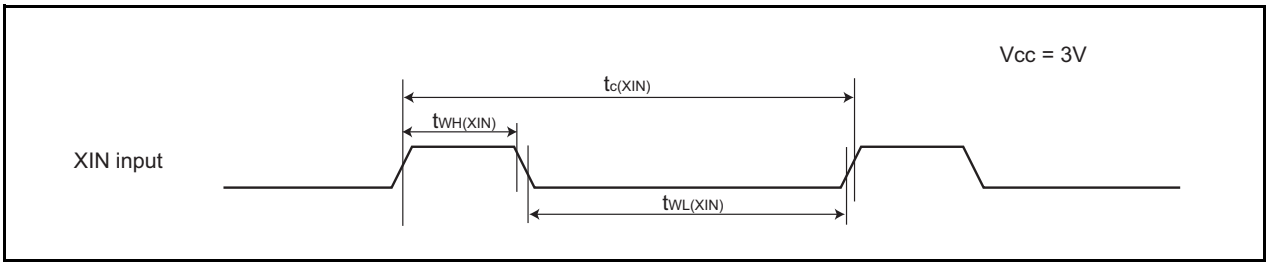


Figure 5.12 XIN Input Timing Diagram when Vcc = 3 V

Table 5.23 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input Cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

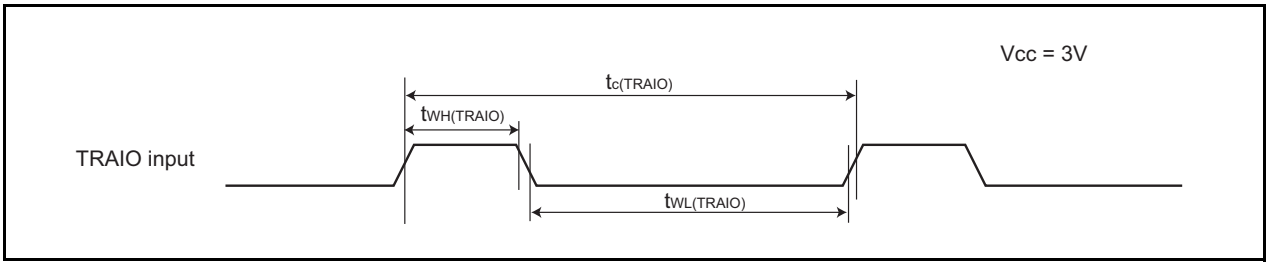


Figure 5.13 TRAIO Input Timing Diagram when Vcc = 3 V

Table 5.24 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	300	–	ns
$t_{W(CKH)}$	CLK0 input “H” width	150	–	ns
$t_{W(CKL)}$	CLK0 input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

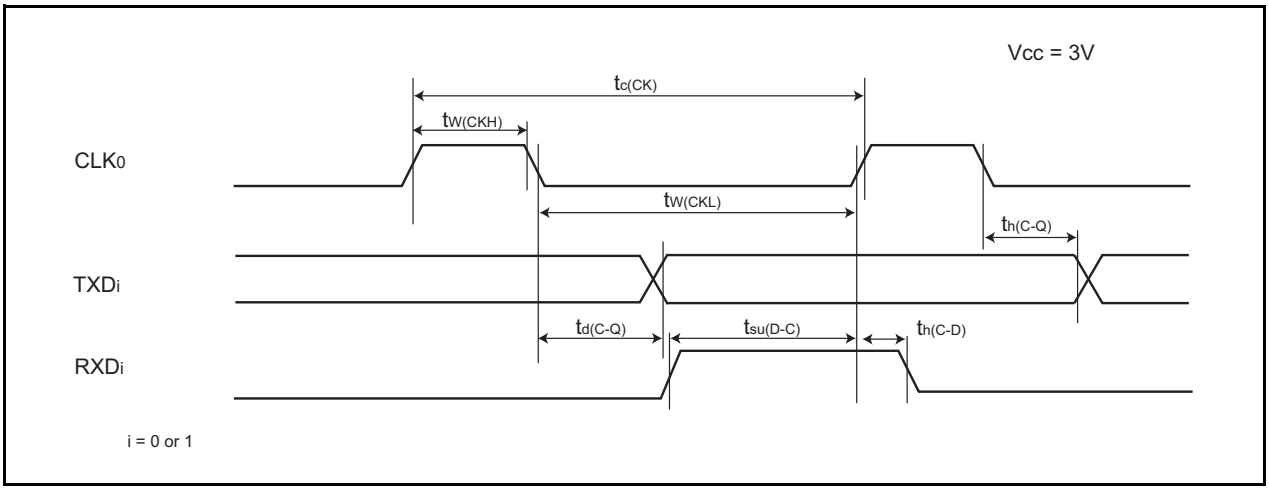


Figure 5.14 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.25 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input HIGH width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input LOW width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.

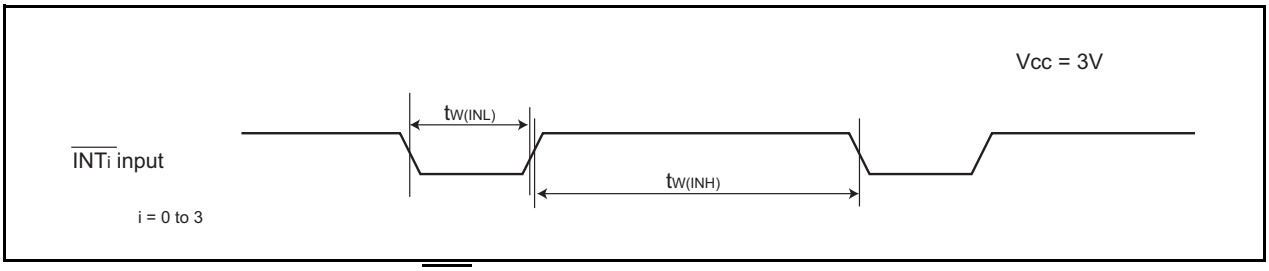
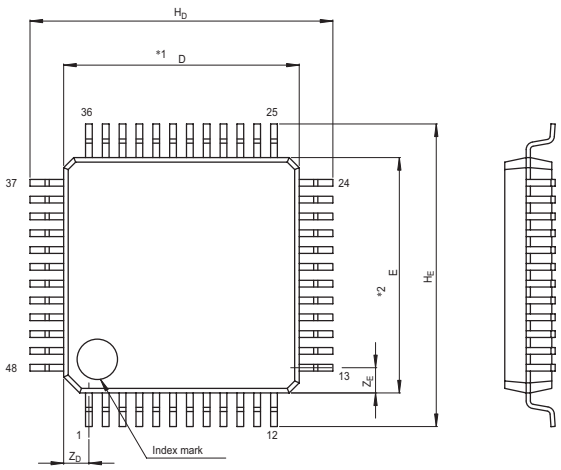


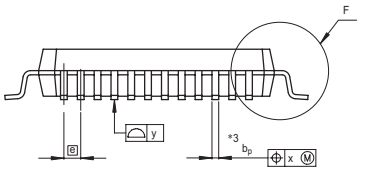
Figure 5.15 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 3 V (i = 0 to 3)

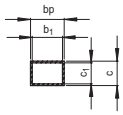
Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

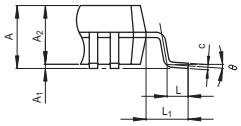
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g







Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

REVISION HISTORY	R8C/20 Group, R8C/21 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.20	Sep 29, 2005	20	Table 4.6 SFR Information (6) revised - 0145h: POCR0 → TRDPOCR0 - 0146h, 0147h: TRDCNT0 → TRD0 - 0148h, 0149h: GRA0 → TRDGRA0 - 014Ah, 014Bh: GRB0 → TRDGRB0 - 014Ch, 014Dh: GRC0 → TRDGRC0 - 014Eh, 014Fh: GRD0 → TRDGRD0 - 0155h: POCR1 -> TRDPOCR1 - 0156h, 0157h: TRDCNT1 → TRD1 - 0158h, 0159h: GRA1 → TRDGRA1 - 015Ah, 015Bh: GRB1 → TRDGRB1 - 015Ch, 015Dh: GRC1 → TRDGRC1 - 015Eh, 015Fh: GRD1 → TRDGRD1
		22	5. Electrical Characteristics added
1.00	Nov 15, 2006	All pages	“Preliminary” and “Under development” deleted
		2	Table 1.1 Functions and Specifications for R8C/20 Group revised. NOTE1 deleted.
		3	Table 1.2 Functions and Specifications for R8C/21 Group revised. NOTE1 deleted.
		5	Table 1.3 Product Information for R8C/20 Group; “R5F2120AJFP (D)”, “R5F2120CJFP (D)”, “R5F2120AKFP (D)”, “R5F2120CKFP (D)”, and NOTE added. Figure 1.2 Type Number, Memory Size, and Package of R8C/20 Group; “A: 96 KB” and “C: 128 KB” added.
		6	Table 1.4 Product Information for R8C/21 Group; “R5F2121AJFP (D)”, “R5F2121CJFP (D)”, “R5F2121AKFP (D)”, “R5F2121CKFP (D)”, and NOTE added. Figure 1.3 Type Number, Memory Size, and Package of R8C/21 Group; “A: 96 KB” and “C: 128 KB” added.
		13	Figure 3.1 Memory Map of R8C/20 Group revised.
		14	Figure 3.2 Memory Map of R8C/21 Group revised.
		15	Table 4.1 SFR Information (1)(1); NOTE8; “The CSPROINI bit in the OFS register is set to 0.” → “The CSPROINI bit in the OFS register is 0.” revised.
		21	Table 5.1 Absolute Maximum Ratings; Power dissipation revised. Table 5.2 Recommended Operating Conditions; System clock revised.
		26	Table 5.8 Voltage Monitor 1 Reset Circuit Electrical Characteristics → Table 5.8 Power-on Reset Circuit, Voltage Monitor 1 Reset Circuit Electrical Characteristics(1) replaced. Table 5.8 revised. NOTE3 added. Table 5.9 Power-on Reset Circuit Electrical Characteristics deleted. Figure 5.3 Power-on Reset Circuit Electrical Characteristics revised.
		27	Table 5.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics → Table 5.9 High-Speed On-Chip Oscillator Circuit Electrical Characteristics revised.