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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2120cjfp-u0

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

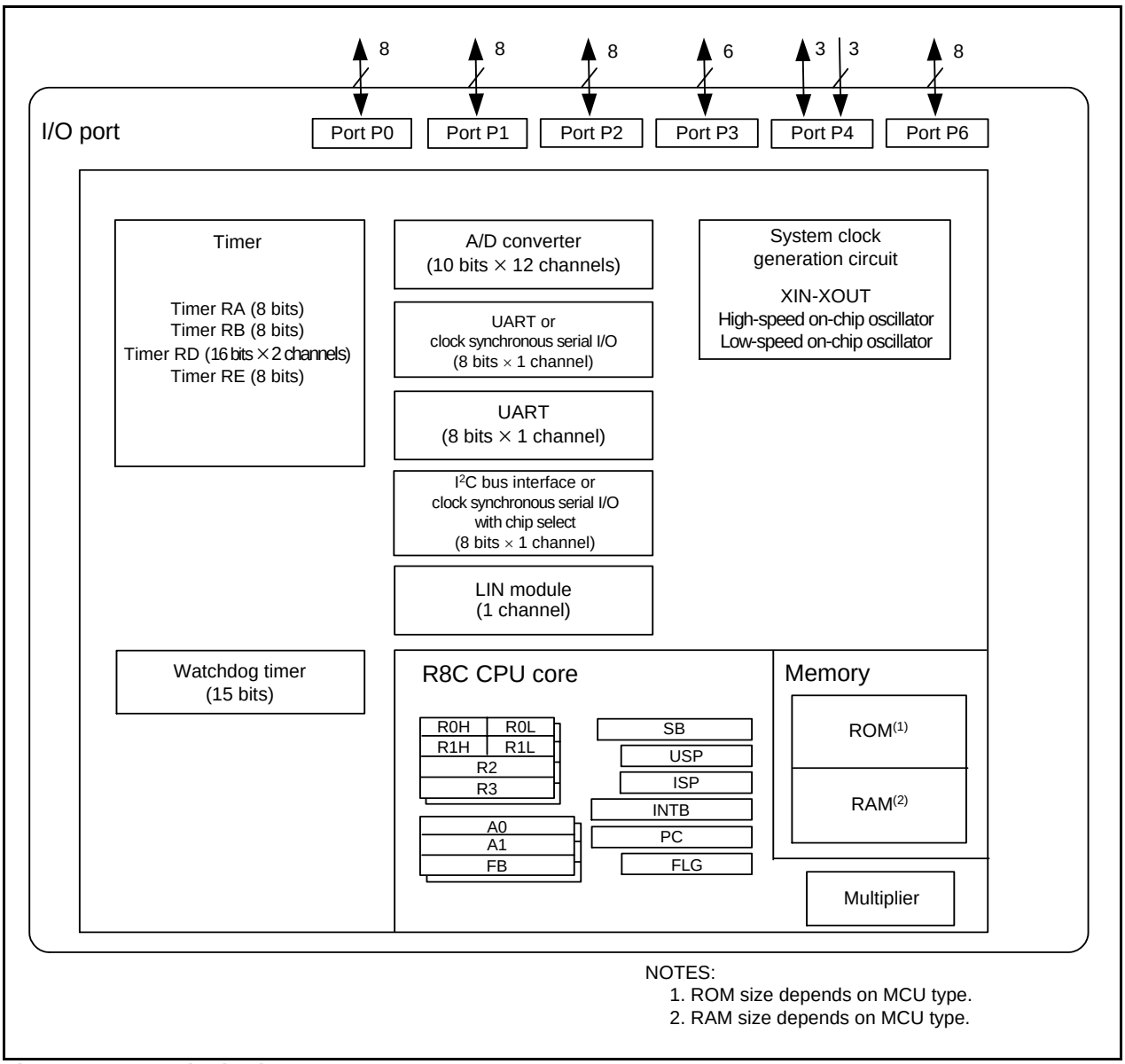


Figure 1.1 Block Diagram

Table 1.4 Product Information for R8C/21 Group **Current of Aug. 2008**

Type No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			

NOTE:
1. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **23. Notes on Emulator Debugger** of Hardware Manual.

Figure 1.3 Type Number, Memory Size, and Package of R8C/21 Group

1.5 Pin Assignments

Figure 1.4 shows Pin Assignments (Top View).

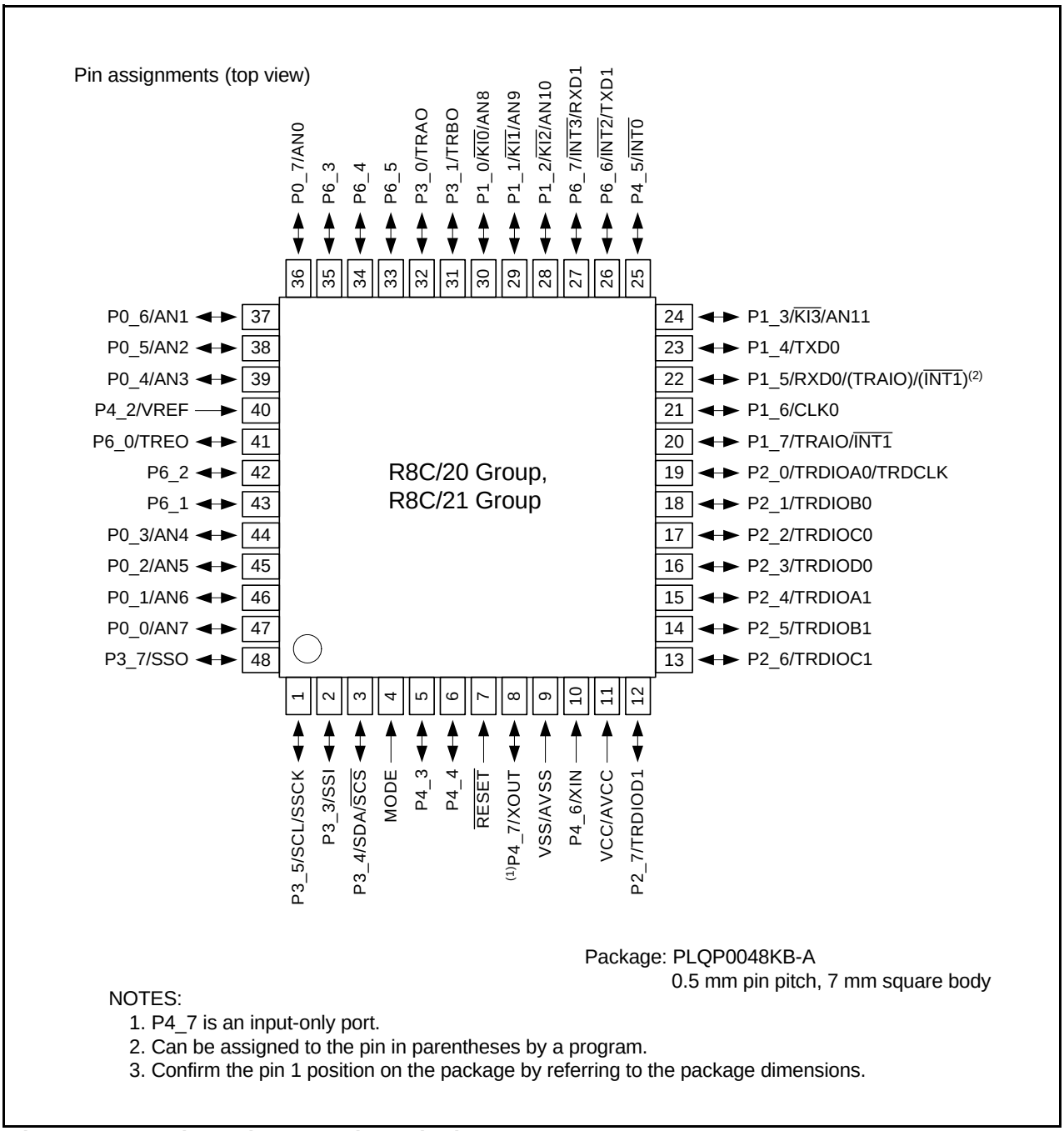


Figure 1.4 Pin Assignments (Top View)

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. Of these, R0, R1, R2, R3, A0, A1, and FB comprise a register bank. Two sets of register banks are provided.

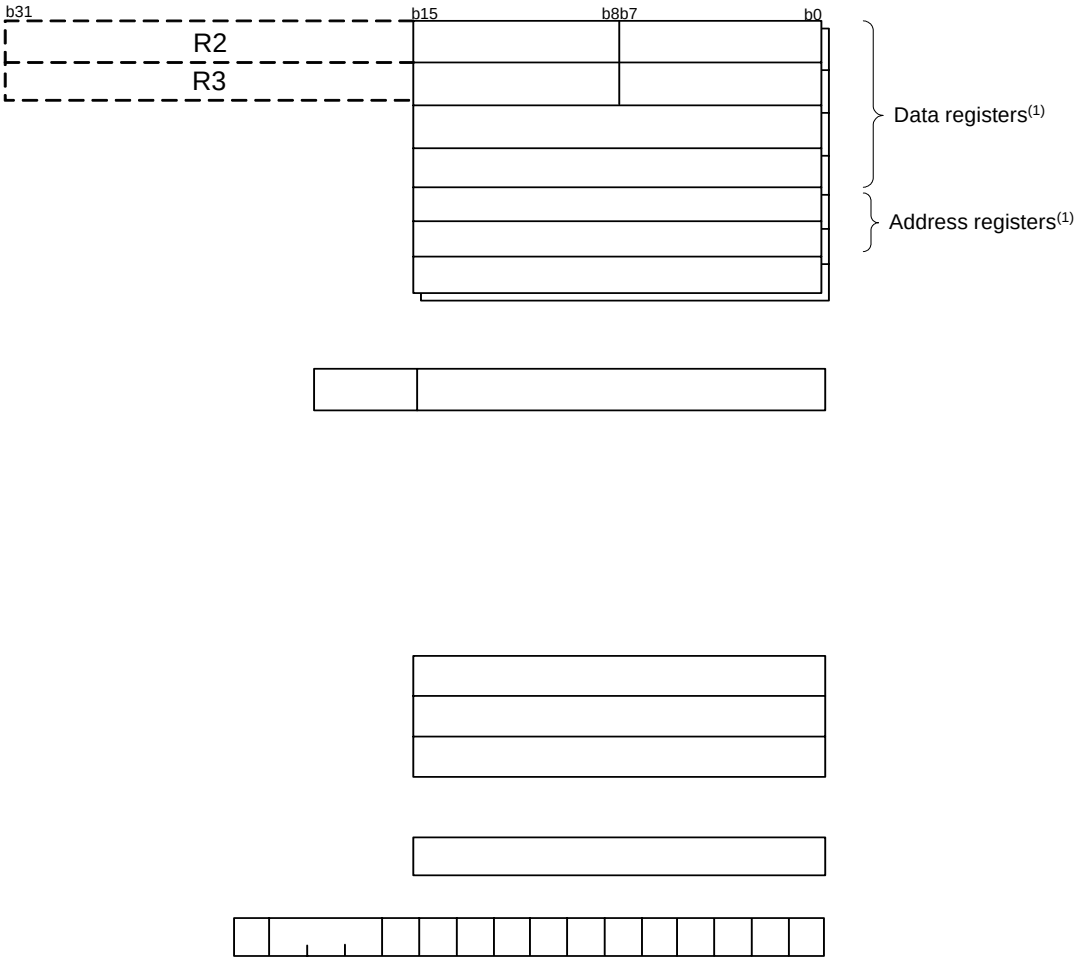


Figure 2.1 CPU Registers

2.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.
An interrupt is disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hard

Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules		
			Interrupt	Timer	Serial

NOTE:
1. Can be assigned to the pin in parentheses by a program.

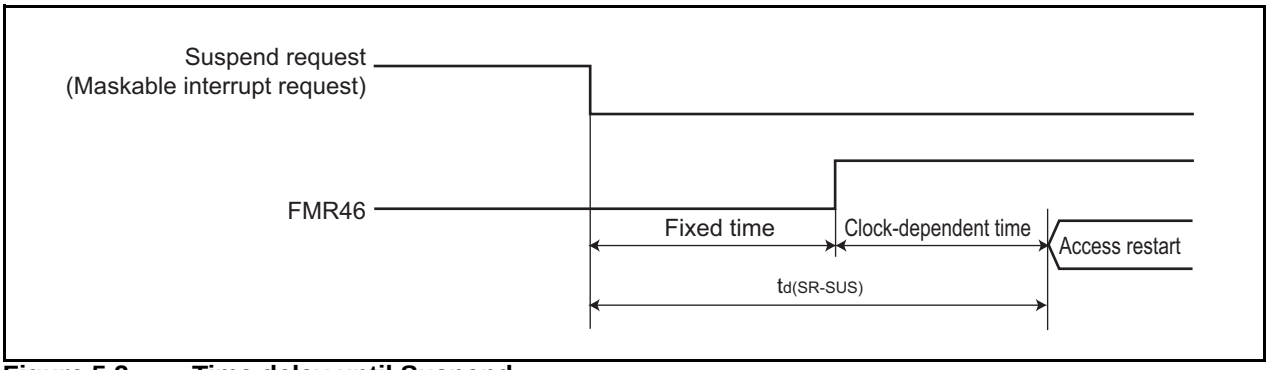


Figure 5.2 Time delay until Suspend

Table 5.6 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level(3, 4)		2.70	2.85	3.00	V
$t_{d(Vdet1-A)}$	Voltage monitor 1 reset generation time(5)		–	40	200	μs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	0.6	–	μA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(2)		–	–	100	μs
Vccmin	MCU operating voltage minimum value		2.70	–	–	V

NOTES:
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and Topr = -40°C to 85°C (J version) / -40°C to 125°C (K version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
3. Hold $V_{det2} > V_{det1}$.
4. This parameter shows the voltage detection level when the power supply drops. The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.
5. Time until the voltage monitor 1 reset is generated after the voltage passes V_{det1} when V_{CC} falls. When using the digital filter, its sampling time is added to $t_{d(Vdet1-A)}$. When using the voltage monitor 1 reset, maintain this time until V_{CC} = 2.0 V after the voltage passes V_{det1} when the power supply falls.

Table 5.7 Voltage Detection 2 Circuit Electrical Characteristics

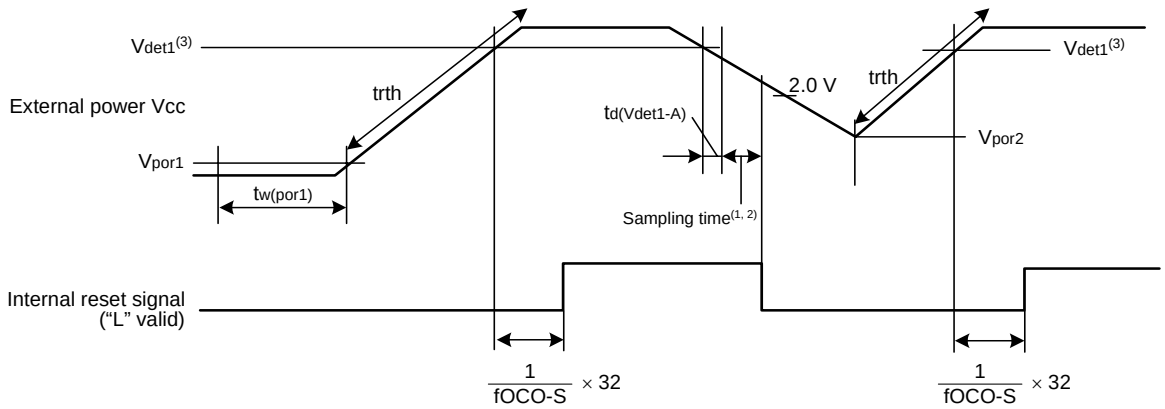
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level(4)		3.3	3.6	3.9	V
$t_{d(Vdet2-A)}$	Voltage monitor 2 reset/interrupt request generation time(2, 5)		–	40	200	μs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0V	–	0.6	–	μA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	μs

NOTES:
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and Topr = -40°C to 85°C (J version) / -40°C to 125°C (K version).
2. Time until the voltage monitor 2 reset/interrupt request is generated since the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.
4. Hold $V_{det2} > V_{det1}$.
5. When using the digital filter, its sampling time is added to $t_{d(Vdet2-A)}$. When using the voltage monitor 2 reset, maintain this time until V_{CC} = 2.0 V after the voltage passes V_{det2} when the power supply falls.

Table 5.8 Power-on Reset Circuit, Voltage Monitor 1 Reset Circuit Electrical Characteristics(3)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage(4)		–	–	0.1	V
V_{por2}	Power-on reset or voltage monitor 1 valid voltage		0	–	Vdet1	V
trth	External power V_{CC} rise gradient	$V_{CC} \leq 3.6$ V	20(2)	–	–	mV/msec
		$V_{CC} > 3.6$ V	20(2)	–	2,000	mV/msec

NOTES:
1. Topr = -40°C to 85°C (J version) / -40°C to 125°C (K version), unless otherwise specified.
2. This condition (the minimum value of external power V_{CC} rise gradient) does not apply if $V_{por2} \geq 1.0$ V.
3. To use the power-on reset function, enable voltage monitor 1 reset by setting the LVD1ON bit in the OFS register to 0, the VW1C0 and VW1C6 bits in the VW1C register to 1 respectively, and the VCA26 bit in the VCA2 register to 1.
4. $t_{w(por1)}$ indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain tw(por1) for 30s or more if -20°C ≤ Topr ≤ 125°C, maintain $t_{w(por1)}$ for 3,000s or more if -40°C ≤ Topr < -20°C.



NOTES:
1. When using the voltage monitor 1 digital filter, ensure VCC is 2.0 V or higher during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.
3. V_{det1} indicates the voltage detection level of the voltage detection 1 circuit. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.

Figure 5.3 Power-on Reset Circuit Electrical Characteristics

Table 5.12 Timing Requirements of Clock Synchronous Serial I/O with Chip Select(1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	–	t_{CYC}(2)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	μs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	μs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_H	SSO, SSI data input hold time			1	–	–	t_{CYC}(2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		$1t_{CYC}$ + 50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		$1t_{CYC}$ + 50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1	t_{CYC}(2)
t_{SA}	SSI slave access time			–	–	$1t_{CYC}$ + 100	ns
t_{OR}	SSI slave out open time			–	–	$1t_{CYC}$ + 100	ns

NOTES:
1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. $1t_{CYC}$ = 1/f1(s)

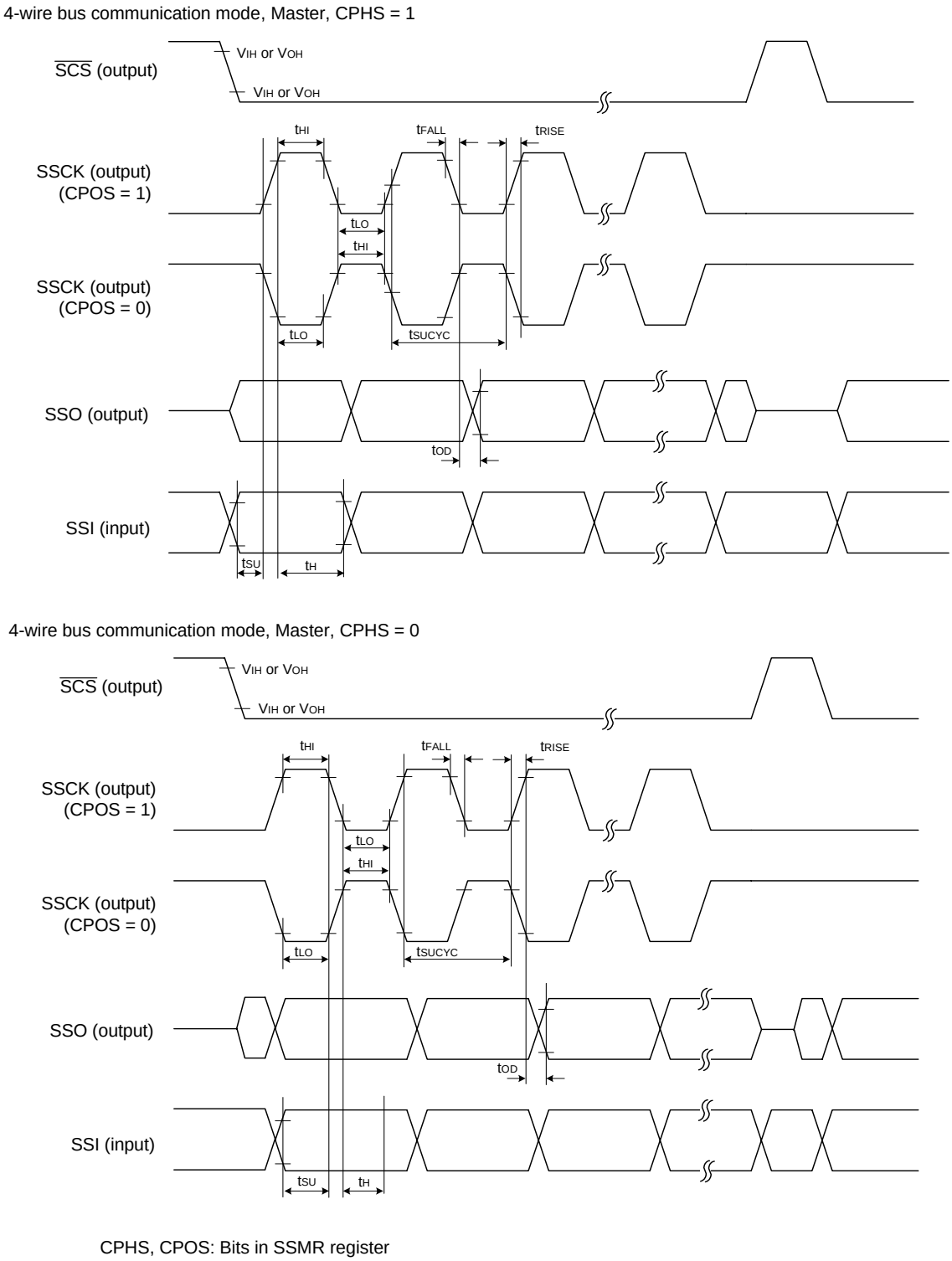


Figure 5.4 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

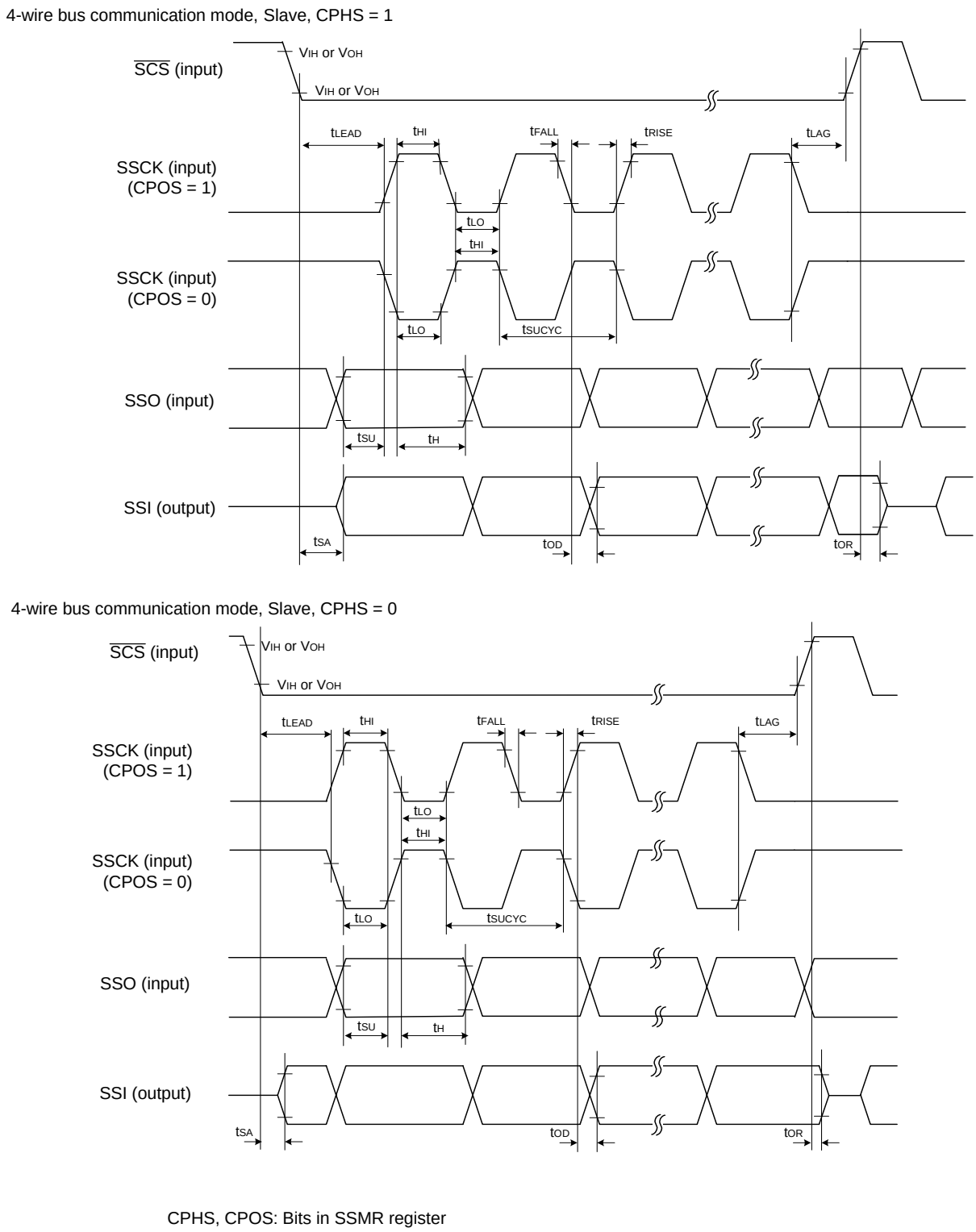


Figure 5.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

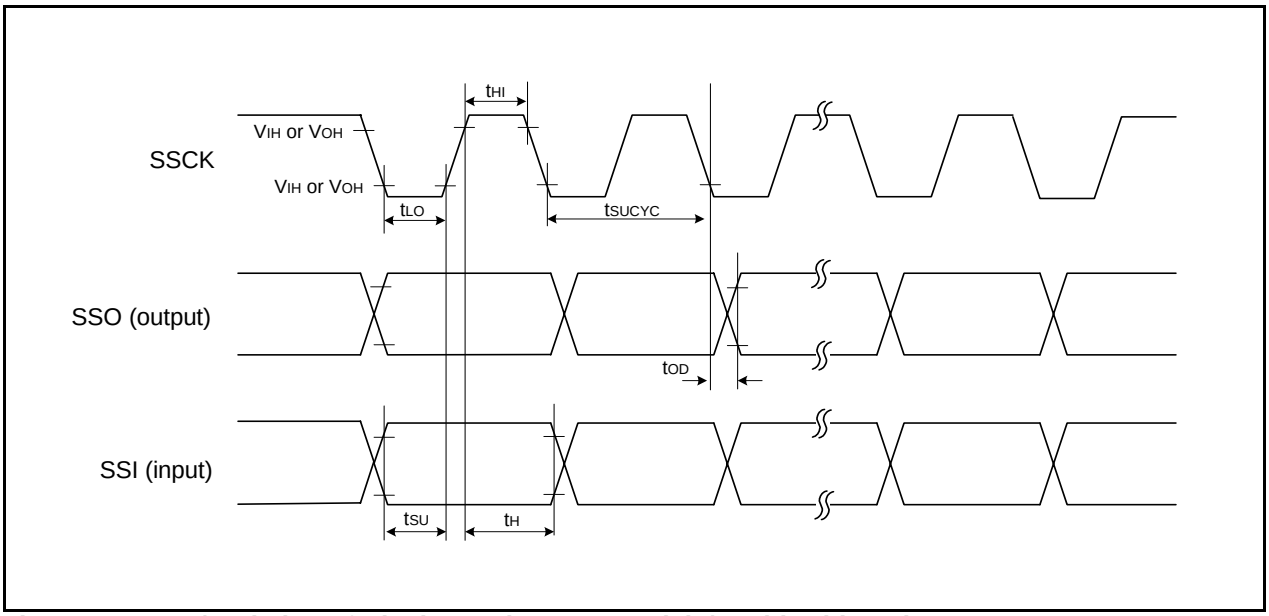


Figure 5.6 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

Table 5.14 Electrical Characteristics (1) [V_{CC} = 5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” Voltage	Except XOUT	I_{OH} = -5 mA		V_{CC} – 2.0	–	V_{CC}	V
			I_{OH} = -200 μA		V_{CC} – 0.3	–	V_{CC}	V
		XOUT	Drive capacity HIGH	I_{OH} = -1 mA	V_{CC} – 2.0	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -500 μA	V_{CC} – 2.0	–	V_{CC}	V
V_{OL}	Output “L” Voltage	Except XOUT	I_{OL} = 5 mA		–	–	2.0	V
			I_{OL} = 200 μA		–	–	0.45	V
		XOUT	Drive capacity HIGH	I_{OL} = 1 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 500 μA	–	–	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, SSI, SCL, SDA, SSO			0.1	0.5	–	V
		$\overline{RESET}$			0.1	1.0	–	V
I_{IH}	Input “H” current		VI = 5 V, V_{CC} = 5 V		–	–	5.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 5 V		–	–	-5.0	μA
R_{PULLUP}	Pull-Up Resistance		VI = 0 V, V_{CC} = 5 V		30	50	167	kΩ
R_{fXIN}	Feedback Resistance	XIN			–	1.0	–	MΩ
V_{RAM}	RAM Hold Voltage		During stop mode		2.0	–	–	V

NOTE:
1. V_{CC} = 4.2 to 5.5 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.15 Electrical Characteristics (2) [Vcc = 5 V]
(Topr = -40 to 85°C (J version) / -40 to 125°C (K version), Unless Otherwise Specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) In single-chip mode, the output pins are open and other pins are Vss	High-clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	11.0	22.0	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	8.8	17.6	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5.8	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	5.0	–	mA
			XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.8	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.8	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5.8	11.6	mA
			XIN clock off High-speed on-chip oscillator on fOCO= 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 FMR47 = 1	–	143	286	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA20 = 0 VCA26 = VCA27 = 0	–	53	106	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA20 = 0 VCA26 = VCA27 = 0	–	38	76	μA
		Stop mode Topr = 25°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	0.8	3.0	μA
		Stop mode Topr = 85°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	1.2	–	μA
		Stop mode Topr = 125°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	4.0	–	μA

Timing Requirements (Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C) [Vcc = 5 V]

Table 5.16 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input "H" width	25	–	ns
$t_{WL(XIN)}$	XIN input "L" width	25	–	ns

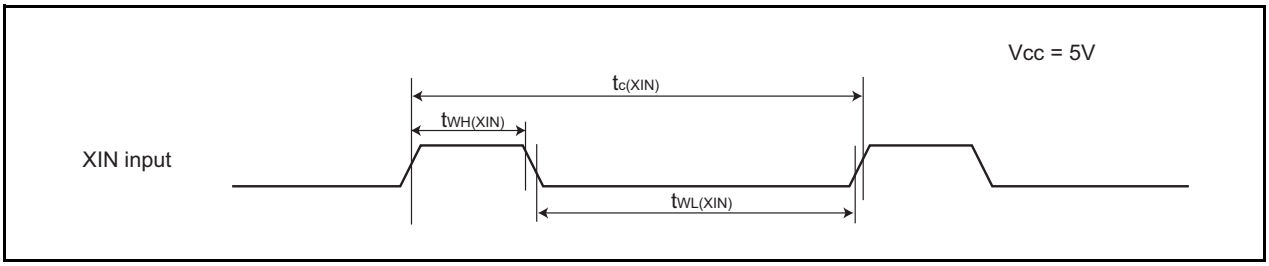


Figure 5.8 XIN Input Timing Diagram when Vcc = 5 V

Table 5.17 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	40	–	ns

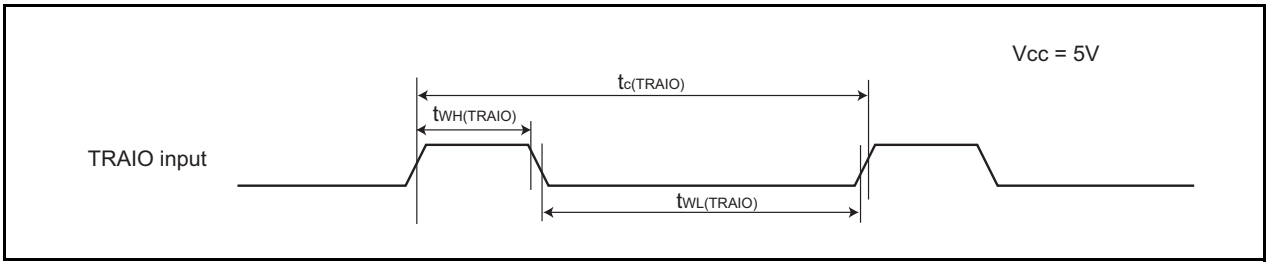


Figure 5.9 TRAIO Input Timing Diagram when Vcc = 5 V

Table 5.18 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	200	–	ns
$t_{W(CKH)}$	CLK0 input “H” width	100	–	ns
$t_{W(CKL)}$	CLK0 input “L” width	100	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	50	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

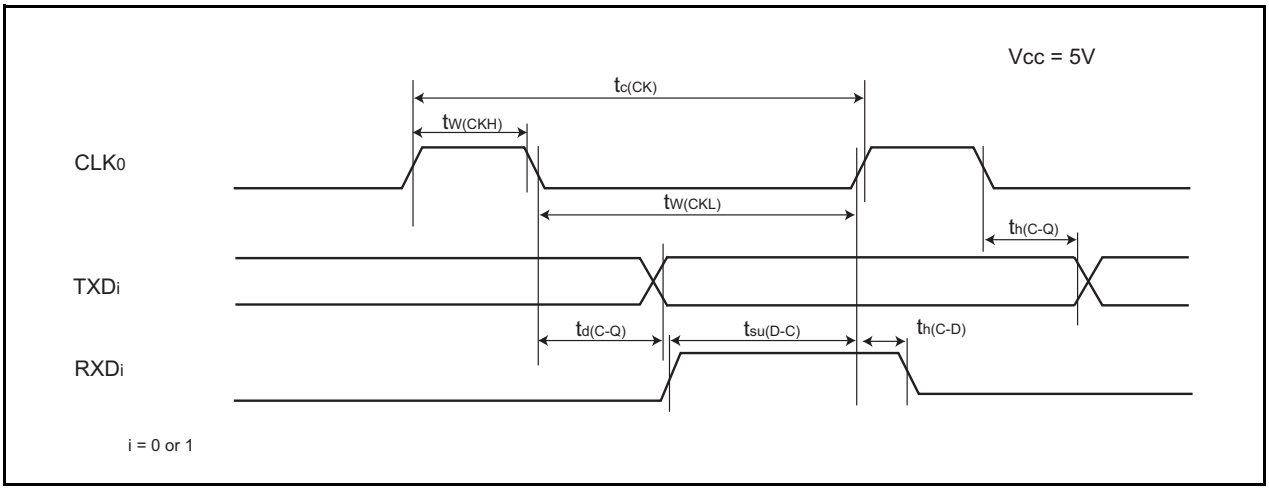


Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.19 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	250(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	250(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input HIGH width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input LOW width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.

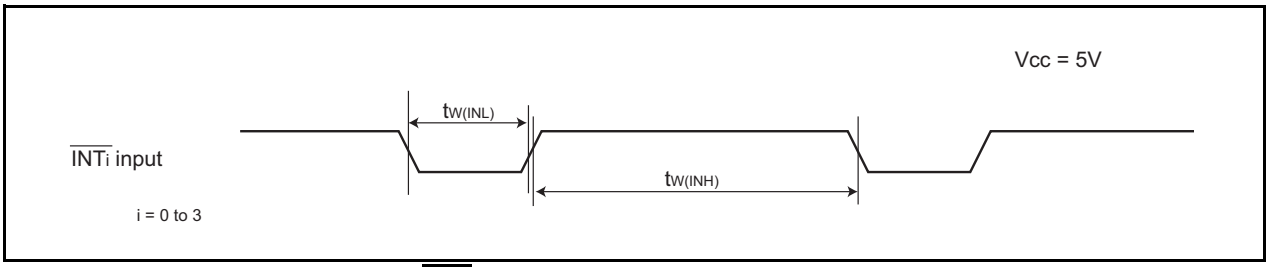


Figure 5.11 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 5 V (i = 0 to 3)

REVISION HISTORY	R8C/20 Group, R8C/21 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Mar 08, 2005	–	First Edition issued
0.20	Sep 29, 2005	–	Words standardized - Clock synchronous serial interface → Clock synchronous serial I/O - Chip-select clock synchronous interface(SSU) → Clock synchronous serial I/O with chip select - I^2C bus interface(IIC) → I^2C bus interface
		2, 3	Table1.1 R8C/20 Group Performance, Table1.2 R8C/21 Group Performance Serial Interface revised: - Clock Synchronous Serial Interface: 1 channel I^2C bus Interface (3), Clock synchronous serial I/O with chip select - Power-On Reset Circuit added - Power Consumption value determined
		5, 6	Table 1.3 Product Information of R8C/20 Group, Table 1.4 Product Information of R8C/21 Group Date revised.
		7	Figure 1.4 Pin Assignment Pin name revised: - P3_5/$\overline{\text{SSC}}$K(/SCL) → P3_5/ SCL/$\overline{\text{SSC}}$K - P3_4/$\overline{\text{SCS}}$(/SDA) → P3_4/ SDA /$\overline{\text{SCS}}$ - VSS → VSS/AVSS - VCC → VCC/AVCC - P1_5/$\overline{\text{RXD}}$0/(TRAIO/$\overline{\text{INT}}$1) → P1_5/RXD0/(TRAIO)/($\overline{\text{INT}}$1) - P6_6/$\overline{\text{INT}}$2/(TXD1) → P6_6/$\overline{\text{INT}}$2/TXD1 - P6_7/$\overline{\text{INT}}$3/(RXD1) → P6_7/$\overline{\text{INT}}$3/RXD1 - NOTE2 added
		8	Table 1.5 Pin Description - Analog Power Supply Input: line added - I^2C Bus Interface (IIC) → I^2C Bus Interface - SSU → Clock Synchronous Serial I/O with Chip Select
		9	Table 1.6 Pin Name Information by Pin Number revised - Pin Number 1: (SCL) → SCL - Pin Number 2: (SDA) → SDA - Pin Number 9: VSS → VSS/AVSS - Pin Number 11: VCC → VCC/AVCC - Pin Number 26: (TXD1) → TXD1 - Pin Number 27: (RXD1) → RXD1
		15	Table 4.1 SFR Information (1) revised - 0013h: XXXXXX00b → 00h
		17	Table 4.3 SFR Information (3) revised - 00BCh: 0000X000b → 00h/0000X000b
		18	Table 4.4 SFR Information (4) revised - 00D6h: 00000XXXb → 00h - 00F5h: UART1 Function Select Register added
		19	Table 4.5 SFR Information (5) revised - 0104h: TRATR → TRA

REVISION HISTORY	R8C/20 Group, R8C/21 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Nov 15, 2006	33	Table 5.15 Electrical Characteristics (1) [VCC = 5 V] → Table 5.14 Electrical Characteristics (1) [VCC = 5 V] revised. RAM Hold Voltage, Min.; “1.8” → “2.0” corrected.
		34	Table 5.16 Electrical Characteristics (2) [Vcc = 5 V] → Table 5.15 Electrical Characteristics (2) [Vcc = 5 V] revised. Wait mode revised.
		37	Table 5.21 Electrical Characteristics (3) [VCC = 3 V → Table 5.20 Electrical Characteristics (3) [VCC = 3 V] revised. RAM hold voltage, Min.;“1.8” → “2.0” corrected.
		38	Table 5.22 Electrical Characteristics (4) [Vcc = 3 V] → Table 5.21 Electrical Characteristics (4) [Vcc = 3 V] revised. Wait mode revised.
2.00	Aug 27, 2008	–	“RENESAS TECHNICAL UPDATE” reflected: TN-16C-A172A/E
		5, 6	Table 1.3, Table 1.4 revised Figure 1.2, Figure 1.3; ROM number “XXX” added
		13, 14	Figure 3.1, Figure 3.2; “Expanding area” deleted
		21	Table 5.2; NOTE2 revised
		23	Table 5.4; NOTE2 and NOTE4 revised
		24	Table 5.5; NOTE2 and NOTE5 revised
		25	Table 5.6; “td(Vdet1-A)” added, NOTE5 added Table 5.7; “td(Vdet2-A)” and NOTE2 revised, NOTE5 added
		26	Table 5.8; “trth” and NOTE2 revised Figure 5.3 revised

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