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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	5K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2121akfp-u0

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R8C/20 Group, R8C/21 Group

RENESAS MCU

REJ03B0120-0200
Rev.2.00
Aug 27, 2008

1. Overview

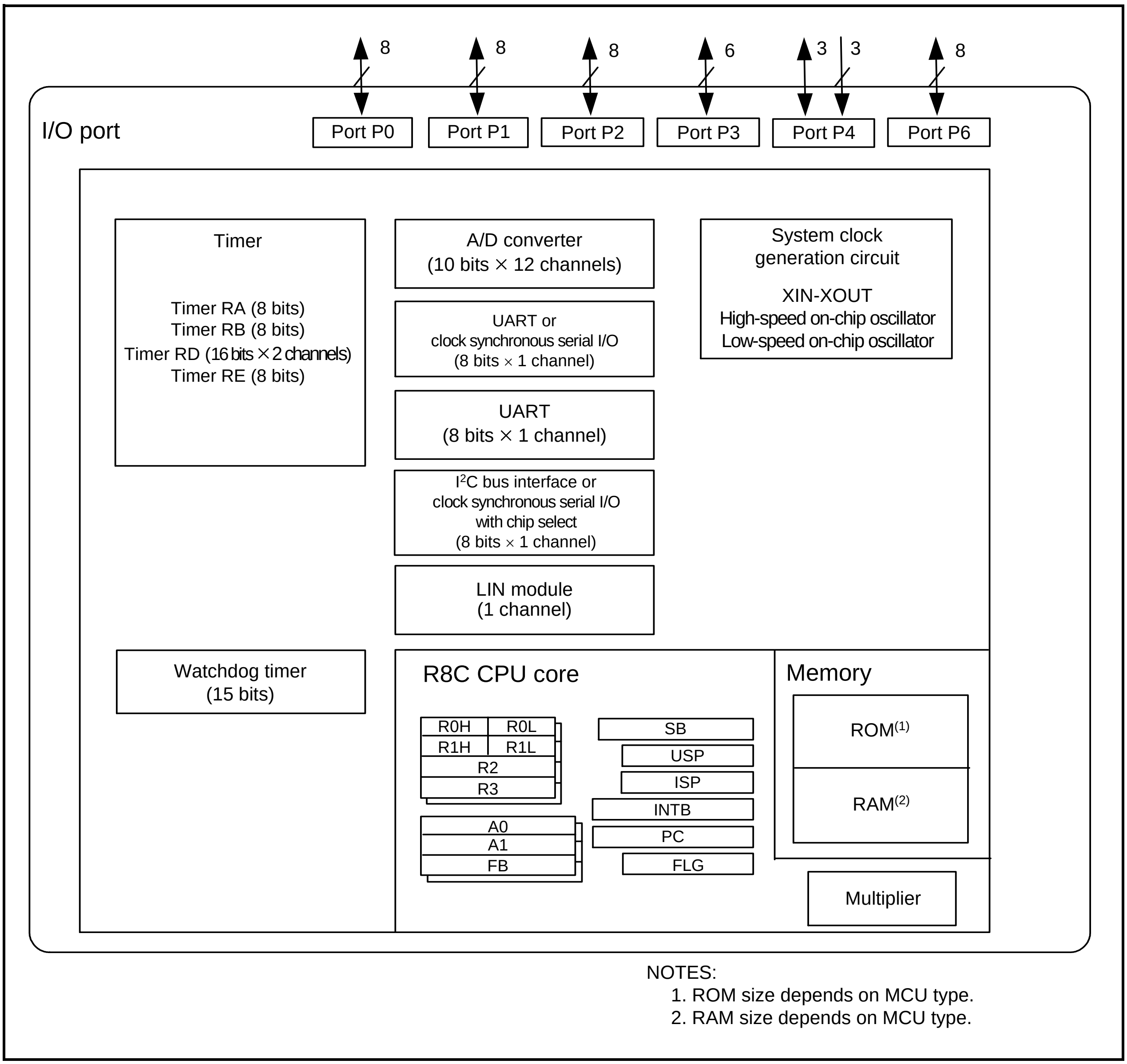
This MCU is built using the high-performance silicon gate CMOS process using the R8C CPU core and is packaged in a 48-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1 Mbyte of address space, it is capable of executing instructions at high speed. This Furthermore, the data flash (1 KB x 2 blocks) is embedded in the R8C/21 Group.
The difference between R8C/20 and R8C/21 Groups is only the existence of the data flash. Their peripheral functions are the same.

1.1 Applications

Automotive, etc.

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.



NOTES:
1. ROM size depends on MCU type.
2. RAM size depends on MCU type.

Figure 1.1 Block Diagram

1.4 Product Information

Table 1.3 lists Product Information for R8C/20 Group and Table 1.4 lists Product Information for R8C/21 Group.

Table 1.3 Product Information for R8C/20 Group **Current of Aug. 2008**

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks	
R5F21206JFP	32 Kbytes	2 Kbytes	PLQP0048KB-A	J version	Flash memory version
R5F21207JFP	48 Kbytes	2.5 Kbytes	PLQP0048KB-A		
R5F21208JFP	64 Kbytes	3 Kbytes	PLQP0048KB-A		
R5F2120AJFP	96 Kbytes	5 Kbytes	PLQP0048KB-A		
R5F2120CJFP	128 Kbytes(1)	6 Kbytes	PLQP0048KB-A		
R5F21206KFP	32 Kbytes	2 Kbytes	PLQP0048KB-A	K version	
R5F21207KFP	48 Kbytes	2.5 Kbytes	PLQP0048KB-A		
R5F21208KFP	64 Kbytes	3 Kbytes	PLQP0048KB-A		
R5F2120AKFP	96 Kbytes	5 Kbytes	PLQP0048KB-A		
R5F2120CKFP	128 Kbytes(1)	6 Kbytes	PLQP0048KB-A		

NOTE:

1. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **23. Notes on Emulator Debugger** of Hardware Manual.

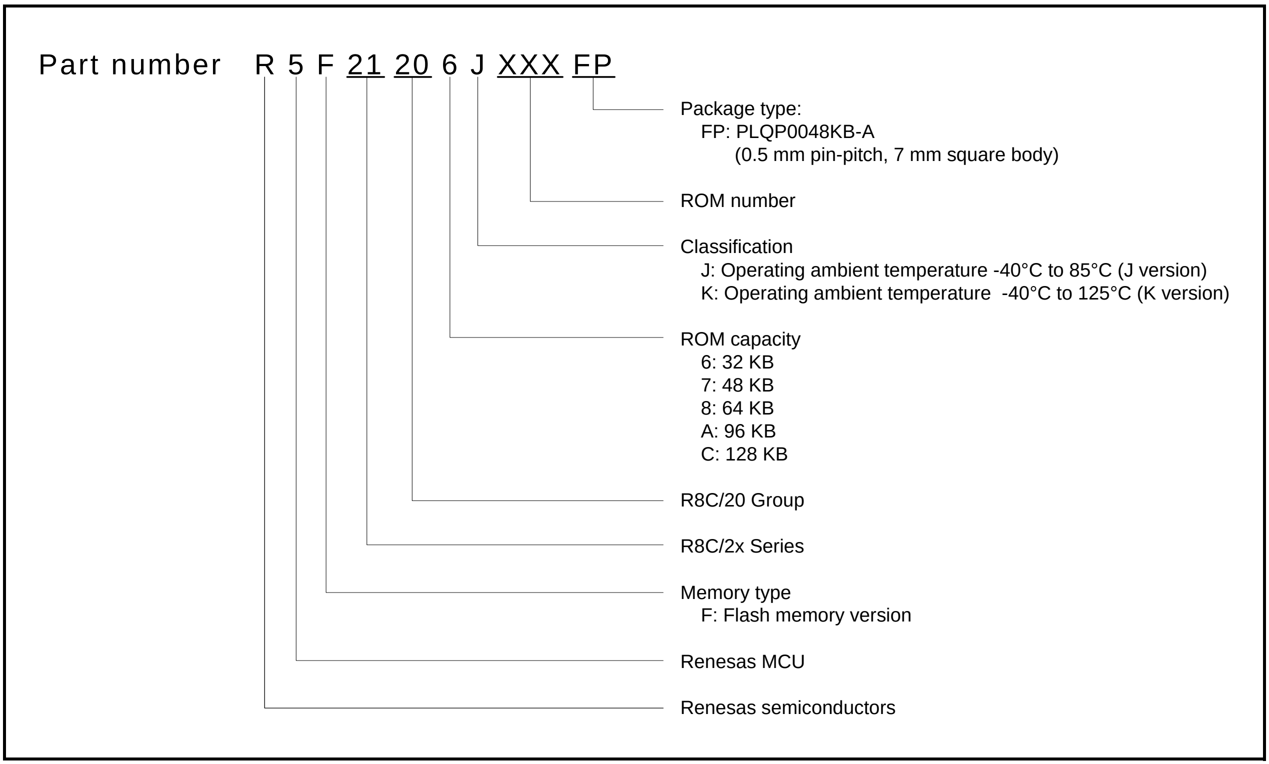
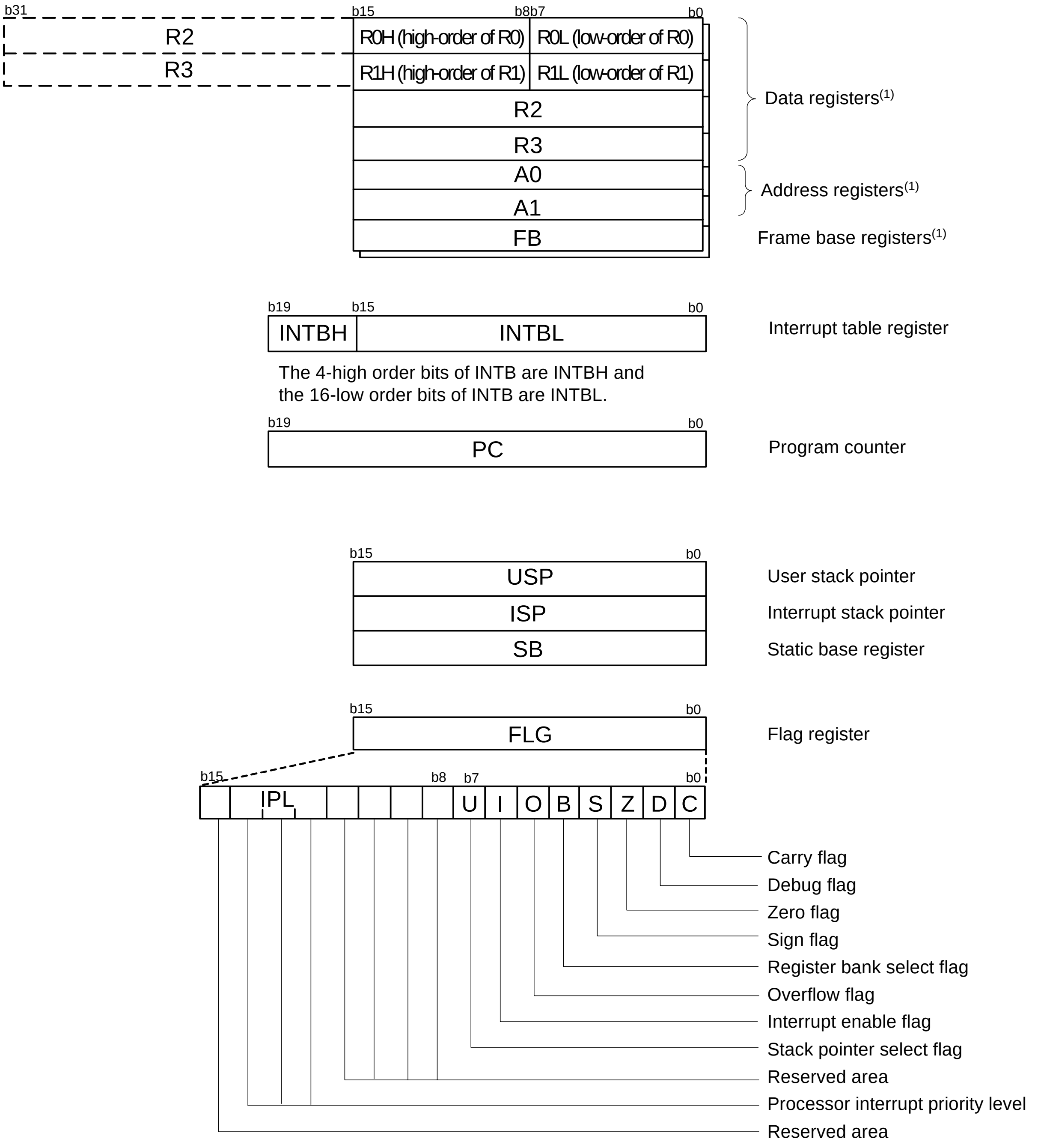


Figure 1.2 Type Number, Memory Size, and Package of R8C/20 Group

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. Of these, R0, R1, R2, R3, A0, A1, and FB comprise a register bank. Two sets of register banks are provided.



NOTE:
1. A register bank comprises these registers. Two sets of register banks are provided.

Figure 2.1 CPU Registers

Table 4.2 SFR Information (2)(1)

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h			
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register/IIC Bus Interrupt Control Register(2)	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.3 SFR Information (3)(1)

Address	Register	Symbol	After reset
0080h			
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h			
0089h			
008Ah			
008Bh			
008Ch			
008Dh			
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART1 Transmit/Receive Mode Register	U1MR	00h
00A9h	UART1 Bit Rate Register	U1BRG	XXh
00AAh	UART1 Transmit Buffer Register	U1TB	XXh
00ABh			XXh
00ACh	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
00ADh	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
00AEh	UART1 Receive Buffer Register	U1RB	XXh
00AFh			XXh
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h	SS Control Register H/IIC Bus Control Register 1(2)	SSCRH/ICCR1	00h
00B9h	SS Control Register L/IIC Bus Control Register 2(2)	SSCRL/ICCR2	01111101b
00BAh	SS Mode Register/IIC Bus Mode Register 1(2)	SSMR/ICMR	00011000b
00BBh	SS Enable Register/IIC Bus Interrupt Enable Register(2)	SSER/ICIER	00h
00BCh	SS Status Register/IIC Bus Status Register(2)	SSSR/ICSR	00h/0000X000b
00BDh	SS Mode Register 2/Slave Address Register(2)	SSMR2/SAR	00h
00BEh	SS Transmit Data Register/IIC Bus Transmit Data Register(2)	SSTDR/ICDRT	FFh
00BFh	SS Receive Data Register/IIC Bus Receive Data Register(2)	SSRDR/ICDRR	FFh

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.6 SFR Information (6)[1]

Address	Register	Symbol	After reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIORA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIORA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			
FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
V_{CC}/AV_{CC}	Supply voltage		-0.3 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC}+0.3	V
V_O	Output voltage		-0.3 to V_{CC}+0.3	V
P_d	Power dissipation	-40°C ≤ Topr ≤ 85°C	300	mW
		85°C < Topr ≤ 125°C	125	mW
T_{opr}	Operating ambient temperature		-40 to 85 (J version) / -40 to 125 (K version)	°C
T_{stg}	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage			2.7	–	5.5	V
V_{SS}/AV_{CC}	Supply voltage			–	0	–	V
V_{IH}	Input "H" voltage			0.8V_{CC}	–	V_{CC}	V
V_{IL}	Input "L" voltage			0	–	0.2V_{CC}	V
$I_{OH(sum)}$	Peak sum output "H" current	Sum of all Pins $I_{OH (peak)}$		–	–	-60	mA
$I_{OH(peak)}$	Peak output "H" current			–	–	-10	mA
$I_{OH(avg)}$	Average output "H" current			–	–	-5	mA
$I_{OL(sum)}$	Peak sum output "L" currents	Sum of all Pins $I_{OL (peak)}$		–	–	60	mA
$I_{OL(peak)}$	Peak output "L" currents			–	–	10	mA
$I_{OL(avg)}$	Average output "L" current			–	–	5	mA
f(XIN)	XIN clock input oscillation frequency		3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	0	–	20	MHz
			3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 125°C	0	–	16	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
–	System clock	OCD2 = 0 When XIN clock is selected.	3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	0	–	20	MHz
			3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 125°C	0	–	16	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
		OCD2 = 1 When on-chip oscillator clock is selected.	FRA01 = 0 When low-speed on-chip oscillator clock is selected.	–	125	–	kHz
			FRA01 = 1 When high-speed on-chip oscillator clock is selected. 3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	–	–	20	MHz
			FRA01 = 1 When high-speed on-chip oscillator clock is selected.	–	–	10	MHz

NOTES:

1. V_{CC} = 2.7 to 5.5 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance[2]	R8C/20 Group	100[3]	–	–	times
		R8C/21 Group	1,000[3]	–	–	times
–	Byte program time		–	50	400	µs
–	Block erase time		–	0.4	9	s
$t_{d(SR-SUS)}$	Time delay from suspend request until erase suspend		–	–	97 + CPU clock × 6 cycle	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3 + CPU clock × 4 cycle	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time[7]	Ambient temperature = 55°C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 1,000), each block can be erased n times.
   For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure endurance can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.5 Flash Memory (Data Flash Block A, Block B) Electrical Characteristics(4)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)		10,000(3)	–	–	times
–	Byte program time (Program/erase endurance ≤ 1,000 times)		–	50	400	µs
–	Byte program time (Program/erase endurance > 1,000 times)		–	65	–	µs
–	Block erase time (Program/erase endurance ≤ 1,000 times)		–	0.2	9	s
–	Block erase time (Program/erase endurance > 1,000 times)		–	0.3	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until erase suspend		–	–	97 + CPU clock × 6 cycle	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3 + CPU clock × 4 cycle	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		-40	–	85(8)	°C
–	Data hold time(9)	Ambient temperature = 55°C	20	–	–	year

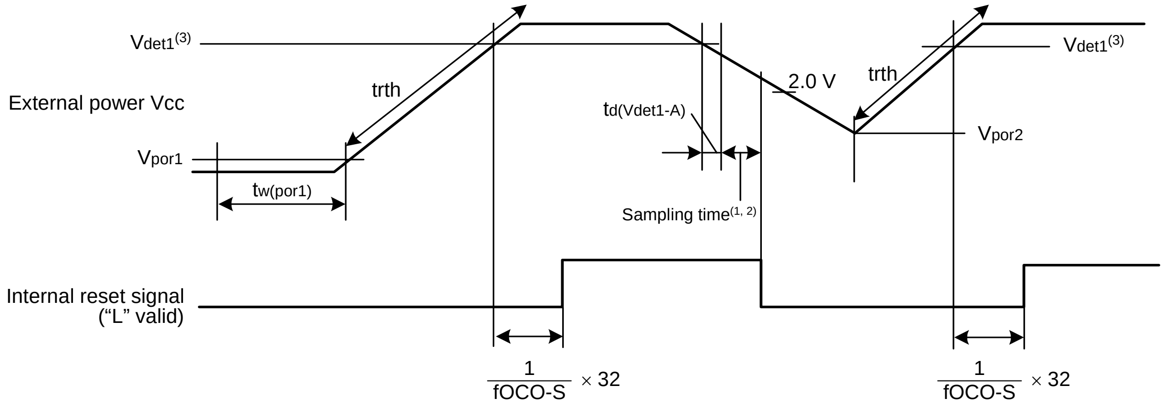
NOTES:

1. V_{CC} = 2.7 to 5.5 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times.
   For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. MInimum endurance to guarantee all electrical characteristics after program and erase (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times are the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure endurance can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
6. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. 125°C for K version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.8 Power-on Reset Circuit, Voltage Monitor 1 Reset Circuit Electrical Characteristics(3)

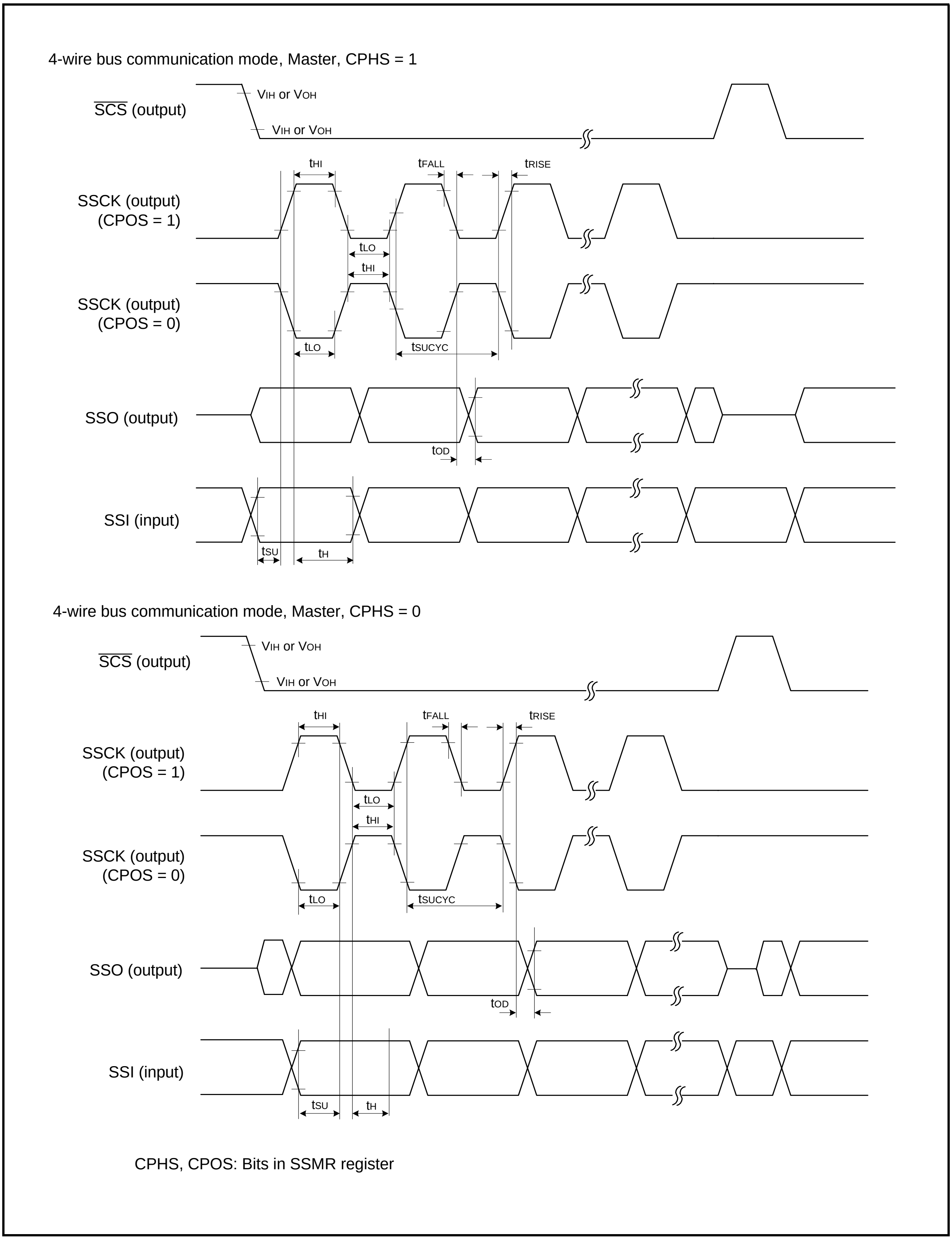
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage(4)		–	–	0.1	V
V_{por2}	Power-on reset or voltage monitor 1 valid voltage		0	–	Vdet1	V
trth	External power V_{CC} rise gradient	$V_{CC} \le 3.6$ V	20(2)	–	–	mV/msec
		$V_{CC} > 3.6$ V	20(2)	–	2,000	mV/msec

NOTES:
1. Topr = -40°C to 85°C (J version) / -40°C to 125°C (K version), unless otherwise specified.
2. This condition (the minimum value of external power V_{CC} rise gradient) does not apply if $V_{por2} \ge 1.0$ V.
3. To use the power-on reset function, enable voltage monitor 1 reset by setting the LVD1ON bit in the OFS register to 0, the VW1C0 and VW1C6 bits in the VW1C register to 1 respectively, and the VCA26 bit in the VCA2 register to 1.
4. $t_{w(por1)}$ indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain tw(por1) for 30s or more if -20°C ≤ Topr ≤ 125°C, maintain $t_{w(por1)}$ for 3,000s or more if -40°C ≤ Topr < -20°C.



NOTES:
1. When using the voltage monitor 1 digital filter, ensure VCC is 2.0 V or higher during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.
3. V_{det1} indicates the voltage detection level of the voltage detection 1 circuit. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.

Figure 5.3 Power-on Reset Circuit Electrical Characteristics



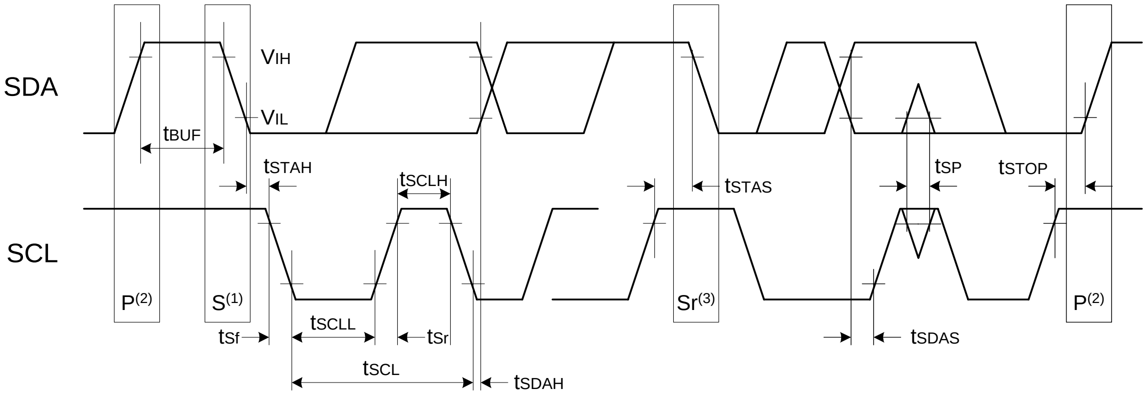
CPHS, CPOS: Bits in SSMR register

Figure 5.4 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

Table 5.13 Timing Requirements of I²C Bus Interface(1)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC}$ + 600(2)	–	–	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC}$ + 300(2)	–	–	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC}$ + 300(2)	–	–	ns
t_{sf}	SCL, SDA input falling time		–	–	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		–	–	$1t_{CYC}$(2)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$(2)	–	–	ns
t_{STAH}	Start condition input hole time		$3t_{CYC}$(2)	–	–	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$(2)	–	–	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$(2)	–	–	ns
t_{SOAS}	Data input setup time		$1t_{CYC}$ + 20(2)	–	–	ns
t_{SDAH}	Data input hold time		0	–	–	ns

NOTES:
1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
2. $1t_{CYC}$ = 1/f1(s)



NOTES:
1. Start condition
2. Stop condition
3. Retransmit “Start” condition

Figure 5.7 I/O Timing of I²C Bus Interface

Table 5.15 Electrical Characteristics (2) [VCC = 5 V]
(Topr = -40 to 85°C (J version) / -40 to 125°C (K version), Unless Otherwise Specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 3.3 to 5.5 V) In single-chip mode, the output pins are open and other pins are VSS	High-clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	11.0	22.0	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	8.8	17.6	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5.8	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	5.0	–	mA
			XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.8	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.8	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5.8	11.6	mA
			XIN clock off High-speed on-chip oscillator on fOCO= 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 FMR47 = 1	–	143	286	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA20 = 0 VCA26 = VCA27 = 0	–	53	106	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA20 = 0 VCA26 = VCA27 = 0	–	38	76	µA
		Stop mode Topr = 25°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	0.8	3.0	µA
		Stop mode Topr = 85°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	1.2	–	µA
		Stop mode Topr = 125°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	4.0	–	µA

Timing Requirements (Unless Otherwise Specified: VCC = 5 V, VSS = 0 V at Topr = 25°C) [VCC = 5 V]

Table 5.16 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	25	–	ns
$t_{WL(XIN)}$	XIN input “L” width	25	–	ns

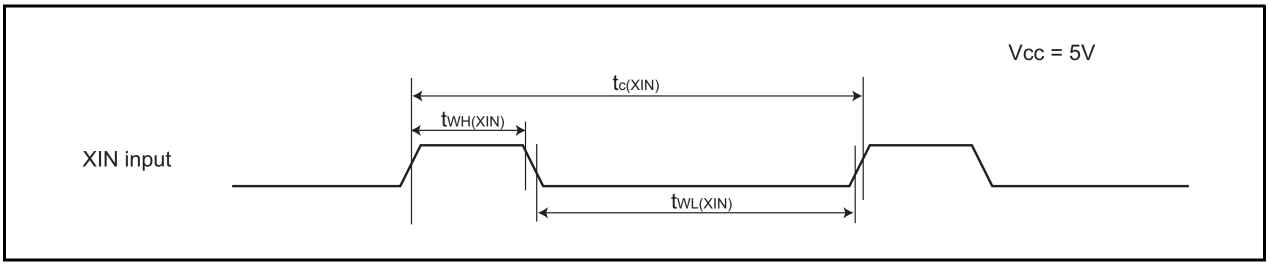


Figure 5.8 XIN Input Timing Diagram when VCC = 5 V

Table 5.17 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

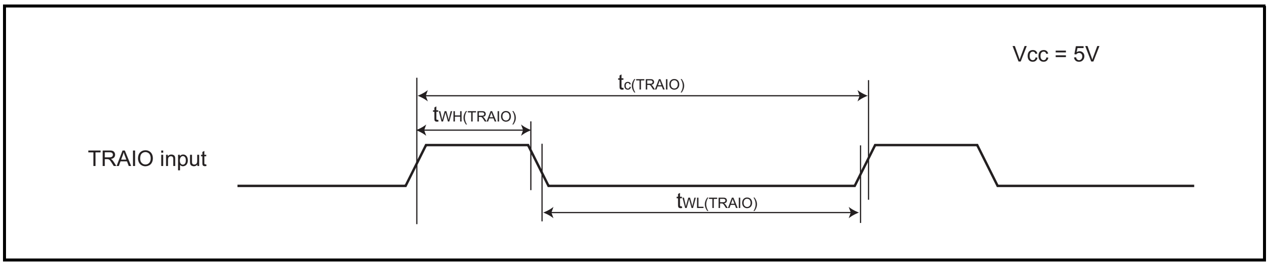


Figure 5.9 TRAIO Input Timing Diagram when VCC = 5 V

Table 5.21 Electrical Characteristics (4) [VCC = 3 V]
(Topr = -40 to 85°C (J version) / -40 to 125°C (K version), Unless Otherwise Specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 2.7 to 3.3 V) In single-chip mode, the output pins are open and other pins are VSS	High-clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	10.5	21.0	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	8.3	16.6	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5.3	10.6	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4.5	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.3	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.3	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5.6	11.2	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.4	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 FMR47 = 1	–	138	276	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA20 = 0 VCA26 = VCA27 = 0	–	48	96	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA20 = 0 VCA26 = VCA27 = 0	–	35	70	µA
		Stop mode Topr = 25°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	0.7	3.0	µA
		Stop mode Topr = 85°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	1.1	–	µA
		Stop mode Topr = 125°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	3.8	–	µA

Timing Requirements (Unless Otherwise Specified: V_{CC} = 3 V, V_{SS} = 0V at Topr = 25°C) [V_{CC} = 3 V]

Table 5.22 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input “H” width	40	–	ns
$t_{WL(XIN)}$	XIN input “L” width	40	–	ns

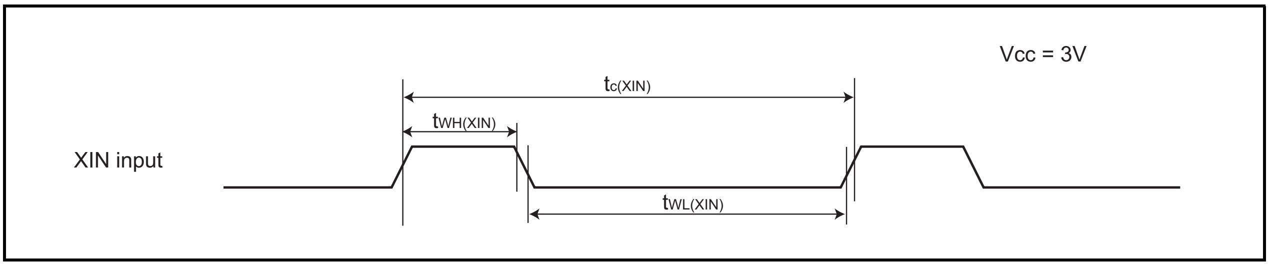


Figure 5.12 XIN Input Timing Diagram when V_{CC} = 3 V

Table 5.23 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input Cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

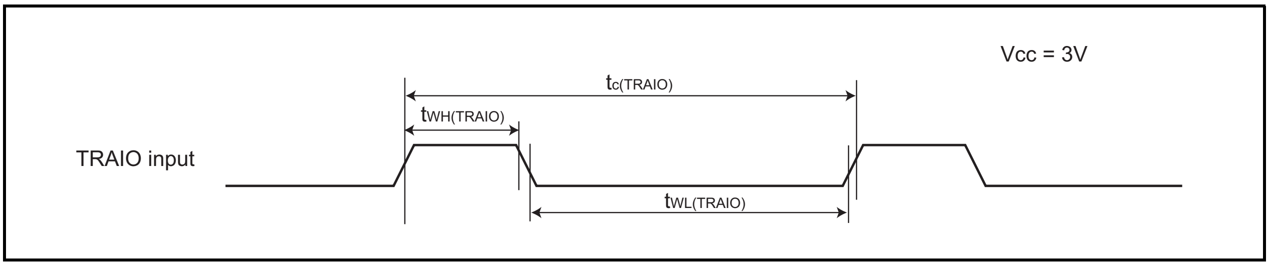


Figure 5.13 TRAIO Input Timing Diagram when V_{CC} = 3 V

Table 5.24 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	300	–	ns
$t_{W(CKH)}$	CLK0 input “H” width	150	–	ns
$t_{W(CKL)}$	CLK0 input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

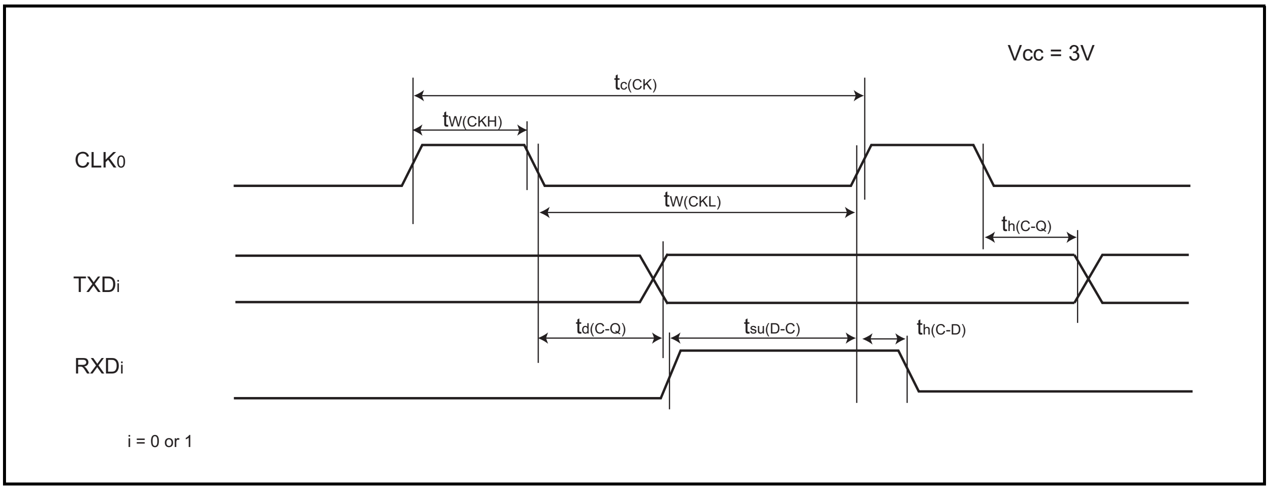


Figure 5.14 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.25 External Interrupt $\overline{\text{INTi}}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{\text{INTi}}$ input “H” width	380[1]	–	ns
$t_{W(INL)}$	$\overline{\text{INTi}}$ input “L” width	380[2]	–	ns

NOTES:

1. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use the $\overline{\text{INTi}}$ input HIGH width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use the $\overline{\text{INTi}}$ input LOW width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.

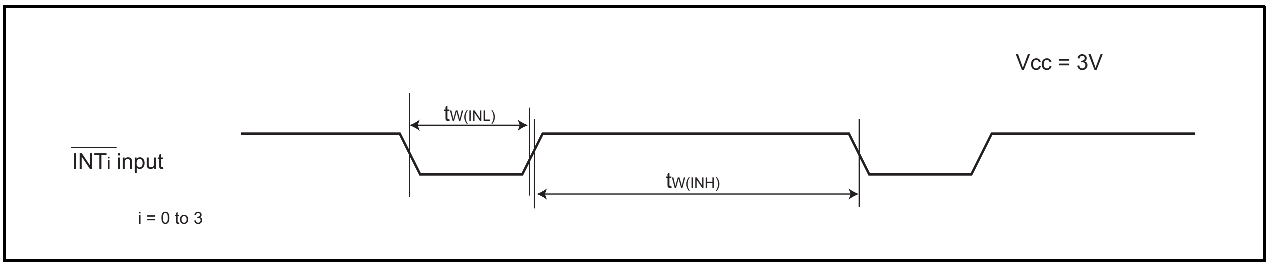


Figure 5.15 External Interrupt $\overline{\text{INTi}}$ Input Timing Diagram when Vcc = 3 V (i = 0 to 3)

REVISION HISTORY	R8C/20 Group, R8C/21 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Mar 08, 2005	–	First Edition issued
0.20	Sep 29, 2005	–	Words standardized - Clock synchronous serial interface → Clock synchronous serial I/O - Chip-select clock synchronous interface(SSU) → Clock synchronous serial I/O with chip select - I^2C bus interface(IIC) → I^2C bus interface
		2, 3	Table1.1 R8C/20 Group Performance, Table1.2 R8C/21 Group Performance Serial Interface revised: - Clock Synchronous Serial Interface: 1 channel I^2C bus Interface (3), Clock synchronous serial I/O with chip select - Power-On Reset Circuit added - Power Consumption value determined
		5, 6	Table 1.3 Product Information of R8C/20 Group, Table 1.4 Product Information of R8C/21 Group Date revised.
		7	Figure 1.4 Pin Assignment Pin name revised: - P3_5/SSCK(/SCL) → P3_5/ SCL/SSCK - P3_4/$\overline{\text{SCS}}$(/SDA) → P3_4/ SDA /$\overline{\text{SCS}}$ - VSS → VSS/AVSS - VCC → VCC/AVCC - P1_5/RXD0/(TRAIO/$\overline{\text{INT1}}$) → P1_5/RXD0/(TRAIO)/($\overline{\text{INT1}}$) - P6_6/$\overline{\text{INT2}}$/(TXD1) → P6_6/$\overline{\text{INT2}}$/TXD1 - P6_7/$\overline{\text{INT3}}$/(RXD1) → P6_7/$\overline{\text{INT3}}$/RXD1 - NOTE2 added
		8	Table 1.5 Pin Description - Analog Power Supply Input: line added - I^2C Bus Interface (IIC) → I^2C Bus Interface - SSU → Clock Synchronous Serial I/O with Chip Select
		9	Table 1.6 Pin Name Information by Pin Number revised - Pin Number 1: (SCL) → SCL - Pin Number 2: (SDA) → SDA - Pin Number 9: VSS → VSS/AVSS - Pin Number 11: VCC → VCC/AVCC - Pin Number 26: (TXD1) → TXD1 - Pin Number 27: (RXD1) → RXD1
		15	Table 4.1 SFR Information (1) revised - 0013h: XXXXXX00b → 00h
		17	Table 4.3 SFR Information (3) revised - 00BCh: 0000X000b → 00h/0000X000b
		18	Table 4.4 SFR Information (4) revised - 00D6h: 00000XXXb → 00h - 00F5h: UART1 Function Select Register added
		19	Table 4.5 SFR Information (5) revised - 0104h: TRATR → TRA