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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MIPS32
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	256-LBGA
Supplier Device Package	256-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/79rc32h434-266bci

DMA Controller

The DMA controller consists of 6 independent DMA channels, all of which operate in exactly the same manner. The DMA controller off-loads the CPU core from moving data among the on-chip interfaces, external peripherals, and memory. The controller supports scatter/gather DMA with no alignment restrictions, making it appropriate for communications and graphics systems.

UART Interface

The RC32434 contains a serial channel (UART) that is compatible with the industry standard 16550 UART.

I²C Interface

The standard I2C interface allows the RC32434 to connect to a number of standard external peripherals for a more complete system solution. The RC32434 supports both master and slave operations.

General Purpose I/O Controller

The RC32434 has 14 general purpose input/output pins. Each pin may be used as an active high or active low level interrupt or non-maskable interrupt input, and each signal may be used as a bit input or output port.

System Integrity Functions

The RC32434 contains a programmable watchdog timer that generates a non-maskable interrupt (NMI) when the counter expires and also contains an address space monitor that reports errors in response to accesses to undecoded address regions.

Thermal Considerations

The RC32434 is guaranteed in an ambient temperature range of 0° to +70° C for commercial temperature devices and - 40° to +85° for industrial temperature devices.

Revision History

November 3, 2003: Initial publication. Preliminary Information.

December 15, 2003: Final version. In Table 7, changed maximum value for Tskew in 266MHz category and changed values for Tdo in all speed grades for signals DDRADDR, etc. In Table 8, changed minimum values in all speed grades for all Tdo signals and for Tsu and Tzd in MDATA[7:0]. In Table 16, added reference to Power Considerations document. In Table 17, added 2 rows under PCI and Notes 1 and 2.

January 5, 2004: In Table 19, Pin F6 was changed from Vcc I/O to Vss. In Table 23, pin F6 was deleted from the Vcc I/O row and added to the Vss row.

January 27, 2004: In Table 3, revised description for MADDR[3:0] and changed 4096 cycles to 4000 for MADDR[7]. (Note: MADDR was incorrectly labeled as MDATA in previous data sheet.)

March 29, 2004: Added Standby mode to Table 16, Power Consumption.

April 19, 2004: Added the I²C feature. In Table 20, pin L1 becomes SDA and pin L2 becomes SCL.

May 25, 2004: In Table 9, signals MIIRXCLK and MIITXCLK, the Min and Max values for Thigh/Tlow_9c were changed to 140 and 260 respectively and the Min and Max values for Thigh/Tlow_9d were changed to 14.0 and 26.0 respectively.

December 8, 2005: In Table 18, corrected error for Capacitance Max value from 8.0 to 10.5.

January 19, 2006: Removed all references to NVRAM.

Signal	Type	Name/Description
PCILOCKN	I/O	PCI Lock. This signal is asserted by an external bus master to indicate that an exclusive operation is occurring.
PCIPAR	I/O	PCI Parity. Even parity of the PCIAD[31:0] bus. Driven by the bus master during address and write Data phases. Driven by the bus target during the read data phase.
PCIPERRN	I/O	PCI Parity Error. If a parity error is detected, this signal is asserted by the receiving bus agent 2 clocks after the data is received.
PCIREQN[3:0]	I/O	<p>PCI Bus Request.</p> <p>In PCI host mode with internal arbiter: These signals are inputs whose assertion indicates to the internal RC32434 arbiter that an agent desires ownership of the PCI bus.</p> <p>In PCI host mode with external arbiter: PCIREQN[0]: asserted by the RC32434 to request ownership of the PCI bus. PCIREQN[3:1]: unused and driven high.</p> <p>In PCI satellite mode: PCIREQN[0]: this signal is asserted by the RC32434 to request use of the PCI bus. PCIREQN[1]: function changes to PCIIDSEL and is used as a chip select during configuration read and write transactions. PCIREQN[3:2]: unused and driven high.</p>
PCIRSTN	I/O	PCI Reset. In host mode, this signal is asserted by the RC32434 to generate a PCI reset. In satellite mode, assertion of this signal initiates a warm reset.
PCISERRN	I/O	PCI System Error. This signal is driven by an agent to indicate an address parity error, data parity error during a special cycle command, or any other system error. Requires an external pull-up.
PCISTOPN	I/O	PCI Stop. Driven by the bus target to terminate the current bus transaction. For example, to indicate a retry.
PCITRDYN	I/O	PCI Target Ready. Driven by the bus target to indicate that the current data can complete.
General Purpose Input/Output		
GPIO[0]	I/O	<p>General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0SOUT Alternate function: UART channel 0 serial output.</p>
GPIO[1]	I/O	<p>General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0SINP Alternate function: UART channel 0 serial input.</p>
GPIO[2]	I/O	<p>General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0RTSN Alternate function: UART channel 0 request to send.</p>
GPIO[3]	I/O	<p>General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0CTSN Alternate function: UART channel 0 clear to send.</p>

Table 1 Pin Description (Part 3 of 6)

Signal	Type	Name/Description
GPIO[4]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[22] Alternate function: Memory and peripheral bus address.
GPIO[5]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[23] Alternate function: Memory and peripheral bus address.
GPIO[6]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[24] Alternate function: Memory and peripheral bus address. The value of this pin may be used as a counter timer clock input (see Counter Timer Clock Select Register in Chapter 14, Counter/Timers, of the RC32434 User Manual).
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[25] Alternate function: Memory and peripheral bus address. The value of this pin may be used as a counter timer clock input (see Counter Timer Clock Select Register in Chapter 14, Counter/Timers, of the RC32434 User Manual).
GPIO[8]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: CPU Alternate function: CPU or DMA debug output pin.
GPIO[9]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIREQN[4] Alternate function: PCI Request 4.
GPIO[10]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIGNTN[4] Alternate function: PCI Grant 4.
GPIO[11]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIREQN[5] Alternate function: PCI Request 5.
GPIO[12]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIGNTN[5] Alternate function: PCI Grant 5.
GPIO[13]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIMUINTN Alternate function: PCI Messaging unit interrupt output.
SPI Interface		
SCK	I/O	Serial Clock. This signal is used as the serial clock output. This pin may be used as a bit input/output port.

Table 1 Pin Description (Part 4 of 6)

Signal	Type	Name/Description
EJTAG_TMS	I	EJTAG Mode. The value on this signal controls the test mode select of the EJTAG Controller. When using the JTAG boundary scan, this pin should be left disconnected (since there is an internal pull-up) or driven high.
JTAG_TRST_N	I	JTAG Reset. This active low signal asynchronously resets the boundary scan logic, JTAG TAP Controller, and the EJTAG Debug TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board 3) clock JTAG_TCK while holding EJTAG_TMS and/or JTAG_TMS high.
JTAG_TCK	I	JTAG Clock. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic, JTAG Controller, or the EJTAG Controller. JTAG_TCK is independent of the system and the processor clock with a nominal 50% duty cycle.
JTAG_TDO	O	JTAG Data Output. This is the serial data shifted out from the boundary scan logic, JTAG Controller, or the EJTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TDI	I	JTAG Data Input. This is the serial data input to the boundary scan logic, JTAG Controller, or the EJTAG Controller.
System		
CLK	I	Master Clock. This is the master clock input. The processor frequency is a multiple of this clock frequency. This clock is used as the system clock for all memory and peripheral bus operations.
EXTBCV	I	Load External Boot Configuration Vector. When this pin is asserted (i.e., high) the boot configuration vector is loaded from an externally supplied value during a cold reset.
EXTCLK	O	External Clock. This clock is used for all memory and peripheral bus operations.
COLDRSTN	I	Cold Reset. The assertion of this signal initiates a cold reset. This causes the processor state to be initialized, boot configuration to be loaded, and the internal PLL to lock onto the master clock (CLK).
RSTN	I/O	Reset. The assertion of this bidirectional signal initiates a warm reset. This signal is asserted by the RC32434 during a warm reset.

Table 1 Pin Description (Part 6 of 6)

Pin Characteristics

Note: Some input pads of the RC32434 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs (such as WAITACKN) which, if left floating, could adversely affect the RC32434's operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes ¹
Ethernet Interfaces	MIICL	I	LVTTL	STI	pull-down	
	MIICRS	I	LVTTL	STI	pull-down	
	MIIRXCLK	I	LVTTL	STI	pull-up	
	MIIRXD[3:0]	I	LVTTL	STI	pull-up	
	MIIRXDV	I	LVTTL	STI	pull-down	
	MIIRXER	I	LVTTL	STI	pull-down	
	MIITXCLK	I	LVTTL	STI	pull-up	
	MIITXD[3:0]	O	LVTTL	Low Drive		
	MIITXENP	O	LVTTL	Low Drive		
	MIITXER	O	LVTTL	Low Drive		
	MIIMDC	O	LVTTL	Low Drive		
	MIIMDIO	I/O	LVTTL	Low Drive	pull-up	
EJTAG / JTAG	JTAG_TMS	I	LVTTL	STI	pull-up	
	EJTAG_TMS	I	LVTTL	STI	pull-up	
	JTAG_TRST_N	I	LVTTL	STI	pull-up	
	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDO	O	LVTTL	Low Drive		
	JTAG_TDI	I	LVTTL	STI	pull-up	
System	CLK	I	LVTTL	STI		
	EXTBCV	I	LVTTL	STI	pull-down	
	EXTCLK	O	LVTTL	High Drive		
	COLDRSTN	I	LVTTL	STI		
	RSTN	I/O	LVTTL	Low Drive / STI	pull-up	pull-up on board

Table 2 Pin Characteristics (Part 2 of 2)

¹. External pull-up required in most system applications. Some applications may require additional pull-ups not identified in this table.

². Use a 2.2K pull-up resistor for I2C pins.

Boot Configuration Vector

The encoding of the boot configuration vector is described in Table 3, and the vector input is illustrated in Figure 4. The value of the boot configuration vector read in by the RC32434 during a cold reset may be determined by reading the Boot Configuration Vector (BCV) Register.

Signal	Name/Description
MADDR[3:0]	CPU Pipeline Clock Multiplier. This field specifies the value by which the PLL multiplies the master clock input (CLK) to obtain the processor clock frequency (PCLK). For master clock input frequency constraints, refer to Table 3.2 in the RC32434 User Manual. 0x0 - PLL Bypass 0x1 - Multiply by 3 0x2 - Multiply by 4 0x3 - Multiply by 5 - Reserved 0x4 - Multiply by 5 0x5 - Multiply by 6 - Reserved 0x6 - Multiply by 6 0x7 - Multiply by 8 0x8 - Multiply by 10 0x9 through 0xF - Reserved
MADDR[5:4]	External Clock Divider. This field specifies the value by which the IPBus clock (ICLK), which is always 1/2 PCLK, is divided in order to generate the external clock output on the EXTCLK pin. 0x0 - Divide by 1 0x1 - Divide by 2 0x2 - Divide by 4 0x3 - reserved
MADDR[6]	Endian. This bit specifies the endianness. 0x0 - little endian 0x1 - big endian
MADDR[7]	Reset Mode. This bit specifies the length of time the RSTN signal is driven. 0x0 - Normal reset: RSTN driven for minimum of 4000 clock cycles. If the internal boot configuration vector is selected, the expiration of an 18-bit counter operating at the master clock input (CLK) frequency is used as the PLL stabilization delay. 0x1 - Reserved
MADDR[10:8]	PCI Mode. This bit controls the operating mode of the PCI bus interface. The initial value of the EN bit in the PCIC register is determined by the PCI mode. 0x0 - Disabled (EN initial value is zero) 0x1 - PCI satellite mode with PCI target not ready (EN initial value is one) 0x2 - PCI satellite mode with suspended CPU execution (EN initial value is one) 0x3 - PCI host mode with external arbiter (EN initial value is zero) 0x4 - PCI host mode with internal arbiter using fixed priority arbitration algorithm (EN initial value is zero) 0x5 - PCI host mode with internal arbiter using round robin arbitration algorithm (EN initial value is zero) 0x6 - <i>reserved</i> 0x7 - <i>reserved</i>

Table 3 Boot Configuration Encoding (Part 1 of 2)

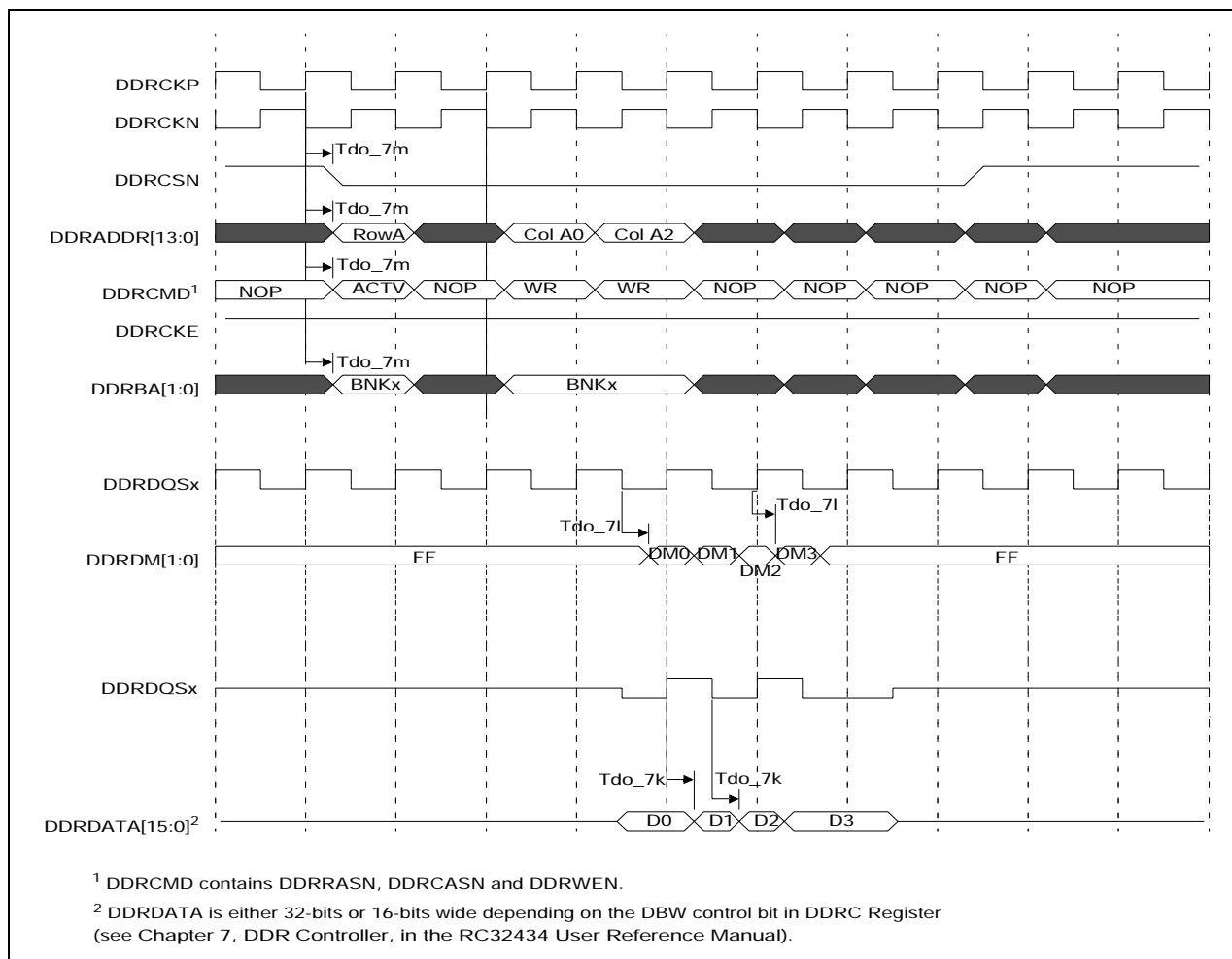


Figure 7 DDR SDRAM Timing Waveform — Write Access

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Condi-tions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Memory and Peripheral Bus ¹													See Figures 8 and 9.
MADDR[21:0]	Tdo_8a	EXTCLK rising	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns		
	Tdz_8a ²		—	—	—	—	—	—	—	—	ns		
	Tzd_8a ²		—	—	—	—	—	—	—	—	ns		
MADDR[25:22]	Tdo_8b	EXTCLK rising	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns		
	Tdz_8b ²		—	—	—	—	—	—	—	—	ns		
	Tzd_8b ²		—	—	—	—	—	—	—	—	ns		

Table 8 Memory and Peripheral Bus AC Timing Characteristics (Part 1 of 2)

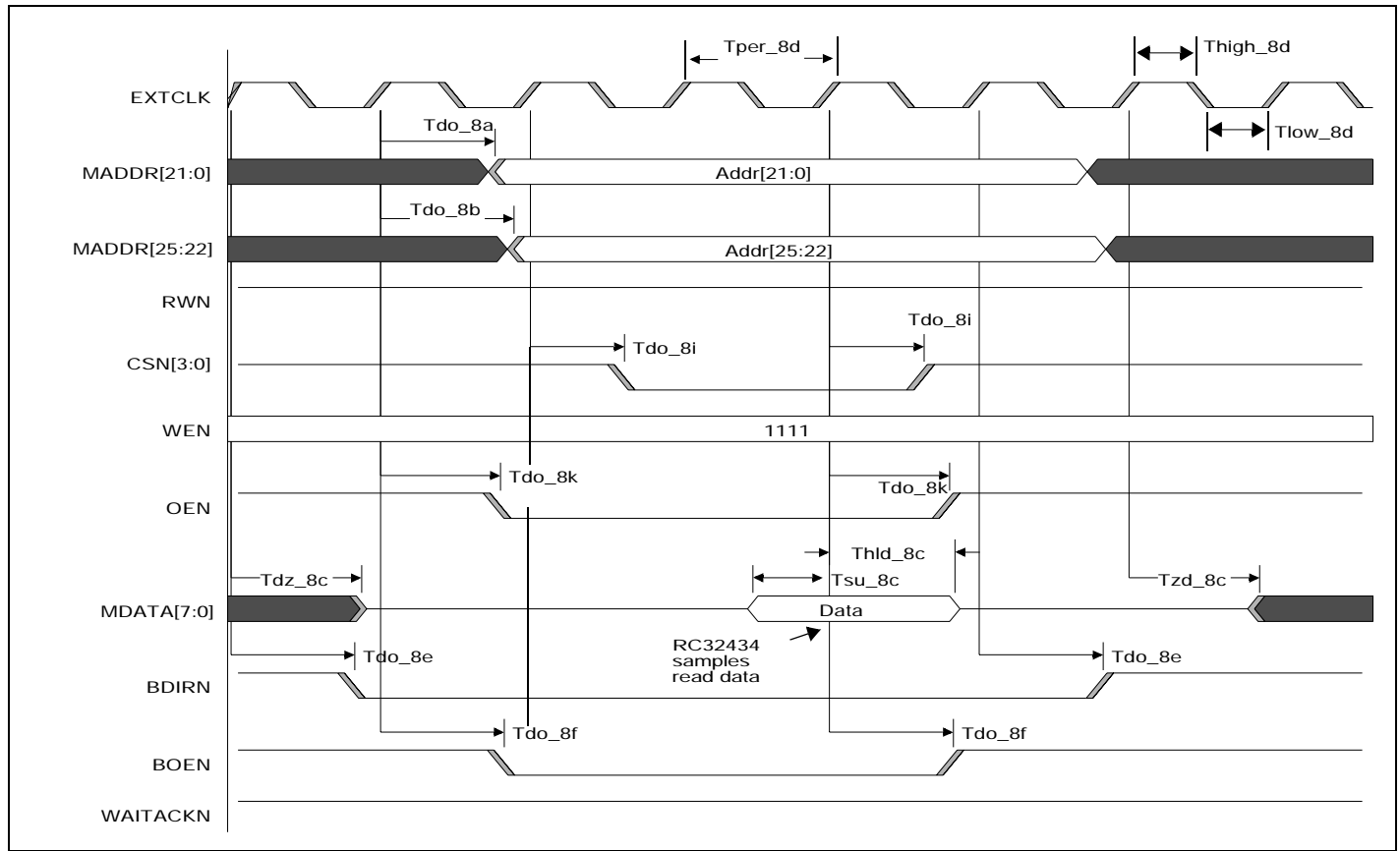


Figure 8 Memory and Peripheral Bus AC Timing Waveform — Read Access

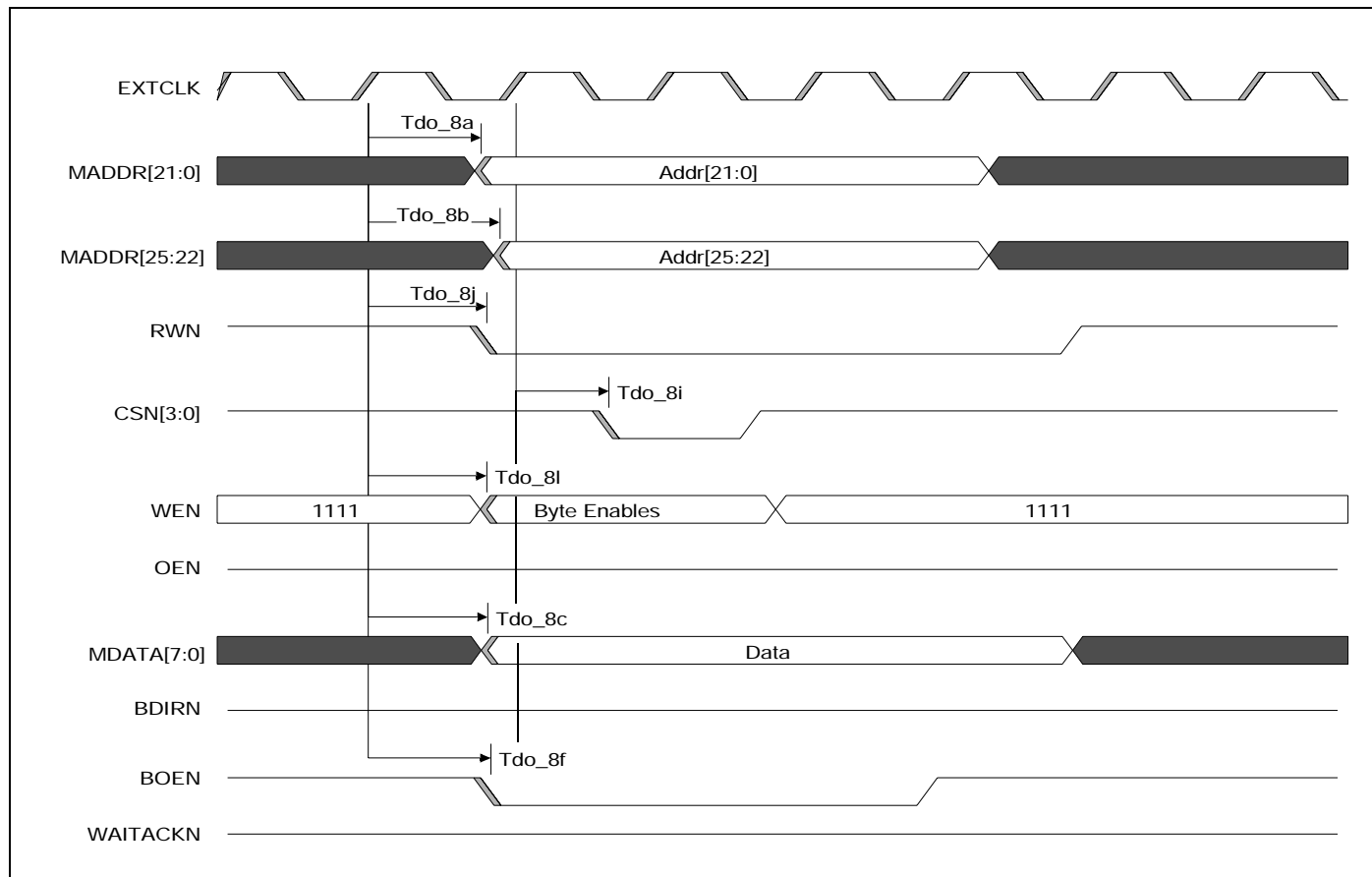


Figure 9 Memory and Peripheral Bus AC Timing Waveform — Write Access

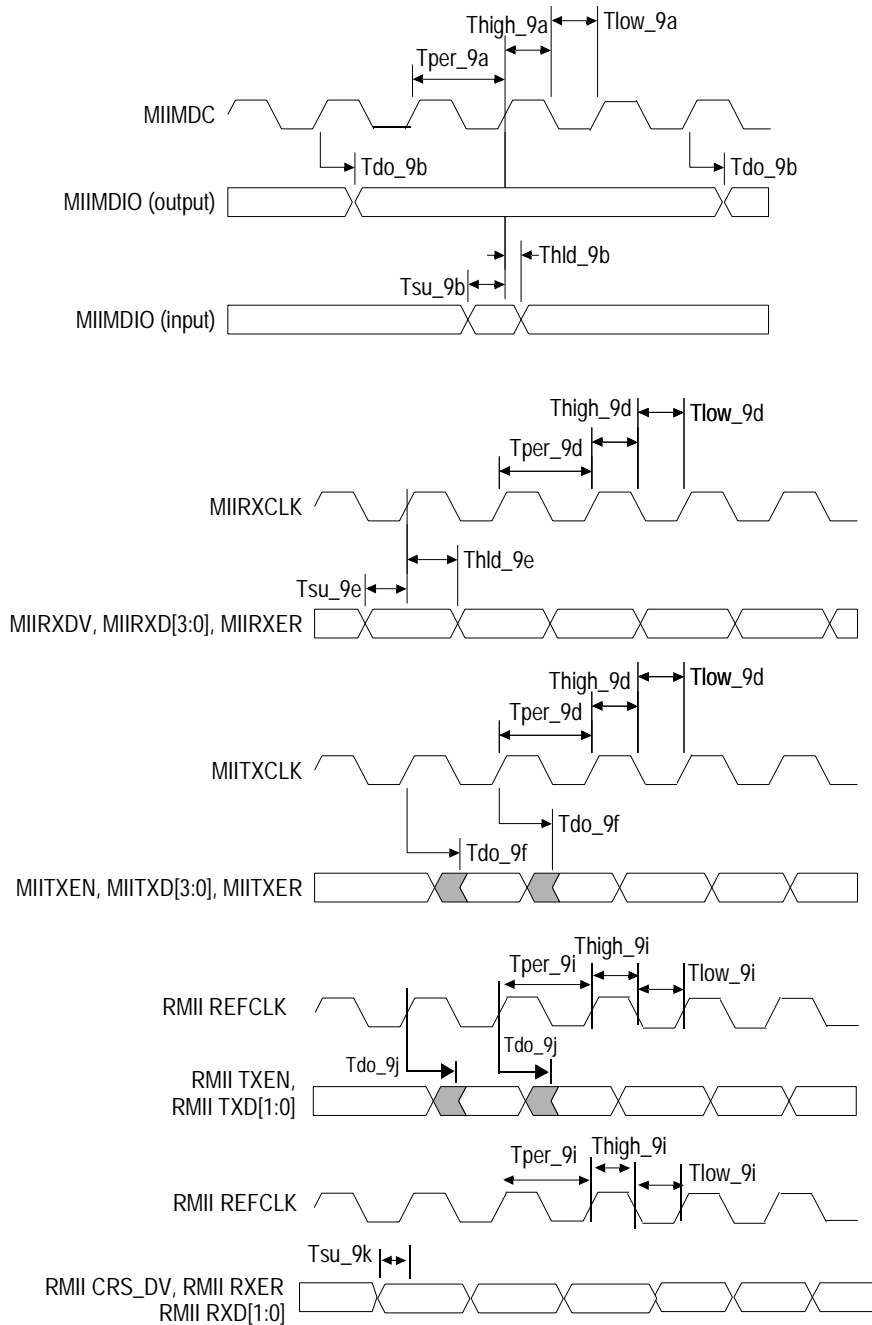


Figure 10 Ethernet AC Timing Waveform

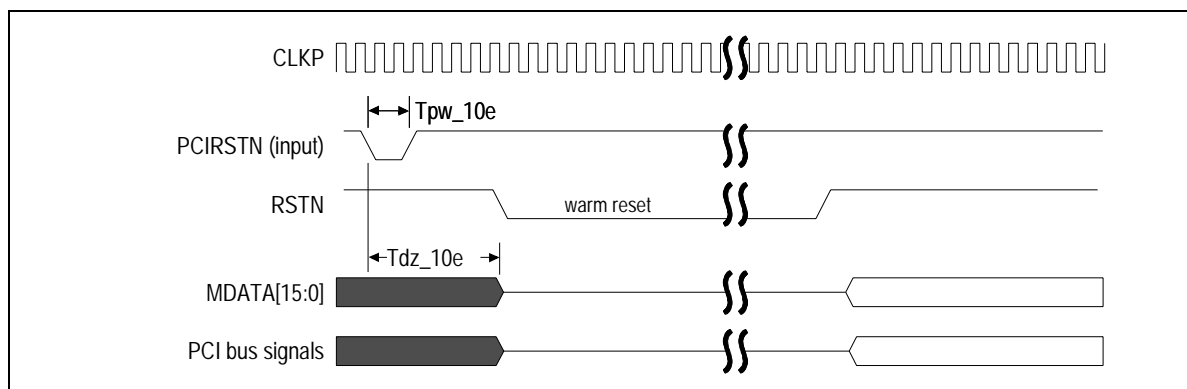


Figure 13 PCI AC Timing Waveform — PCI Reset in Satellite Mode

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference		
			Min	Max	Min	Max	Min	Max	Min	Max					
I ² C ¹															
SCL	Frequency	none	0	100	0	100	0	100	0	100	kHz	100 KHz	See Figure 14.		
	Thigh_12a, Tlow_12a		4.0	—	4.0	—	4.0	—	4.0	—	μs				
	Trise_12a		—	1000	—	1000	—	1000	—	1000	ns				
	Tfall_12a		—	300	—	300	—	300	—	300	ns				
SDA	Tsu_12b	SCL rising	250	—	250	—	250	—	250	—	ns				
	Thld_12b		0	3.45	0	3.45	0	3.45	0	3.45	μs				
	Trise_12b		—	1000	—	1000	—	1000	—	1000	ns				
	Tfall_12b		—	300	—	300	—	300	—	300	ns				
Start or repeated start condition	Tsu_12c	SDA falling	4.7	—	4.7	—	4.7	—	4.7	—	μs				
	Thld_12c		4.0	—	4.0	—	4.0	—	4.0	—	μs				
Stop condition	Tsu_12d	SDA rising	4.0	—	4.0	—	4.0	—	4.0	—	μs				
Bus free time between a stop and start condition	Tdelay_12e		4.7	—	4.7	—	4.7	—	4.7	—	μs				
SCL	Frequency	none	0	400	0	400	0	400	0	400	kHz	400 KHz			
	Thigh_12a, Tlow_12a		0.6	—	0.6	—	0.6	—	0.6	—	μs				
	Trise_12a		—	300	—	300	—	300	—	300	ns				
	Tfall_12a		—	300	—	300	—	300	—	300	ns				
SDA	Tsu_12b	SCL rising	100	—	100	—	100	—	100	—	ns				
	Thld_12b		0	0.9	0	0.9	0	0.9	0	0.9	μs				
	Trise_12b		—	300	—	300	—	300	—	300	ns				
	Tfall_12ba		—	300	—	300	—	300	—	300	ns				

Table 11 I²C AC Timing Characteristics (Part 1 of 2)

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Start or repeated start condition	Tsu_12c	SDA falling	0.6	—	0.6	—	0.6	—	0.6	—	µs	400 KHz	See Figure 14.
	Thld_12c		0.6	—	0.6	—	0.6	—	0.6	—	µs		
Stop condition	Tsu_12d	SDA rising	0.6	—	0.6	—	0.6	—	0.6	—	µs		
Bus free time between a stop and start condition	Tdelay_12e		1.3	—	1.3	—	1.3	—	1.3	—	µs		

Table 11 I²C AC Timing Characteristics (Part 2 of 2)

¹. For more information, see the I²C-Bus specification by Philips Semiconductor.

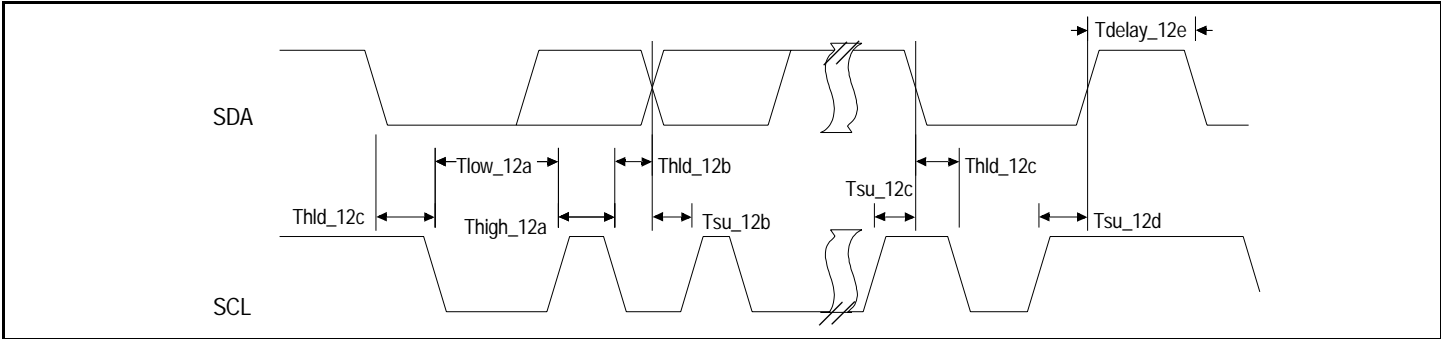


Figure 14 I2C AC Timing Waveform

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Condi-tions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
GPIO													
GPIO[13:0]	Tpw_13b ¹	None	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	ns		See Figure 15.

Table 12 GPIO AC Timing Characteristics

¹. The values for this symbol were determined by calculation, not by testing.

1

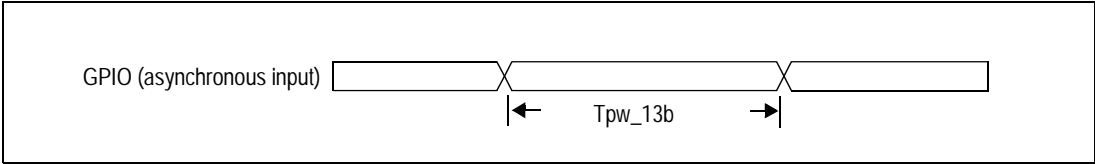


Figure 15 GPIO AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{SS}	Common ground	0	0	0	V
V_{SS}^{PLL}	PLL ground				
$V_{CC}^{I/O}$	I/O supply except for SSTL_2 ¹	3.135	3.3	3.465	V
$V_{CC}^{SI/O} (DDR)$	I/O supply for SSTL_2 ¹	2.375	2.5	2.625	V
V_{CC}^{PLL}	PLL supply (digital)	1.1	1.2	1.3	V
V_{CC}^{APLL}	PLL supply (analog)	3.135	3.3	3.465	V
V_{CC}^{Core}	Internal logic supply	1.1	1.2	1.3	V
$DDRVREF$ ²	SSTL_2 input reference voltage	$0.5(V_{CC}^{SI/O})$	$0.5(V_{CC}^{SI/O})$	$0.5(V_{CC}^{SI/O})$	V
V_{TT} ³	SSTL_2 termination voltage	$DDRVREF - 0.04$	$DDRVREF$	$DDRVREF + 0.04$	V

Table 15 RC32434 Operating Voltages

¹ SSTL_2 I/Os are used to connect to DDR SDRAM.

² Peak-to-peak AC noise on DDRVREF may not exceed $\pm 2\%$ DDRVREF (DC).

³ V_{TT} of the SSTL_2 transmitting device must track DDRVREF of the receiving device.

Recommended Operating Temperatures

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 16 RC32434 Operating Temperatures

Capacitive Load Deration

Refer to the [79RC32434 IBIS Model](#) on the IDT web site (www.idt.com).

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 15.

Note: See Table 2, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Min.	Typical	Max.	Unit	Conditions
LOW Drive Output	I_{OL}	—	14.0	—	mA	$V_{OL} = 0.4V$
	I_{OH}	—	-12.0	—	mA	$V_{OH} = 1.5V$
HIGH Drive Output	I_{OL}	—	41.0	—	mA	$V_{OL} = 0.4V$
	I_{OH}	—	-42.0	—	mA	$V_{OH} = 1.5V$
Schmitt Trigger Input (STI)	V_{IL}	-0.3	—	0.8	V	—
	V_{IH}	2.0	—	$V_{CC}/O + 0.5$	V	—
SSTL_2 (for DDR SDRAM)	I_{OL}	7.6	—	—	mA	$V_{OL} = 0.5V$
	I_{OH}	-7.6	—	—	mA	$V_{OH} = 1.76V$
	V_{IL}	-0.3	—	$0.5(V_{CC}/O) - 0.18$	V	
	V_{IH}	$0.5(V_{CC}/O) + 0.18$	—	$V_{CC}/O + 0.3$	V	
PCI	$I_{OH}(AC)$ Switching	$-12(V_{CC}/O)$	—	—	mA	$0 < V_{OUT} < 0.3(V_{CC}/O)$
		$-17.1(V_{CC}/O - V_{OUT})$	—	—	mA	$0.3(V_{CC}/O) < V_{OUT} < 0.9(V_{CC}/O)$
		—	—	$-32(V_{CC}/O)$	—	$0.7(V_{CC}/O)$
		$16(V_{CC}/O)$	—	See Note 1	mA	$0.7(V_{CC}/O) < V_{OUT} < V_{CC}/O$
	$I_{OL}(AC)$ Switching	$+16(V_{CC}/O)$	—	—	mA	$V_{CC}/O > V_{OUT} > 0.6(V_{CC}/O)$
		$+26.7(V_{OUT})$	—	—	mA	$0.6(V_{CC}/O) > V_{OUT} > 0.1(V_{CC}/O)$
		—	—	$+38(V_{CC}/O)$	mA	$V_{OUT} = 0.18(V_{CC}/O)$
		—	—	See Note 2	mA	$0.18(V_{CC}/O) > V_{OUT} > 0$
	V_{IL}	-0.3	—	$0.3(V_{CC}/O)$	V	
	V_{IH}	$0.5(V_{CC}/O)$	—	5.5	V	
Capacitance	C_{IN}	—	—	10.5	pF	—
Leakage	Inputs	—	—	± 10	μA	$V_{CC} \text{ (max)}$
	I/O_{LEAK} w/o Pull-ups/downs	—	—	± 10	μA	$V_{CC} \text{ (max)}$
	I/O_{LEAK} WITH Pull-ups/downs	—	—	± 80	μA	$V_{CC} \text{ (max)}$

Table 18 DC Electrical Characteristics

Note 1: $I_{OH}(AC) \text{ max} = (98/V_{CC}/O) * (V_{OUT} - V_{CC}/O) * (V_{OUT} + 0.4V_{CC}/O)$

Note 2: $I_{OL}(AC) \text{ max} = (256/V_{CC}/O) * V_{OUT} * (V_{CC}/O - V_{OUT})$

Absolute Maximum Ratings

Symbol	Parameter	Min ¹	Max ¹	Unit
V _{CC} I/O	I/O supply except for SSTL_2 ²	-0.6	4.0	V
V _{CC} SI/O (DDR)	I/O supply for SSTL_2 ²	-0.6	4.0	V
V _{CC} Core	Core Supply Voltage	-0.6	2.0	V
V _{CC} PLL	PLL supply (digital)	-0.6	2.0	V
V _{CC} APLL	PLL supply (analog)	-0.6	4.0	V
V _{in} I/O	I/O Input Voltage except for SSTL_2	-0.6	V _{CC} I/O + 0.5	V
V _{in} SI/O	I/O Input Voltage for SSTL_2	-0.6	V _{CC} SI/O + 0.5	V
T _a Industrial	Ambient Operating Temperature	-40	+85	°C
T _a Commercial	Ambient Operating Temperature	0	+70	°C
T _s	Storage Temperature	-40	+125	°C

Table 19 Absolute Maximum Ratings

¹. Functional and tested operating conditions are given in Table 15. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

². SSTL_2 I/Os are used to connect to DDR SDRAM.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
C2	BDIRN		G2	MIITXER		L2	SCL		R2	PCICBEN[3]	
C3	COLDRSTN		G3	MIIRXER		L3	GPIO[8]	1	R3	PCIAD[23]	
C4	WEN		G4	MIITXCLK		L4	SDI		R4	PCIAD[21]	
C5	MDATA[3]		G5	V _{cc} I/O		L5	V _{cc} I/O		R5	PCIAD[17]	
C6	MDATA[5]		G6	V _{ss}		L6	V _{ss}		R6	PCIRSTN	
C7	GPIO[6]	1	G7	V _{ss}		L7	V _{ss}		R7	PCICBEN[2]	
C8	MADDR[21]		G8	V _{ss}		L8	V _{cc} CORE		R8	PCITRDYN	
C9	MADDR[18]		G9	V _{ss}		L9	V _{ss}		R9	PCICBEN[1]	
C10	MADDR[14]		G10	V _{ss}		L10	V _{ss}		R10	PCIAD[12]	
C11	JTAG_TMS		G11	V _{ss}		L11	V _{ss}		R11	PCIAD[8]	
C12	V _{cc} APLL		G12	V _{cc} DDR		L12	V _{cc} DDR		R12	PCIAD[5]	
C13	CLK		G13	DDRDM[1]		L13	DDRADDR[9]		R13	PCIAD[3]	
C14	MADDR[4]		G14	DDRQDS[1]		L14	DDRWEN		R14	PCIAD[0]	
C15	MADDR[0]		G15	DDRDATA[10]		L15	DDRCASN		R15	PCIGNTN[2]	
C16	DDRDATA[0]		G16	DDRDATA[11]		L16	DDRADDR[8]		R16	DDRADDR[1]	
D1	MIIRXD[0]		H1	MIIMDIO		M1	GPIO[12]	1	T1	PCIAD[24]	
D2	MIICL		H2	MIIMDC		M2	PCIAD[31]		T2	GPIO[13]	1
D3	MIICRS		H3	GPIO[0]	1	M3	GPIO[11]	1	T3	PCIAD[22]	
D4	MIIRXD[1]		H4	GPIO[1]	1	M4	GPIO[9]	1	T4	PCIAD[19]	
D5	MDATA[7]		H5	V _{cc} CORE		M5	V _{cc} I/O		T5	PCIAD[16]	
D6	MDATA[2]		H6	V _{cc} CORE		M6	V _{cc} I/O		T6	PCICLK	
D7	MDATA[0]		H7	V _{ss}		M7	V _{cc} I/O		T7	PCIGNTN[0]	
D8	MADDR[20]		H8	V _{ss}		M8	V _{cc} CORE		T8	PCIDEVSELN	
D9	MADDR[19]		H9	V _{ss}		M9	V _{cc} CORE		T9	PCIPAR	
D10	MADDR[15]		H10	V _{ss}		M10	V _{cc} I/O		T10	PCIAD[13]	
D11	EXTBCV		H11	V _{ss}		M11	V _{cc} DDR		T11	PCIAD[9]	
D12	JTAG_TRSTN		H12	V _{cc} CORE		M12	V _{cc} DDR		T12	PCIAD[6]	
D13	WAITACKN		H13	DDRDATA[15]		M13	DDRRASN		T13	PCIAD[2]	
D14	DDRDATA[2]		H14	DDRDATA[14]		M14	DDRBA[1]		T14	PCIAD[1]	
D15	DDRDATA[3]		H15	DDRDATA[12]		M15	DDRADDR[6]		T15	PCIGNTN[1]	
D16	DDRDATA[1]		H16	DDRDATA[13]		M16	DDRADDR[7]		T16	PCIGNTN[3]	

Table 20 RC32434 Pinout (Part 2 of 2)

RC32434 Ground Pins

V _{SS}	V _{SS}	V _{SS} PLL
F6	J6	A11, B12
F7	J7	
F8	J8	
F10	J9	
F11	J10	
G6	K7	
G7	K8	
G8	K9	
G9	K10	
G10	K11	
G11	L6	
H7	L7	
H8	L9	
H9	L10	
H10	L11	
H11		

Table 23 RC32434 Ground Pins

RC32434 Signals Listed Alphabetically

The following table lists the RC32434 pins in alphabetical order.

Signal Name	I/O Type	Location	Signal Category
BDIRN	O	C2	Memory and Peripheral Bus
BOEN	O	B1	
CLK	I	C13	System
COLDRSTN	I	C3	
CSN[0]	O	A4	Memory and Peripheral Bus
CSN[1]	O	B4	
CSN[2]	O	A3	
CSN[3]	O	B3	

Table 24 RC32434 Alphabetical Signal List (Part 1 of 7)

Signal Name	I/O Type	Location	Signal Category
DDRADDR[0]	O	P14	DDR Bus
DDRADDR[1]	O	R16	
DDRADDR[2]	O	P15	
DDRADDR[3]	O	N15	
DDRADDR[4]	O	N14	
DDRADDR[5]	O	N13	
DDRADDR[6]	O	M15	
DDRADDR[7]	O	M16	
DDRADDR[8]	O	L16	
DDRADDR[9]	O	L13	
DDRADDR[10]	O	K15	
DDRADDR[11]	O	K14	
DDRADDR[12]	O	K16	
DDRADDR[13]	O	E15	
DDRBA[0]	O	N16	
DDRBA[1]	O	M14	
DDRCASN	O	L15	
DDRCKE	O	K13	
DDRCKN	O	J13	
DDRCKP	O	J15	
DDRCSN	O	P16	
DDRDATA[0]	I/O	C16	
DDRDATA[1]	I/O	D16	
DDRDATA[2]	I/O	D14	
DDRDATA[3]	I/O	D15	
DDRDATA[4]	I/O	E16	
DDRDATA[5]	I/O	E14	
DDRDATA[6]	I/O	E13	
DDRDATA[7]	I/O	F16	
DDRDATA[8]	I/O	F14	
DDRDATA[9]	I/O	F13	
DDRDATA[10]	I/O	G15	
DDRDATA[11]	I/O	G16	
DDRDATA[12]	I/O	H15	
DDRDATA[13]	I/O	H16	
DDRDATA[14]	I/O	H14	

Table 24 RC32434 Alphabetical Signal List (Part 2 of 7)

Signal Name	I/O Type	Location	Signal Category
PCISTOPN	I/O	P8	PCI Bus Interface
PCITRDYN	I/O	R8	
RSTN	I/O	B2	System
RWN	O	A1	Memory and Peripheral Bus
SCK	I/O	K2	Serial Peripheral Interface
SCL	I/O	L2	I ² C
SDA	I/O	L1	
SDI	I/O	L4	Serial Peripheral Interface
SDO	I/O	K4	
Vcc APLL		C12	Power
Vcc Core		E8, E9, F9, H5, H6, H12, J5, J11, J12, L8, M8, M9	
Vcc DDR		E11, E12, F12, G12, K12, L12, M11, M12	
Vcc I/O		E5, E6, E7, E10, F5, G5, K5, K6, L5, M5, M6, M7, M10	
Vcc PLL		B11	
Vss		F6, F7, F8, F10, F11, G6, G7, G8, G9, G10, G11, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, K7, K8, K9, K10, K11, L6, L7, L9, L10, L11	Ground
Vss APLL		B12	
Vss PLL		A11	
WAITACKN	I	D13	Memory and Peripheral Bus
WEN	O	C4	
Reserved		K3, L1, L2	

Table 24 RC32434 Alphabetical Signal List (Part 7 of 7)

RC32434 Package Drawing — 256-pin CABGA

