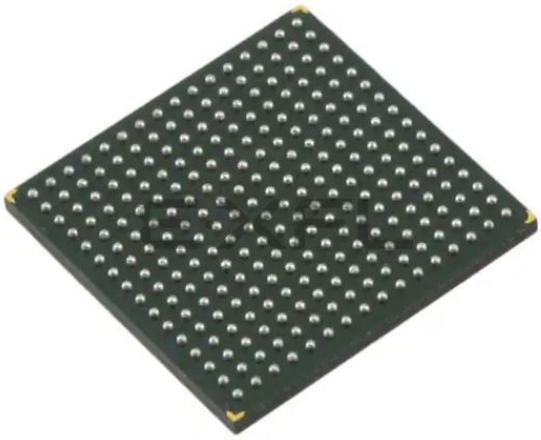
Renesas Electronics America Inc - 79RC32H434-300BCGI Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS32
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	300MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	256-LBGA
Supplier Device Package	256-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/79rc32h434-300bcgi

- **Memory and Peripheral Device Controller**
  - *Provides "glueless" interface to standard SRAM, Flash, ROM, dual-port memory, and peripheral devices*
  - *Demultiplexed address and data buses: 8-bit data bus, 26-bit address bus, 4 chip selects, control for external data bus buffers*

    Automatic byte gathering and scattering
  - *Flexible protocol configuration parameters: programmable number of wait states (0 to 63), programmable postread/post-write delay (0 to 31), supports external wait state generation, supports Intel and Motorola style peripherals*
  - *Write protect capability per chip select*
  - *Programmable bus transaction timer generates warm reset when counter expires*
  - *Supports up to 64 MB of memory per chip select*
- **DMA Controller**
  - *6 DMA channels: two channels for PCI (PCI to Memory and Memory to PCI), two channels for the Ethernet interface, and two channels for memory to memory DMA operations*
  - *Provides flexible descriptor based operation*
  - *Supports unaligned transfers (i.e., source or destination address may be on any byte boundary) with arbitrary byte length*
- **Universal Asynchronous Receiver Transmitter (UART)**
  - *Compatible with the 16550 and 16450 UARTs*
  - *16-byte transmit and receive buffers*
  - *Programmable baud rate generator derived from the system clock*
  - *Fully programmable serial characteristics:*
    - *5, 6, 7, or 8 bit characters*
    - *Even, odd or no parity bit generation and detection*
    - *1, 1-1/2 or 2 stop bit generation*
  - *Line break generation and detection*
  - *False start bit detection*
  - *Internal loopback mode*
- **I^2C-Bus**
  - *Supports standard 100 Kbps mode as well as 400 Kbps fast mode*
  - *Supports 7-bit and 10-bit addressing*
  - *Supports four modes: master transmitter, master receiver, slave transmitter, slave receiver*
- **Additional General Purpose Peripherals**
  - *Interrupt controller*
  - *System integrity functions*
  - *General purpose I/O controller*
  - *Serial peripheral interface (SPI)*
- **Counter/Timers**
  - *Three general purpose 32-bit counter timers*
  - *Timers may be cascaded*
  - *Selectable counter/timer clock source*
- **JTAG Interface**
  - *Compatible with IEEE Std. 1149.1 - 1990*

CPU Execution Core

The 32-bit CPU core is 100% compatible with the MIPS32 instruction set architecture (ISA). Specifically, this device features the 4Kc CPU core developed by MIPS Technologies Inc. (www.mips.com). This core issues a single instruction per cycle, includes a five stage pipeline and is optimized for applications that require integer arithmetic.

The CPU core includes 8 KB instruction and 8 KB data caches. Both caches are 4-way set associative and can be locked on a per line basis, which allows the programmer control over this precious on-chip memory resource. The core also features a memory management unit (MMU). The CPU core also incorporates an enhanced joint test access group (EJTAG) interface that is used to interface to in-circuit emulator tools, providing access to internal registers and enabling the part to be controlled externally, simplifying the system debug process.

The use of this core allows IDT's customers to leverage the broad range of software and development tools available for the MIPS architecture, including operating systems, compilers, and in-circuit emulators.

PCI Interface

The PCI interface on the RC32434 is compatible with version 2.2 of the PCI specification. An on-chip arbiter supports up to six external bus masters, supporting both fixed priority and rotating priority arbitration schemes. The part can support both satellite and host PCI configurations, enabling the RC32434 to act as a slave controller for a PCI add-in card application or as the primary PCI controller in the system. The PCI interface can be operated synchronously or asynchronously to the other I/O interfaces on the RC32434 device.

Ethernet Interface

The RC32434 has one Ethernet Channel supporting 10Mbps and 100Mbps speeds to provide a standard media independent interface (MII or RMII), allowing a wide range of external devices to be connected efficiently.

Double Data Rate Memory Controller

The RC32434 incorporates a high performance double data rate (DDR) memory controller which supports x16 memory configurations up to 256MB. This module provides all of the signals required to interface to discrete memory devices, including a chip select, differential clocking outputs and data strobes.

Memory and I/O Controller

The RC32434 uses a dedicated local memory/IO controller including a de-multiplexed 8-bit data and 26-bit address bus. It includes all of the signals required to interface directly to a maximum of four Intel or Motorola-style external peripherals.

Pin Description Table

The following table lists the functions of the pins provided on the RC32434. Some of the functions listed may be multiplexed onto the same pin.

The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
Memory and Peripheral Bus		
BDIRN	O	**External Buffer Direction.** Controls the direction of the external data bus buffer for the memory and peripheral bus. If the RC32434 memory and peripheral bus is connected to the A side of a transceiver, such as an IDT74FCT245, then this pin may be directly connected to the direction control (e.g., BDIR) pin of the transceiver.
BOEN	O	**External Buffer Enable.** This signal provides an output enable control for an external buffer on the memory and peripheral data bus.
WEN	O	**Write Enables.** This signal is the memory and peripheral bus write enable signal.
CSN[3:0]	O	**Chip Selects.** These signals are used to select an external device on the memory and peripheral bus.
MADDR[21:0]	O	**Address Bus.** 22-bit memory and peripheral bus address bus. MADDR[25:22] are available as GPIO alternate functions.
MDATA[7:0]	I/O	**Data Bus.** 8-bit memory and peripheral data bus. During a cold reset, these pins function as inputs that are used to load the boot configuration vector.
OEN	O	**Output Enable.** This signal is asserted when data should be driven by an external device on the memory and peripheral bus.
RWN	O	**Read Write.** This signal indicates whether the transaction on the memory and peripheral bus is a read transaction or a write transaction. A high level indicates a read from an external device. A low level indicates a write to an external device.
WAITACKN	I	**Wait or Transfer Acknowledge.** When configured as wait, this signal is asserted during a memory and peripheral bus transaction to extend the bus cycle. When configured as a transfer acknowledge, this signal is asserted during a transaction to signal the completion of the transaction.
DDR Bus		
DDRADDR[13:0]	O	**DDR Address Bus.** 14-bit multiplexed DDR address bus. This bus is used to transfer the addresses to the DDR devices.
DDRBA[1:0]	O	**DDR Bank Address.** These signals are used to transfer the bank address to the DDRs.
DDRCASN	O	**DDR Column Address Strobe.** This signal is asserted during DDR transactions.
DDRCKE	O	**DDR Clock Enable.** The DDR clock enable signal is asserted during normal DDR operation. This signal is negated following a cold reset or during a power down operation.
DDRCKN	O	**DDR Negative DDR clock.** This signal is the negative clock of the differential DDR clock pair.

Table 1 Pin Description (Part 1 of 6)

Signal	Type	Name/Description
DDRCKP	O	**DDR Positive DDR clock.** This signal is the positive clock of the differential DDR clock pair.
DDRCSN	O	**DDR Chip Selects.** This active low signal is used to select DDR device(s) on the DDR bus.
DDRDATA[15:0]	I/O	**DDR Data Bus.** 16-bit DDR data bus is used to transfer data between the RC32434 and the DDR devices. Data is transferred on both edges of the clock.
DDRDM[1:0]	O	**DDR Data Write Enables.** Byte data write enables are used to enable specific byte lanes during DDR writes. DDRDM[0] corresponds to DDRDATA[7:0] DDRDM[1] corresponds to DDRDATA[15:8]
DDRDQS[1:0]	I/O	**DDR Data Strobes.** DDR byte data strobes are used to clock data between DDR devices and the RC32434. These strobes are inputs during DDR reads and outputs during DDR writes. DDRDQS[0] corresponds to DDRDATA[7:0] DDRDQS[1] corresponds to DDRDATA[15:8]
DDRRASN	O	**DDR Row Address Strobe.** The DDR row address strobe is asserted during DDR transactions.
DDRVREF	I	**DDR Voltage Reference.** SSTL_2 DDR voltage reference is generated by an external source.
DDRWEN	O	**DDR Write Enable.** DDR write enable is asserted during DDR write transactions.
PCI Bus		
PCIAD[31:0]	I/O	**PCI Multiplexed Address/Data Bus**. Address is driven by a bus master during initial PCIFRAMEN assertion. Data is then driven by the bus master during writes or by the bus target during reads.
PCICBEN[3:0]	I/O	**PCI Multiplexed Command/Byte Enable Bus**. PCI commands are driven by the bus master during the initial PCIFRAMEN assertion. Byte enable signals are driven by the bus master during subsequent data phase(s).
PCICLK	I	**PCI Clock**. Clock used for all PCI bus transactions.
PCIDEVSELN	I/O	**PCI Device Select**. This signal is driven by a bus target to indicate that the target has decoded the address as one of its own address spaces.
PCIFRAMEN	I/O	**PCI Frame**. Driven by a bus master. Assertion indicates the beginning of a bus transaction. Negation indicates the last data.
PCIGNTN[3:0]	I/O	**PCI Bus Grant**. **In PCI host mode with internal arbiter:** The assertion of these signals indicates to the agent that the internal RC32434 arbiter has granted the agent access to the PCI bus. **In PCI host mode with external arbiter:** PCIGNTN[0]: asserted by an external arbiter to indicate to the RC32434 that access to the PCI bus has been granted. PCIGNTN[3:1]: unused and driven high. **In PCI satellite mode:** PCIGNTN[0]: This signal is asserted by an external arbiter to indicate to the RC32434 that access to the PCI bus has been granted. PCIGNTN[3:1]: unused and driven high.
PCIIRDYN	I/O	**PCI Initiator Ready**. Driven by the bus master to indicate that the current datum can complete.

Table 1 Pin Description (Part 2 of 6)

Signal	Type	Name/Description
GPIO[4]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[22] Alternate function: Memory and peripheral bus address.
GPIO[5]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[23] Alternate function: Memory and peripheral bus address.
GPIO[6]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[24] Alternate function: Memory and peripheral bus address. The value of this pin may be used as a counter timer clock input (see Counter Timer Clock Select Register in Chapter 14, Counter/Timers, of the RC32434 User Manual).
GPIO[7]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[25] Alternate function: Memory and peripheral bus address. The value of this pin may be used as a counter timer clock input (see Counter Timer Clock Select Register in Chapter 14, Counter/Timers, of the RC32434 User Manual).
GPIO[8]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: CPU Alternate function: CPU or DMA debug output pin.
GPIO[9]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIREQN[4] Alternate function: PCI Request 4.
GPIO[10]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIGNTN[4] Alternate function: PCI Grant 4.
GPIO[11]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIREQN[5] Alternate function: PCI Request 5.
GPIO[12]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIGNTN[5] Alternate function: PCI Grant 5.
GPIO[13]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIMUINTN Alternate function: PCI Messaging unit interrupt output.
SPI Interface		
SCK	I/O	**Serial Clock**. This signal is used as the serial clock output. This pin may be used as a bit input/output port.

Table 1 Pin Description (Part 4 of 6)

Signal	Type	Name/Description
SDI	I/O	**Serial Data Input**. This signal is used to shift in serial data. This pin may be used as a bit input/output port.
SDO	I/O	**Serial Data Output**. This signal is used shift out serial data.
I^2C Bus Interface		
SCL	I/O	**I^2C Clock.** I^2C-bus clock.
SDA	I/O	**I^2C Data Bus.** I^2C-bus data bus.
Ethernet Interfaces		
MIICL	I	**Ethernet MII Collision Detected.** This signal is asserted by the ethernet PHY when a collision is detected.
MIICRS	I	**Ethernet MII Carrier Sense.** This signal is asserted by the ethernet PHY when either the transmit or receive medium is not idle.
MIIRXCLK	I	**Ethernet MII Receive Clock.** This clock is a continuous clock that provides a timing reference for the reception of data. This pin also functions as the RMII REF_CLK input.
MIIRXD[3:0]	I	**Ethernet MII Receive Data.** This nibble wide data bus contains the data received by the ethernet PHY. This pin also functions as the RMII RXD[1:0] input.
MIIRXDV	I	**Ethernet MII Receive Data Valid.** The assertion of this signal indicates that valid receive data is in the MII receive data bus. This pin also functions as the RMII CRS_DV input.
MIIRXER	I	**Ethernet MII Receive Error.** The assertion of this signal indicates that an error was detected somewhere in the ethernet frame currently being sent in the MII receive data bus. This pin also functions as the RMII RX_ER input.
MIITXCLK	I	**Ethernet MII Transmit Clock.** This clock is a continuous clock that provides a timing reference for the transfer of transmit data.
MIITXD[3:0]	O	**Ethernet MII Transmit Data.** This nibble wide data bus contains the data to be transmitted. This pin also functions as the RMII TXD[1:0] output.
MIITXENP	O	**Ethernet MII Transmit Enable.** The assertion of this signal indicates that data is present on the MII for transmission. This pin also functions as the RMII TX_EN output.
MIITXER	O	**Ethernet MII Transmit Coding Error.** When this signal is asserted together with MIITXENP, the ethernet PHY will transmit symbols which are not valid data or delimiters.
MIIMDC	O	**MII Management Data Clock.** This signal is used as a timing reference for transmission of data on the management interface.
MIIMDIO	I/O	**MII Management Data.** This bidirectional signal is used to transfer data between the station management entity and the ethernet PHY.
EJTAG / JTAG		
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller. When using the EJTAG debug interface, this pin should be left disconnected (since there is an internal pull-up) or driven high.

Table 1 Pin Description (Part 5 of 6)

Signal	Type	Name/Description
EJTAG_TMS	I	**EJTAG Mode**. The value on this signal controls the test mode select of the EJTAG Controller. When using the JTAG boundary scan, this pin should be left disconnected (since there is an internal pull-up) or driven high.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic, JTAG TAP Controller, and the EJTAG Debug TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board 3) clock JTAG_TCK while holding EJTAG_TMS and/or JTAG_TMS high.
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic, JTAG Controller, or the EJTAG Controller. JTAG_TCK is independent of the system and the processor clock with a nominal 50% duty cycle.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic, JTAG Controller, or the EJTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic, JTAG Controller, or the EJTAG Controller.
System		
CLK	I	**Master Clock.** This is the master clock input. The processor frequency is a multiple of this clock frequency. This clock is used as the system clock for all memory and peripheral bus operations.
EXTBCV	I	**Load External Boot Configuration Vector.** When this pin is asserted (i.e., high) the boot configuration vector is loaded from an externally supplied value during a cold reset.
EXTCLK	O	**External Clock.** This clock is used for all memory and peripheral bus operations.
COLDRSTN	I	**Cold Reset.** The assertion of this signal initiates a cold reset. This causes the processor state to be initialized, boot configuration to be loaded, and the internal PLL to lock onto the master clock (CLK).
RSTN	I/O	**Reset.** The assertion of this bidirectional signal initiates a warm reset. This signal is asserted by the RC32434 during a warm reset.

Table 1 Pin Description (Part 6 of 6)

Pin Characteristics

Note: Some input pads of the RC32434 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs (such as WAITACKN) which, if left floating, could adversely affect the RC32434's operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes[1]
Memory and Peripheral Bus	BDIRN	O	LVTTL	High Drive		
	BOEN	O	LVTTL	High Drive		
	WEN	O	LVTTL	High Drive		
	CSN[3:0]	O	LVTTL	High Drive		
	MADDR[21:0]	I/O	LVTTL	High Drive		
	MDATA[7:0]	I/O	LVTTL	High Drive		
	OEN	O	LVTTL	High Drive		
	RWN	O	LVTTL	High Drive		
	WAITACKN	I	LVTTL	STI	pull-up	
DDR Bus	DDRADDR[13:0]	O	SSTL_2			
	DDRBA[1:0]	O	SSTL_2			
	DDRCASN	O	SSTL_2			
	DDRCKE	O	SSTL_2 / LVC-MOS			
	DDRCKN	O	SSTL_2			
	DDRCKP	O	SSTL_2			
	DDRCSN	O	SSTL_2			
	DDRDATA[15:0]	I/O	SSTL_2			
	DDRDM[1:0]	O	SSTL_2			
	DDRDQS[1:0]	I/O	SSTL_2			
	DDRRASN	O	SSTL_2			
	DDRVREF	I	Analog			
	DDRWEN	O	SSTL_2			
PCI Bus Interface	PCIAD[31:0]	I/O	PCI			
	PCICBEN[3:0]	I/O	PCI			
	PCICLK	I	PCI			
	PCIDEVSELN	I/O	PCI			pull-up on board
	PCIFRAMEN	I/O	PCI			pull-up on board
	PCIGNTN[3:0]	I/O	PCI			pull-up on board
	PCIIRDYN	I/O	PCI			pull-up on board
	PCILOCKN	I/O	PCI			
	PCIPAR	I/O	PCI			
	PCIPERRN	I/O	PCI			
	PCIREQN[3:0]	I/O	PCI			pull-up on board
	PCIRSTN	I/O	PCI			pull-down on board
	PCISERRN	I/O	PCI	Open Collector		pull-up on board
	PCISTOPN	I/O	PCI			pull-up on board
	PCITRDYN	I/O	PCI			pull-up on board
General Purpose I/O	GPIO[8:0]	I/O	LVTTL	High Drive	pull-up	
	GPIO[13:9]	I/O	PCI			pull-up on board
Serial Peripheral Interface	SCK	I/O	LVTTL	High Drive	pull-up	pull-up on board
	SDI	I/O	LVTTL	High Drive	pull-up	pull-up on board
	SDO	I/O	LVTTL	High Drive	pull-up	pull-up on board
I^2C-Bus Interface	SCL	I/O	LVTTL	Low Drive/STI		pull-up on board[2]
	SDA	I/O	LVTTL	Low Drive/STI		pull-up on board[2]

Table 2 Pin Characteristics (Part 1 of 2)

Boot Configuration Vector

The encoding of the boot configuration vector is described in Table 3, and the vector input is illustrated in Figure 4. The value of the boot configuration vector read in by the RC32434 during a cold reset may be determined by reading the Boot Configuration Vector (BCV) Register.

Signal	Name/Description
MADDR[3:0]	**CPU Pipeline Clock Multiplier**. This field specifies the value by which the PLL multiplies the master clock input (CLK) to obtain the processor clock frequency (PCLK). For master clock input frequency constraints, refer to Table 3.2 in the RC32434 User Manual. 0x0 - PLL Bypass 0x1 - Multiply by 3 0x2 - Multiply by 4 0x3 - Multiply by 5 - Reserved 0x4 - Multiply by 5 0x5 - Multiply by 6 - Reserved 0x6 - Multiply by 6 0x7 - Multiply by 8 0x8 - Multiply by 10 0x9 through 0xF - Reserved
MADDR[5:4]	**External Clock Divider**. This field specifies the value by which the IPBus clock (ICLK), which is always 1/2 PCLK, is divided in order to generate the external clock output on the EXTCLK pin. 0x0 - Divide by 1 0x1 - Divide by 2 0x2 - Divide by 4 0x3 - reserved
MADDR[6]	**Endian.** This bit specifies the endianness. 0x0 - little endian 0x1 - big endian
MADDR[7]	**Reset Mode**. This bit specifies the length of time the RSTN signal is driven. 0x0 - Normal reset: RSTN driven for minimum of 4000 clock cycles. If the internal boot configuration vector is selected, the expiration of an 18-bit counter operating at the master clock input (CLK) frequency is used as the PLL stabilization delay. 0x1 - Reserved
MADDR[10:8]	**PCI Mode**. This bit controls the operating mode of the PCI bus interface. The initial value of the EN bit in the PCIC register is determined by the PCI mode. 0x0 - Disabled (EN initial value is zero) 0x1 - PCI satellite mode with PCI target not ready (EN initial value is one) 0x2 - PCI satellite mode with suspended CPU execution (EN initial value is one) 0x3 - PCI host mode with external arbiter (EN initial value is zero) 0x4 - PCI host mode with internal arbiter using fixed priority arbitration algorithm (EN initial value is zero) 0x5 - PCI host mode with internal arbiter using round robin arbitration algorithm (EN initial value is zero) 0x6 - *reserved* 0x7 - *reserved*

Table 3 Boot Configuration Encoding (Part 1 of 2)

Signal	Name/Description
MADDR[11]	**Disable Watchdog Timer**. When this bit is set, the watchdog timer is disabled following a cold reset. 0x0 - Watchdog timer enabled 0x1 - Watchdog timer disabled
MADDR[13:12]	**Reserved**. These pins must be driven low during boot configuration.
MADDR[15:14]	**Reserved**. Must be set to zero.

Table 3 Boot Configuration Encoding (Part 2 of 2)

Logic Diagram — RC32434

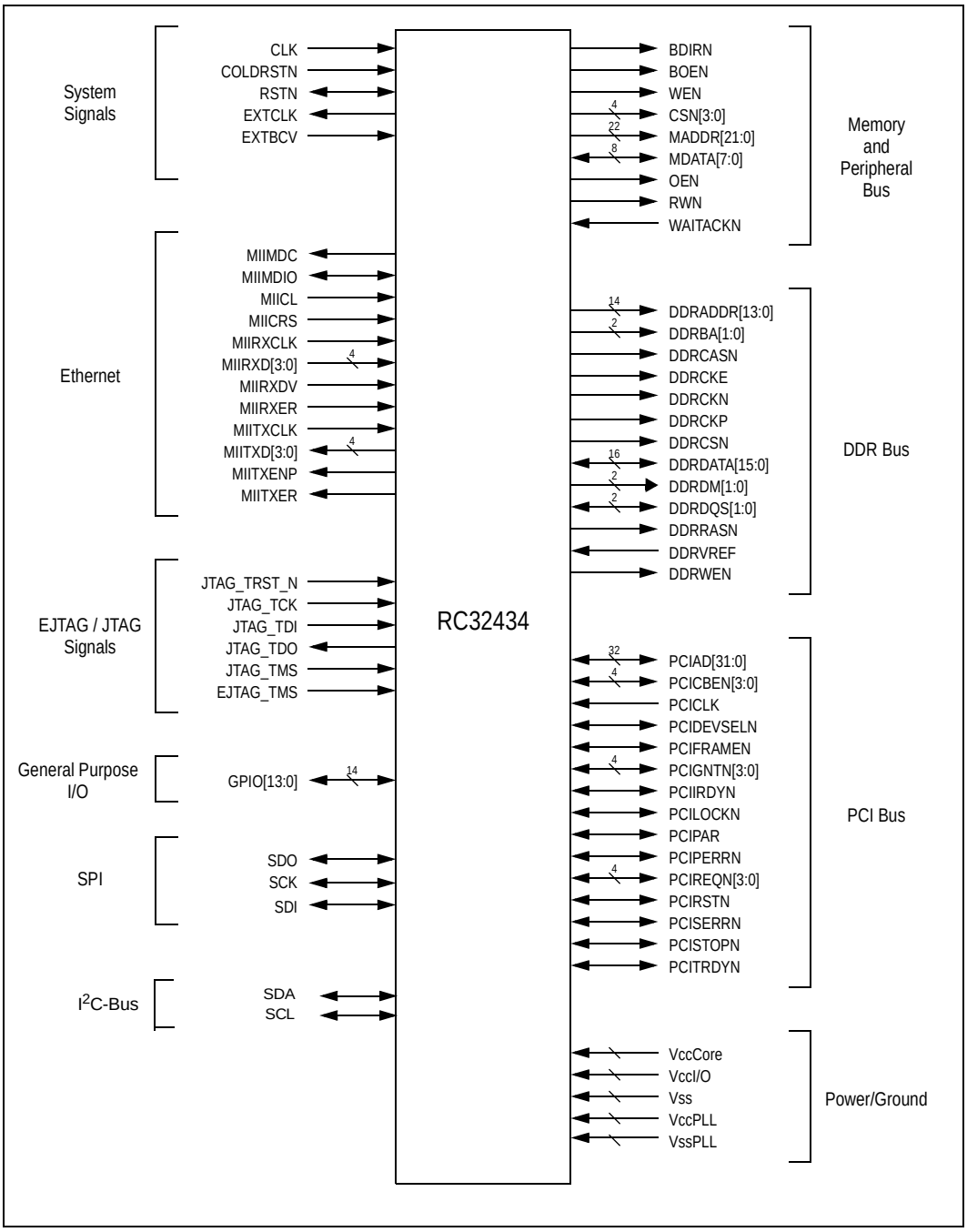


Figure 1 Logic Diagram

AC Timing Characteristics

(Values given below are based on systems running at recommended operating temperatures and supply voltages, shown in Tables 15 and 16.)

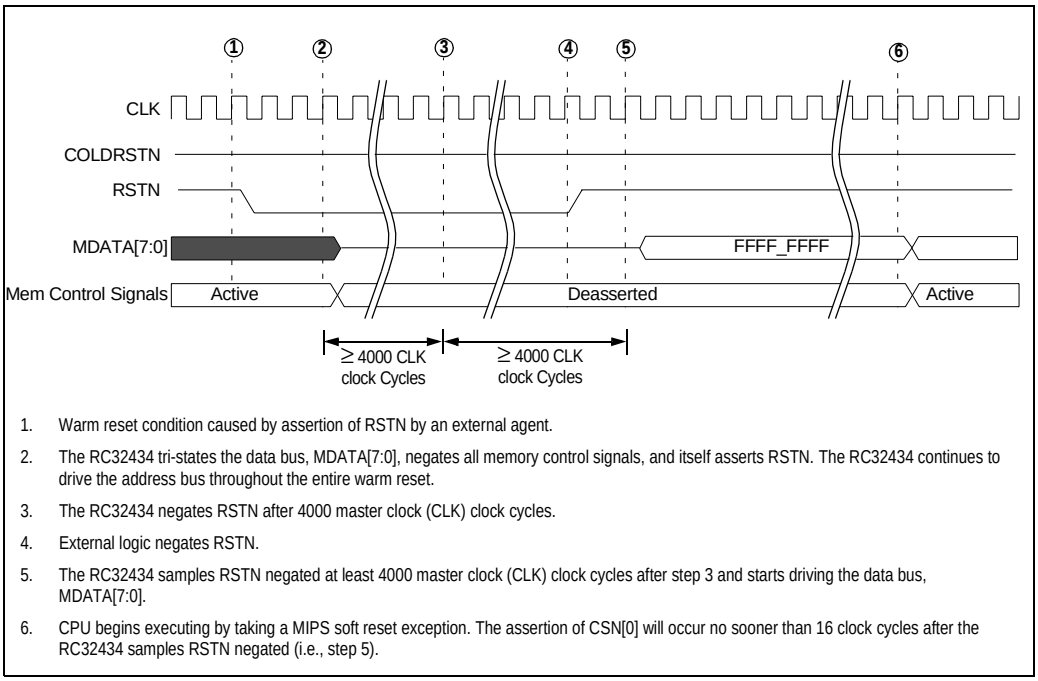
Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Reset													
COLDRSTN[1]	Tpw_6a[2]	none	OSC	—	OSC	—	OSC	—	OSC	—	ms	Cold reset	See Figures 4 and 5.
	Trise_6a	none	—	5.0	—	5.0	—	5.0	—	5.0	ns	Cold reset	
RSTN[3] (input)	Tpw_6b[2]	none	2(CLK)	—	2(CLK)	—	2(CLK)	—	2(CLK)	—	ns	Warm reset	
RSTN[3] (output)	Tdo_6c	COLDRSTN falling	—	15.0	—	15.0	—	15.0	—	15.0	ns	Cold reset	
MADDR[15:0] (boot vector)	Tdz_6d[2]	COLDRSTN falling	—	30.0	—	30.0	—	30.0	—	30.0	ns	Cold reset	
	Tdz_6d[2]	RSTN falling	—	5(CLK)	—	5(CLK)	—	5(CLK)	—	5(CLK)	ns	Warm reset	
	Tzd_6d[2]	RSTN rising	2(CLK)	—	2(CLK)	—	2(CLK)	—	2(CLK)	—	ns	Warm reset	

Table 6 Reset and System AC Timing Characteristics

1. The COLDRSTN minimum pulse width is the oscillator stabilization time (OSC) with V_{cc} stable.

2. The values for this symbol were determined by calculation, not by testing.

3. RSTN is a bidirectional signal. It is treated as an asynchronous input.



1. Warm reset condition caused by assertion of RSTN by an external agent.
2. The RC32434 tri-states the data bus, MDATA[7:0], negates all memory control signals, and itself asserts RSTN. The RC32434 continues to drive the address bus throughout the entire warm reset.
3. The RC32434 negates RSTN after 4000 master clock (CLK) clock cycles.
4. External logic negates RSTN.
5. The RC32434 samples RSTN negated at least 4000 master clock (CLK) clock cycles after step 3 and starts driving the data bus, MDATA[7:0].
6. CPU begins executing by taking a MIPS soft reset exception. The assertion of CSN[0] will occur no sooner than 16 clock cycles after the RC32434 samples RSTN negated (i.e., step 5).

Figure 5 Externally Initiated Warm Reset AC Timing Waveform

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max		
Memory Bus - DDR Access												
DDRDATA[15:0]	Tskew_7g	DDRDQSx	0	0.9	0	0.8[1]	0	0.7	0.0	0.6	ns	See Figures 6 and 7.
	Tdo_7k[2]		1.2	1.9	1.0	1.7	0.7	1.5	0.5	1.4	ns	
DDRDM[1:0]	Tdo_7l	DDRDQSx	1.2	1.9	1.0	1.7	0.7	1.5	0.5	1.4	ns	
DDRDQS[1:0]	Tdo_7i	DDRCKP	-0.75	0.75	-0.75	0.75	-0.7	0.7	-0.7	0.7	ns	
DDRADDR[13:0], DDRBA[1:0], DDRCASN, DDRCKE, DDRCSN, DDRRASN, DDRWEN	Tdo_7m	DDRCKP	1.0	4.0	1.0	4.3	1.0	4.0	1.0	4.0	ns	

Table 7 DDR SDRAM Timing Characteristics

1. Meets DDR timing requirements for 150MHz clock rate DDR SDRAMs with 300 ps remaining margin to compensate for PCB propagation mismatches, which is adequate to guarantee functional timing, provided the RC32434 DDR layout guidelines are adhered to.

2. Setup times are calculated as applicable clock period - Tdo max. For example, if the DDR is running at 266MHz, it uses a 133MHz input clock. The period for a 133MHz clock is 7.5ns. If the Tdo max value is 4.6ns, the T_{IS} parameter is 7.5ns minus 4.6ns = 2.9ns. The DDR spec for this parameter is 1ns, so there is 1.9ns of slack left over for board propagation. Calculations for T_{DS} are similar, but since this parameter is taken relative to the DDRDQS signals, which are referenced on both edges, the effective period with a 133MHz input clock is only 3.75ns. So, if the max Tdo is 1.9ns, we have 3.75ns minus 1.9ns = 1.85ns for T_{DS}. The DDR data sheet specs a value of 0.5ns for 266MHz, so this leaves 1.35ns slack for board propagation delays.

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
MDATA[7:0]	Tsu_8c	EXTCLK rising	6.0	—	6.0	—	6.0	—	6.0	—	ns		See Figures 8 and 9 (cont.).
	Thld_8c		0	—	0	—	0	—	0	—	ns		
	Tdo_8c		0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns		
	Tdz_8c[2]		0	0.5	0	0.5	0	0.5	0	0.5	ns		
	Tzd_8c[2]		0.4	3.3	0.4	3.3	0.4	3.3	0.4	3.3	ns		
EXTCLK[3]	Tper_8d	none	7.5	—	6.66	—	6.66	—	6.66	—	ns		
BDIRN	Tdo_8e	EXTCLK rising	0.4	3.8	0.4	3.8	0.4	3.8	0.4	3.8	ns		
	Tdz_8e[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8e[2]		—	—	—	—	—	—	—	—	ns		
BOEN	Tdo_8f	EXTCLK rising	0.4	3.8	0.4	3.8	0.4	3.8	0.4	3.8	ns		
	Tdz_8f[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8f[2]		—	—	—	—	—	—	—	—	ns		
WAITACKN[4]	Tsu_8h	EXTCLK rising	6.5	—	6.5	—	6.5	—	6.5	—	ns		
	Thld_8h		0	—	0	—	0	—	0	—	ns		
	Tpw_8h[2]	none	2(EXTCLK)	—	2(EXTCLK)	—	2(EXTCLK)	—	2(EXTCLK)	—	ns		
CSN[3:0]	Tdo_8i	EXTCLK rising	0.4	4.0	0.4	4.0	0.4	4.0	0.4	4.0	ns		
	Tdz_8i[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8i[2]		—	—	—	—	—	—	—	—	ns		
RWN	Tdo_8j	EXTCLK rising	0.4	3.8	0.4	3.8	0.4	3.8	0.4	3.8	ns		
	Tdz_8j[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8j[2]		—	—	—	—	—	—	—	—	ns		
OEN	Tdo_8k	EXTCLK rising	0.4	4.0	0.4	4.0	0.4	4.0	0.4	4.0	ns		
	Tdz_8k[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8k[2]		—	—	—	—	—	—	—	—	ns		
WEN	Tdo_8l	EXTCLK rising	0.4	3.7	0.4	3.7	0.4	3.7	0.4	3.7	ns		
	Tdz_8l[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8l[2]		—	—	—	—	—	—	—	—	ns		

Table 8 Memory and Peripheral Bus AC Timing Characteristics (Part 2 of 2)

1. The RC32434 provides bus turnaround cycles to prevent bus contention when going from read to write, write to read, and during external bus ownership. For example, there are no cycles where an external device and the RC32434 are both driving. See Chapter 6, Device Controller, in the RC32434 User Reference Manual.

2. The values for this symbol were determined by calculation, not by testing.

3. The frequency of EXTCLK is programmable. See the External Clock Divider (MDATA[5:4]) description in Table 3 of this data sheet.

4. WAITACKN must meet the setup and hold times if it is synchronous or the minimum pulse width if it is asynchronous.

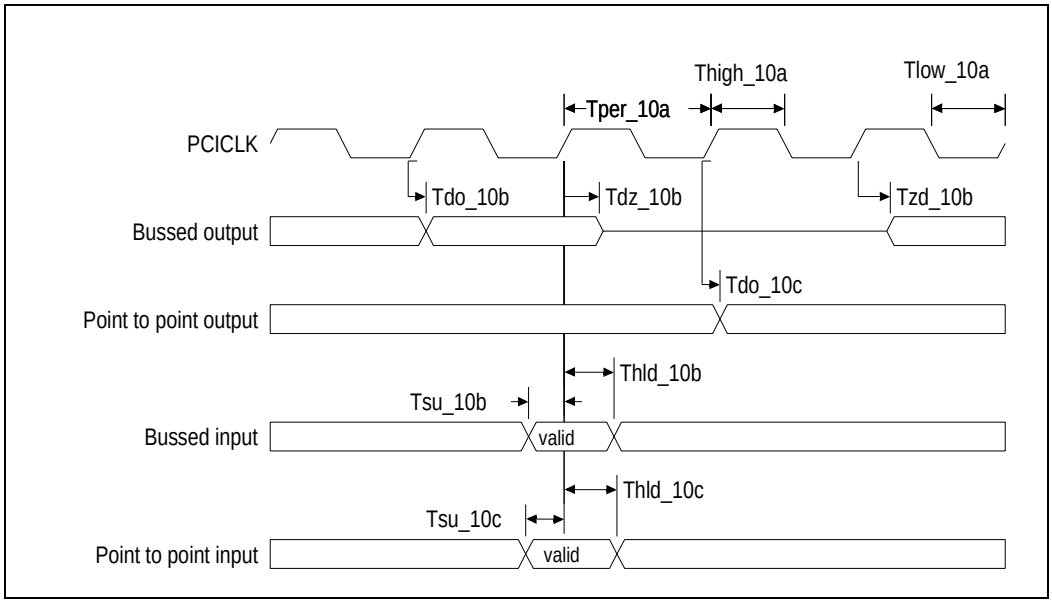
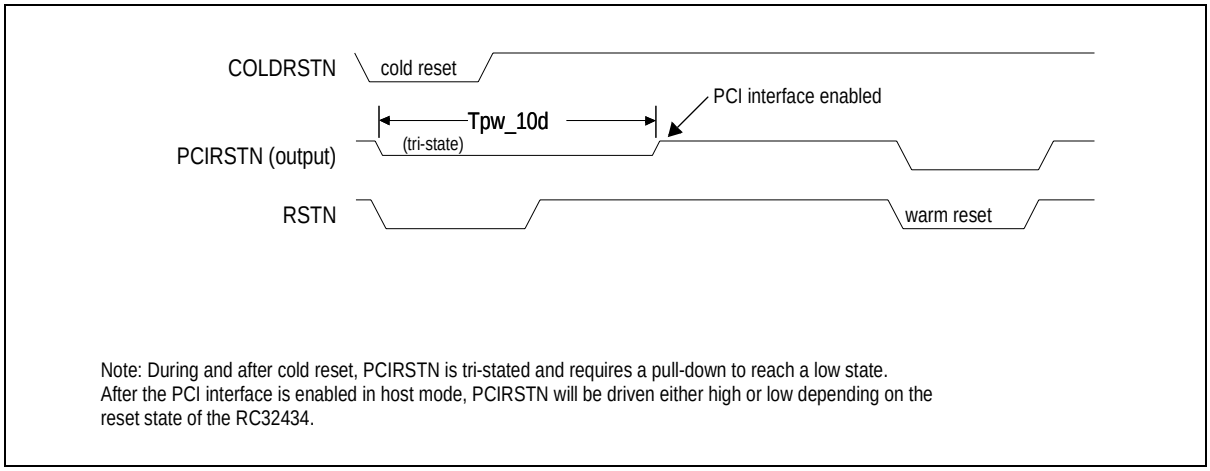


Figure 11 PCI AC Timing Waveform



Note: During and after cold reset, PCIRSTN is tri-stated and requires a pull-down to reach a low state. After the PCI interface is enabled in host mode, PCIRSTN will be driven either high or low depending on the reset state of the RC32434.

Figure 12 PCI AC Timing Waveform — PCI Reset in Host Mode

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Start or repeated start condition	Tsu_12c	SDA falling	0.6	—	0.6	—	0.6	—	0.6	—	µs	400 KHz	See Figure 14.
	Thld_12c		0.6	—	0.6	—	0.6	—	0.6	—	µs		
Stop condition	Tsu_12d	SDA rising	0.6	—	0.6	—	0.6	—	0.6	—	µs		
Bus free time between a stop and start condition	Tdelay_12e		1.3	—	1.3	—	1.3	—	1.3	—	µs		

Table 11 I²C AC Timing Characteristics (Part 2 of 2)

1. For more information, see the I²C-Bus specification by Philips Semiconductor.

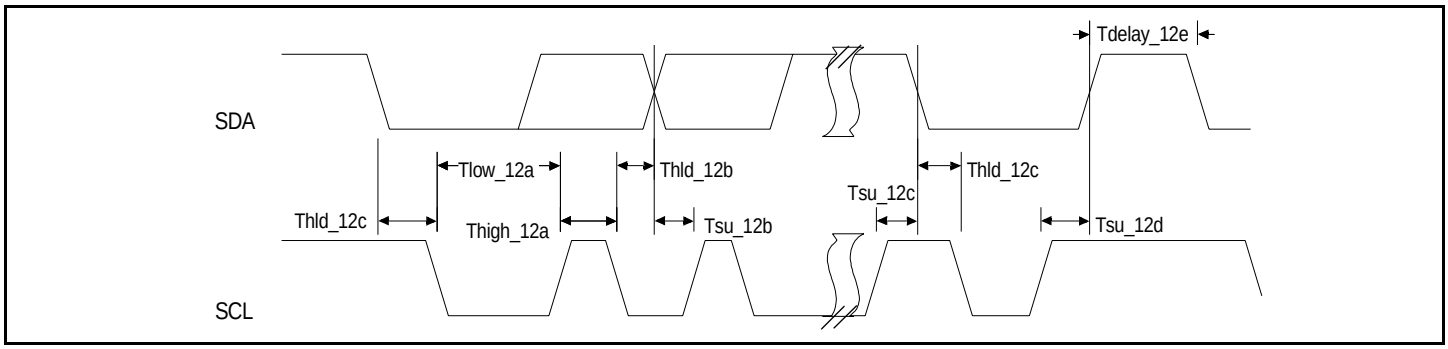


Figure 14 I2C AC Timing Waveform

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
GPIO													
GPIO[13:0]	Tpw_13b[1]	None	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	ns		See Figure 15.

Table 12 GPIO AC Timing Characteristics

1. The values for this symbol were determined by calculation, not by testing.

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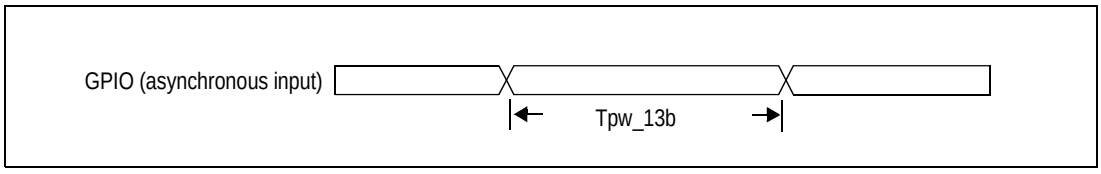


Figure 15 GPIO AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{SS}	Common ground	0	0	0	V
V_{SS}PLL	PLL ground				
V_{CC}I/O	I/O supply except for SSTL_2[1]	3.135	3.3	3.465	V
V_{CC}SI/O (DDR)	I/O supply for SSTL_2[1]	2.375	2.5	2.625	V
V_{CC}PLL	PLL supply (digital)	1.1	1.2	1.3	V
V_{CC}APLL	PLL supply (analog)	3.135	3.3	3.465	V
V_{CC}Core	Internal logic supply	1.1	1.2	1.3	V
DDRVREF[2]	SSTL_2 input reference voltage	0.5(VccSI/O)	0.5(VccSI/O)	0.5(VccSI/O)	V
V_{TT}[3]	SSTL_2 termination voltage	DDRVREF - 0.04	DDRVREF	DDRVREF + 0.04	V

Table 15 RC32434 Operating Voltages

1. SSTL_2 I/Os are used to connect to DDR SDRAM.
2. Peak-to-peak AC noise on DDRVREF may not exceed ± 2% DDRVREF (DC).
3. V_{TT} of the SSTL_2 transmitting device must track DDRVREF of the receiving device.

Recommended Operating Temperatures

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 16 RC32434 Operating Temperatures

Capacitive Load Deration

Refer to the 79RC32434 IBIS Model on the IDT web site (www.idt.com).

Power-on Sequence

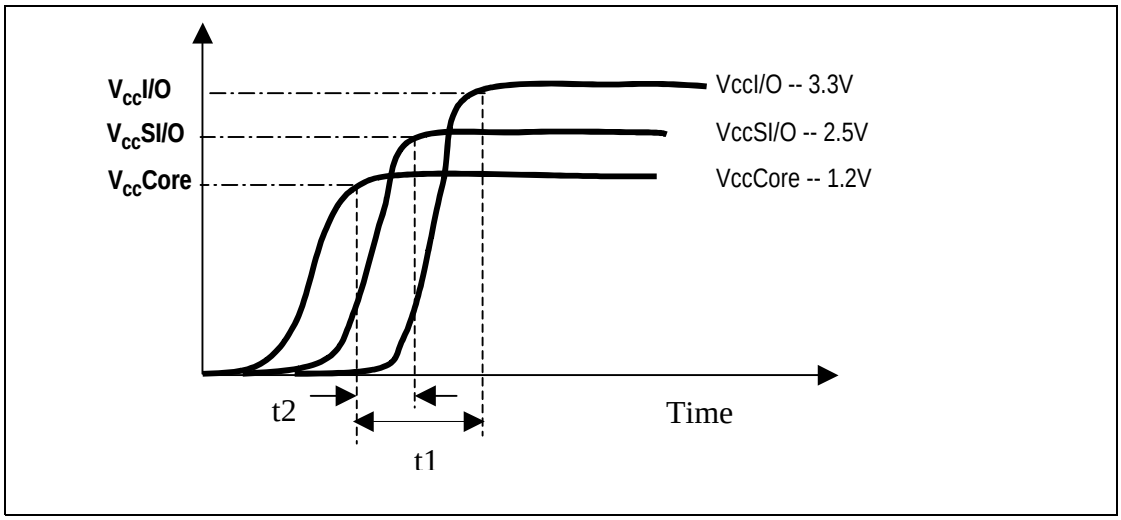
Three power-on sequences are given below. Sequence #1 is recommended because it will prevent I/O conflicts and will also allow the input signals to propagate when the I/O powers are brought up.

Note: The ESD diodes may be damaged if one of the voltages is applied and one of the other voltages is at a ground level.

A. Recommended Sequence

t2 > 0 whenever possible (V_{cc}Core)

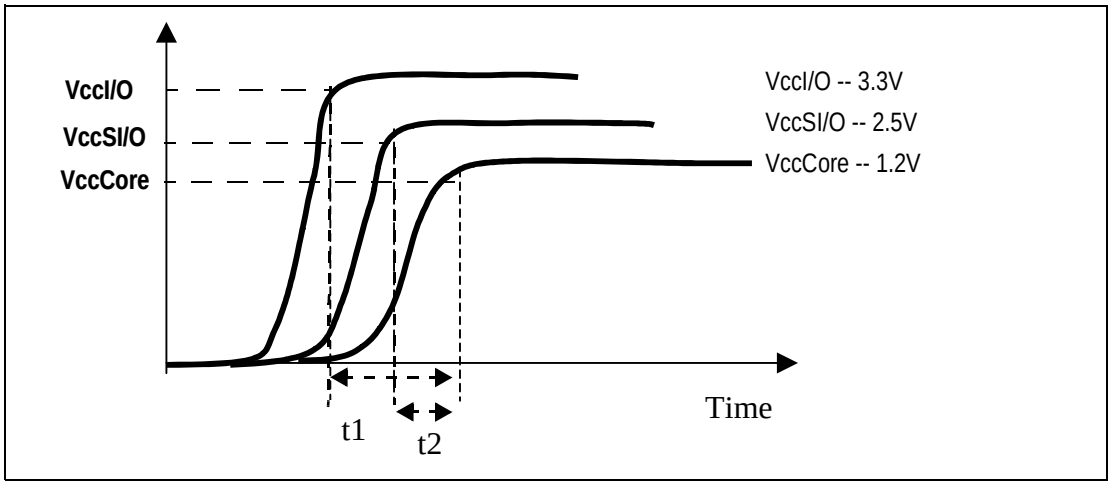
t1 - t2 can be 0 (V_{cc}SI/O followed by V_{cc}I/O)



B. Reverse Voltage Sequence

If sequence A is not feasible, then Sequence B can be used:

t1 <50ms and t2 <50ms to prevent damage.



C. Simultaneous Power-up

VccI/O, VccSI/O, and VccCore can be powered up simultaneously.

Power Consumption

Parameter		266MHz		300MHz		350MHz		400MHz		Unit	Conditions
		Typ.	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**		
I_{CC} I/O		215	270	220	275	225	280	230	285	mA	C_L = 35 pF $T_{ambient}$ = 25°C Max. values use the maximum voltages listed in Table 15. Typical values use the typical voltages listed in that table. Note: For additional information, see Power Considerations for IDT Processors on the IDT web site www.idt.com.
I_{CC} SI/O (DDR)		70	85	75	90	85	100	95	110	mA	
I_{CC} Core, I_{CC} PLL	Normal mode	325	510	350	550	400	610	450	670	mA	
	Standby mode[1]	220	—	240	—	260	—	280	—	mA	
Power Dissipation	Normal mode	1.27	1.82	1.36	1.90	1.45	2.02	1.54	2.15	W	
	Standby mode[1]	0.73	—	0.78	—	0.84	—	0.90	—	W	

Table 17 RC32434 Power Consumption

1. The RC32434 enter Standby mode by executing WAIT instructions. Minimal I/O switching is assumed. On-chip logic outside the CPU core continues to function.

Power Curve

The following graph contains a power curve that shows power consumption at various core frequencies.

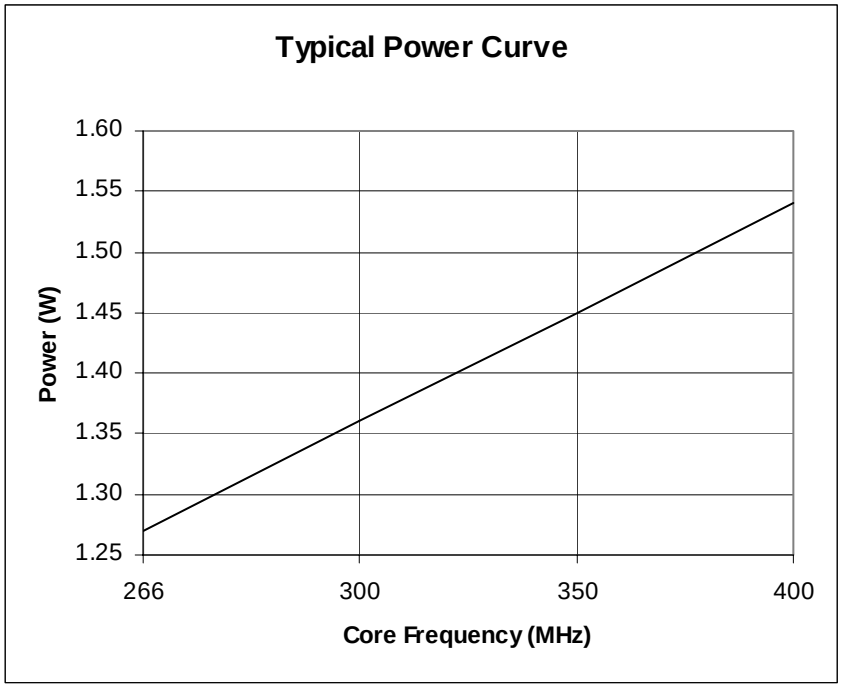


Figure 22 RC32434 Typical Power Usage

Package Pin-out — 256-BGA Signal Pinout for the RC32434

The following table lists the pin numbers, signal names, and number of alternate functions for the RC32434 device. Signal names ending with an "_n" or "n" are active when low.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	RWN		E1	MIIRXD[3]		J1	GPIO[3]	1	N1	PCIAD[29]	
A2	OEN		E2	MIIRXD[2]		J2	JTAG_TCK		N2	PCIAD[28]	
A3	CSN[2]		E3	MIITXD[0]		J3	GPIO[2]	1	N3	PCIAD[30]	
A4	CSN[0]		E4	MIITXD[1]		J4	EJTAG_TMS		N4	PCIAD[18]	
A5	MADDR[10]		E5	V_{cc} I/0		J5	V_{cc} CORE		N5	PCIREQN[1]	
A6	MDATA[6]		E6	V_{cc} I/0		J6	V_{ss}		N6	PCIREQN[2]	
A7	GPIO[7]	1	E7	V_{cc} I/0		J7	V_{ss}		N7	PCIIRDYN	
A8	GPIO[4]	1	E8	V_{cc} CORE		J8	V_{ss}		N8	PCILOCKN	
A9	MADDR[16]		E9	V_{cc} CORE		J9	V_{ss}		N9	PCIPERRN	
A10	MADDR[13]		E10	V_{cc} I/0		J10	V_{ss}		N10	PCIAD[15]	
A11	V_{ss} PLL		E11	V_{cc} DDR		J11	V_{cc} CORE		N11	PCIAD[11]	
A12	JTAG_TDI		E12	V_{cc} DDR		J12	V_{cc} CORE		N12	PCICBEN[0]	
A13	MADDR[9]		E13	DDRDATA[6]		J13	DDRCKN		N13	DDRADDR[5]	
A14	MADDR[7]		E14	DDRDATA[5]		J14	DDRVREF		N14	DDRADDR[4]	
A15	MADDR[5]		E15	DDRADDR[13]		J15	DDRCKP		N15	DDRADDR[3]	
A16	MADDR[2]		E16	DDRDATA[4]		J16	DDRDQS[0]		N16	DDRBA[0]	
B1	BOEN		F1	MIITXD[2]		K1	JTG_TDO		P1	PCIAD[27]	
B2	RSTN		F2	MIIRXCLK		K2	SCK		P2	PCIAD[26]	
B3	CSN[3]		F3	MIITXD[3]		K3	Reserved		P3	GPIO[10]	1
B4	CSN[1]		F4	MIITXENP		K4	SDO		P4	PCIAD[20]	
B5	MADDR[11]		F5	V_{cc} I/0		K5	V_{cc} I/0		P5	PCIREQN[3]	
B6	MDATA[1]		F6	V_{ss}		K6	V_{cc} I/0		P6	PCIREQN[0]	
B7	MDATA[4]		F7	V_{ss}		K7	V_{ss}		P7	PCIFRAMEN	
B8	GPIO[5]	1	F8	V_{ss}		K8	V_{ss}		P8	PCISTOPN	
B9	MADDR[17]		F9	V_{cc} CORE		K9	V_{ss}		P9	PCISERRN	
B10	MADDR[12]		F10	V_{ss}		K10	V_{ss}		P10	PCIAD[14]	
B11	V_{cc} PLL		F11	V_{ss}		K11	V_{ss}		P11	PCIAD[10]	
B12	V_{ss} APLL		F12	V_{cc} DDR		K12	V_{cc} DDR		P12	PCIAD[7]	
B13	MADDR[8]		F13	DDRDATA[9]		K13	DDRCKE		P13	PCIAD[4]	
B14	MADDR[6]		F14	DDRDATA[8]		K14	DDRADDR[11]		P14	DDRADDR[0]	
B15	MADDR[3]		F15	DDRDM[0]		K15	DDRADDR[10]		P15	DDRADDR[2]	
B16	MADDR[1]		F16	DDRDATA[7]		K16	DDRADDR[12]		P16	DDRCSN	
C1	EXTCLK		G1	MIIRXDV		L1	SDA		R1	PCIAD[25]	

Table 20 RC32434 Pinout (Part 1 of 2)

Signal Name	I/O Type	Location	Signal Category
PCISTOPN	I/O	P8	PCI Bus Interface
PCITRDYN	I/O	R8	
RSTN	I/O	B2	System
RWN	O	A1	Memory and Peripheral Bus
SCK	I/O	K2	Serial Peripheral Interface
SCL	I/O	L2	I^2C
SDA	I/O	L1	
SDI	I/O	L4	Serial Peripheral Interface
SDO	I/O	K4	
Vcc APLL		C12	Power
Vcc Core		E8, E9, F9, H5, H6, H12, J5, J11, J12, L8, M8, M9	
Vcc DDR		E11, E12, F12, G12, K12, L12, M11, M12	
Vcc I/O		E5, E6, E7, E10, F5, G5, K5, K6, L5, M5, M6, M7, M10	
Vcc PLL		B11	
Vss		F6, F7, F8, F10, F11, G6, G7, G8, G9, G10, G11, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, K7, K8, K9, K10, K11, L6, L7, L9, L10, L11	Ground
Vss APLL		B12	
Vss PLL		A11	
WAITACKN	I	D13	Memory and Peripheral Bus
WEN	O	C4	
Reserved		K3, L1, L2	

Table 24 RC32434 Alphabetical Signal List (Part 7 of 7)