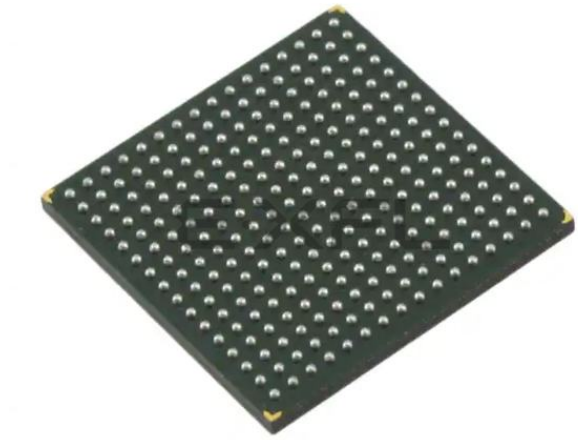

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | MIPS32 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 300MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DDR |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100Mbps (1) |
| SATA | - |
| USB | - |
| Voltage - I/O | 3.3V |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Security Features | - |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-CABGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/79rc32h434-300bci |

### DMA Controller

The DMA controller consists of 6 independent DMA channels, all of which operate in exactly the same manner. The DMA controller off-loads the CPU core from moving data among the on-chip interfaces, external peripherals, and memory. The controller supports scatter/gather DMA with no alignment restrictions, making it appropriate for communications and graphics systems.

### UART Interface

The RC32434 contains a serial channel (UART) that is compatible with the industry standard 16550 UART.

### $I^2C$ Interface

The standard I2C interface allows the RC32434 to connect to a number of standard external peripherals for a more complete system solution. The RC32434 supports both master and slave operations.

### General Purpose I/O Controller

The RC32434 has 14 general purpose input/output pins. Each pin may be used as an active high or active low level interrupt or non-maskable interrupt input, and each signal may be used as a bit input or output port.

### System Integrity Functions

The RC32434 contains a programmable watchdog timer that generates a non-maskable interrupt (NMI) when the counter expires and also contains an address space monitor that reports errors in response to accesses to undecoded address regions.

## Thermal Considerations

The RC32434 is guaranteed in an ambient temperature range of 0° to +70° C for commercial temperature devices and - 40° to +85° for industrial temperature devices.

## Revision History

**November 3, 2003**: Initial publication. Preliminary Information.

**December 15, 2003**: Final version. In Table 7, changed maximum value for Tskew in 266MHz category and changed values for Tdo in all speed grades for signals DDRADDR, etc. In Table 8, changed minimum values in all speed grades for all Tdo signals and for Tsu and Tzd in MDATA[7:0]. In Table 16, added reference to Power Considerations document. In Table 17, added 2 rows under PCI and Notes 1 and 2.

**January 5, 2004**: In Table 19, Pin F6 was changed from Vcc I/O to Vss. In Table 23, pin F6 was deleted from the Vcc I/O row and added to the Vss row.

**January 27, 2004**: In Table 3, revised description for MADDR[3:0] and changed 4096 cycles to 4000 for MADDR[7]. (Note: MADDR was incorrectly labeled as MDATA in previous data sheet.)

**March 29, 2004**: Added Standby mode to Table 16, Power Consumption.

**April 19, 2004**: Added the $I^2C$ feature. In Table 20, pin L1 becomes SDA and pin L2 becomes SCL.

**May 25, 2004**: In Table 9, signals MIIRXCLK and MIITXCLK, the Min and Max values for Thigh/Tlow_9c were changed to 140 and 260 respectively and the Min and Max values for Thigh/Tlow_9d were changed to 14.0 and 26.0 respectively.

**December 8, 2005**: In Table 18, corrected error for Capacitance Max value from 8.0 to 10.5.

**January 19, 2006**: Removed all references to NVRAM.

## Pin Description Table

The following table lists the functions of the pins provided on the RC32434. Some of the functions listed may be multiplexed onto the same pin.

The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

| Signal | Type | Name/Description |
|---|---|---|
| **Memory and Peripheral Bus** | | |
| BDIRN | O | **External Buffer Direction.** Controls the direction of the external data bus buffer for the memory and peripheral bus. If the RC32434 memory and peripheral bus is connected to the A side of a transceiver, such as an IDT74FCT245, then this pin may be directly connected to the direction control (e.g., BDIR) pin of the transceiver. |
| BOEN | O | **External Buffer Enable.** This signal provides an output enable control for an external buffer on the memory and peripheral data bus. |
| WEN | O | **Write Enables.** This signal is the memory and peripheral bus write enable signal. |
| CSN[3:0] | O | **Chip Selects.** These signals are used to select an external device on the memory and peripheral bus. |
| MADDR[21:0] | O | **Address Bus.** 22-bit memory and peripheral bus address bus. MADDR[25:22] are available as GPIO alternate functions. |
| MDATA[7:0] | I/O | **Data Bus.** 8-bit memory and peripheral data bus. During a cold reset, these pins function as inputs that are used to load the boot configuration vector. |
| OEN | O | **Output Enable.** This signal is asserted when data should be driven by an external device on the memory and peripheral bus. |
| RWN | O | **Read Write.** This signal indicates whether the transaction on the memory and peripheral bus is a read transaction or a write transaction. A high level indicates a read from an external device. A low level indicates a write to an external device. |
| WAITACKN | I | **Wait or Transfer Acknowledge.** When configured as wait, this signal is asserted during a memory and peripheral bus transaction to extend the bus cycle. When configured as a transfer acknowledge, this signal is asserted during a transaction to signal the completion of the transaction. |
| **DDR Bus** | | |
| DDRADDR[13:0] | O | **DDR Address Bus.** 14-bit multiplexed DDR address bus. This bus is used to transfer the addresses to the DDR devices. |
| DDRBA[1:0] | O | **DDR Bank Address.** These signals are used to transfer the bank address to the DDRs. |
| DDRCASN | O | **DDR Column Address Strobe.** This signal is asserted during DDR transactions. |
| DDRCKE | O | **DDR Clock Enable.** The DDR clock enable signal is asserted during normal DDR operation. This signal is negated following a cold reset or during a power down operation. |
| DDRCKN | O | **DDR Negative DDR clock.** This signal is the negative clock of the differential DDR clock pair. |

**Table 1 Pin Description (Part 1 of 6)**

# AC Timing Definitions

Below are examples of the AC timing characteristics used throughout this document.

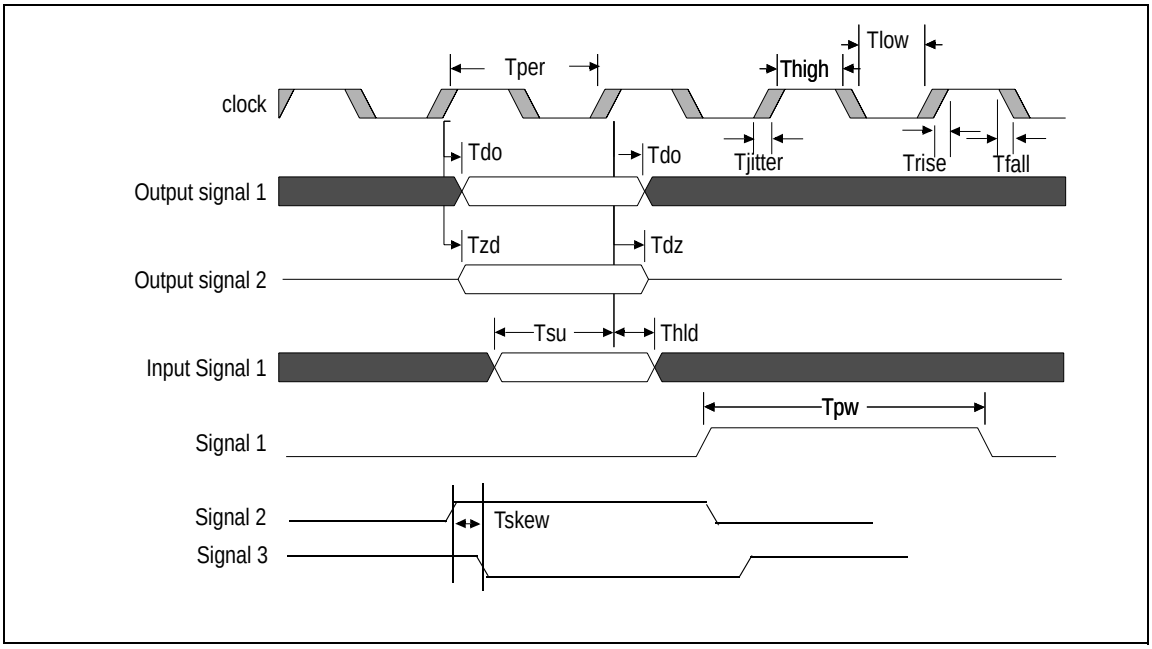
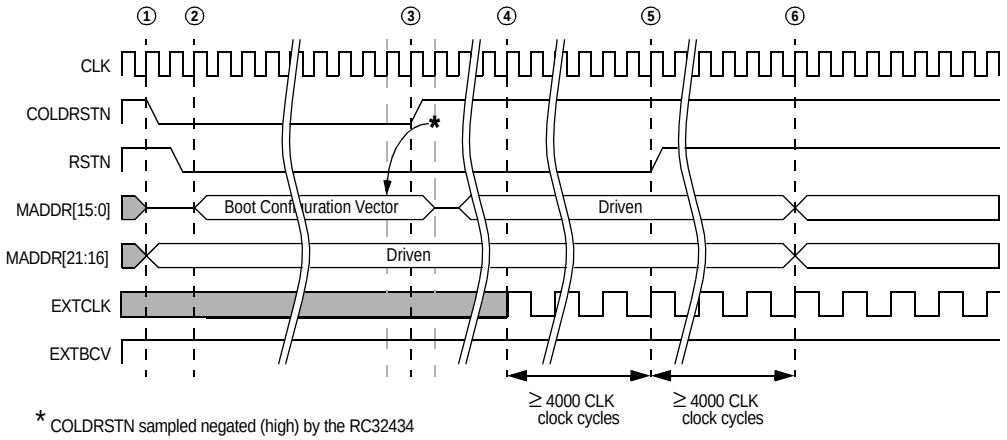



**Figure 2 AC Timing Definitions Waveform**

| Symbol | Definition |
|---|---|
| Tper | Clock period. |
| Tlow | Clock low. Amount of time the clock is low in one clock period. |
| Thigh | Clock high. Amount of time the clock is high in one clock period. |
| Trise | Rise time. Low to high transition time. |
| Tfall | Fall time. High to low transition time. |
| Tjitter | Jitter. Amount of time the reference clock (or signal) edge can vary on either the rising or falling edges. |
| Tdo | Data out. Amount of time after the reference clock edge that the output will become valid. The minimum time represents the data output hold. The maximum time represents the earliest time the designer can use the data. |
| Tzd | Z state to data valid. Amount of time after the reference clock edge that the tri-stated output takes to become valid. |
| Tdz | Data valid to Z state. Amount of time after the reference clock edge that the valid output takes to become tri-stated. |
| Tsu | Input set-up. Amount of time before the reference clock edge that the input must be valid. |
| Thld | Input hold. Amount of time after the reference clock edge that the input must remain valid. |
| Tpw | Pulse width. Amount of time the input or output is active for asynchronous signals. |
| Tslew | Slew rate. The rise or fall rate for a signal to go from a high to low, or low to high. |
| X(clock) | Timing value. This notation represents a value of 'X' multiplied by the clock time period of the specified clock. Using 5(CLK) as an example: X = 5 and the oscillator clock (CLK) = 25MHz, then the timing value is 200. |
| Tskew | Skew. The amount of time two signal edges deviate from one another. |

**Table 4 AC Timing Definitions**




1. EXTBCV is asserted (i.e., pulled-up). COLDRSTN is asserted by external logic. The RC32434 responds by immediately tri-stating the bottom 16-bits of the memory and peripheral address bus (MADDR[15:0]), driving the remaining address bus signals (i.e., MADDR[21:16]), and asserting RSTN. EXTCLK is undefined at this point.
2. External logic drives the boot configuration vector on MADDR[15:0].
3. External logic negates COLDRSTN and tri-states the boot configuration vector on MADDR[15:0]. In response, the RC32434 stops sampling the boot configuration vector and retains the boot configuration vector value seen two clock cycles earlier (i.e., the value on the MADDR[15:0] lines two rising edges of CLK earlier). Within 16 CLK clock cycles after COLDRSTN is sampled negated, the RC32434 begins driving MADDR[15:0].
4. The RC32434 waits for the PLL to stabilize.
5. The RC32434 then begins generating EXTCLK.
6. After at least 4000 CLK clock cycles, the RC32434 tri-states RSTN.
7. At least 4000 CLK clock cycles after negating RSTN, the RC32434 samples RSTN. If RSTN is negated, cold reset has completed and the RC32434 CPU begins executing by taking MIPS reset exception.

**Figure 4 COLD Reset Operation with External Boot Configuration Vector AC Timing Waveform**

**Note:** For a diagram showing the COLD Reset Operation with Internal Boot Configuration Vector, see Figure 3.6 in the RC32434 User Reference Manual.

| Signal | Symbol | Reference Edge | 266MHz | | 300MHz | | 350MHz | | 400MHz | | Unit | Conditions | Timing Diagram Reference |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | | | |
| MDATA[7:0] | Tsu_8c | EXTCLK rising | 6.0 | — | 6.0 | — | 6.0 | — | 6.0 | — | ns | | See Figures 8 and 9 (cont.). |
| | Thld_8c | | 0 | — | 0 | — | 0 | — | 0 | — | ns | | |
| | Tdo_8c | | 0.4 | 4.5 | 0.4 | 4.5 | 0.4 | 4.5 | 0.4 | 4.5 | ns | | |
| | Tdz_8c[2] | | 0 | 0.5 | 0 | 0.5 | 0 | 0.5 | 0 | 0.5 | ns | | |
| | Tzd_8c[2] | | 0.4 | 3.3 | 0.4 | 3.3 | 0.4 | 3.3 | 0.4 | 3.3 | ns | | |
| EXTCLK[3] | Tper_8d | none | 7.5 | — | 6.66 | — | 6.66 | — | 6.66 | — | ns | | |
| BDIRN | Tdo_8e | EXTCLK rising | 0.4 | 3.8 | 0.4 | 3.8 | 0.4 | 3.8 | 0.4 | 3.8 | ns | | |
| | Tdz_8e[2] | | — | — | — | — | — | — | — | — | ns | | |
| | Tzd_8e[2] | | — | — | — | — | — | — | — | — | ns | | |
| BOEN | Tdo_8f | EXTCLK rising | 0.4 | 3.8 | 0.4 | 3.8 | 0.4 | 3.8 | 0.4 | 3.8 | ns | | |
| | Tdz_8f[2] | | — | — | — | — | — | — | — | — | ns | | |
| | Tzd_8f[2] | | — | — | — | — | — | — | — | — | ns | | |
| WAITACKN[4] | Tsu_8h | EXTCLK rising | 6.5 | — | 6.5 | — | 6.5 | — | 6.5 | — | ns | | |
| | Thld_8h | | 0 | — | 0 | — | 0 | — | 0 | — | ns | | |
| | Tpw_8h[2] | none | 2(EXTCLK) | — | 2(EXTCLK) | — | 2(EXTCLK) | — | 2(EXTCLK) | — | ns | | |
| CSN[3:0] | Tdo_8i | EXTCLK rising | 0.4 | 4.0 | 0.4 | 4.0 | 0.4 | 4.0 | 0.4 | 4.0 | ns | | |
| | Tdz_8i[2] | | — | — | — | — | — | — | — | — | ns | | |
| | Tzd_8i[2] | | — | — | — | — | — | — | — | — | ns | | |
| RWN | Tdo_8j | EXTCLK rising | 0.4 | 3.8 | 0.4 | 3.8 | 0.4 | 3.8 | 0.4 | 3.8 | ns | | |
| | Tdz_8j[2] | | — | — | — | — | — | — | — | — | ns | | |
| | Tzd_8j[2] | | — | — | — | — | — | — | — | — | ns | | |
| OEN | Tdo_8k | EXTCLK rising | 0.4 | 4.0 | 0.4 | 4.0 | 0.4 | 4.0 | 0.4 | 4.0 | ns | | |
| | Tdz_8k[2] | | — | — | — | — | — | — | — | — | ns | | |
| | Tzd_8k[2] | | — | — | — | — | — | — | — | — | ns | | |
| WEN | Tdo_8l | EXTCLK rising | 0.4 | 3.7 | 0.4 | 3.7 | 0.4 | 3.7 | 0.4 | 3.7 | ns | | |
| | Tdz_8l[2] | | — | — | — | — | — | — | — | — | ns | | |
| | Tzd_8l[2] | | — | — | — | — | — | — | — | — | ns | | |

**Table 8 Memory and Peripheral Bus AC Timing Characteristics (Part 2 of 2)**

1. The RC32434 provides bus turnaround cycles to prevent bus contention when going from read to write, write to read, and during external bus ownership. For example, there are no cycles where an external device and the RC32434 are both driving. See Chapter 6, Device Controller, in the RC32434 User Reference Manual.

2. The values for this symbol were determined by calculation, not by testing.

3. The frequency of EXTCLK is programmable. See the External Clock Divider (MDATA[5:4]) description in Table 3 of this data sheet.

4. WAITACKN must meet the setup and hold times if it is synchronous or the minimum pulse width if it is asynchronous.

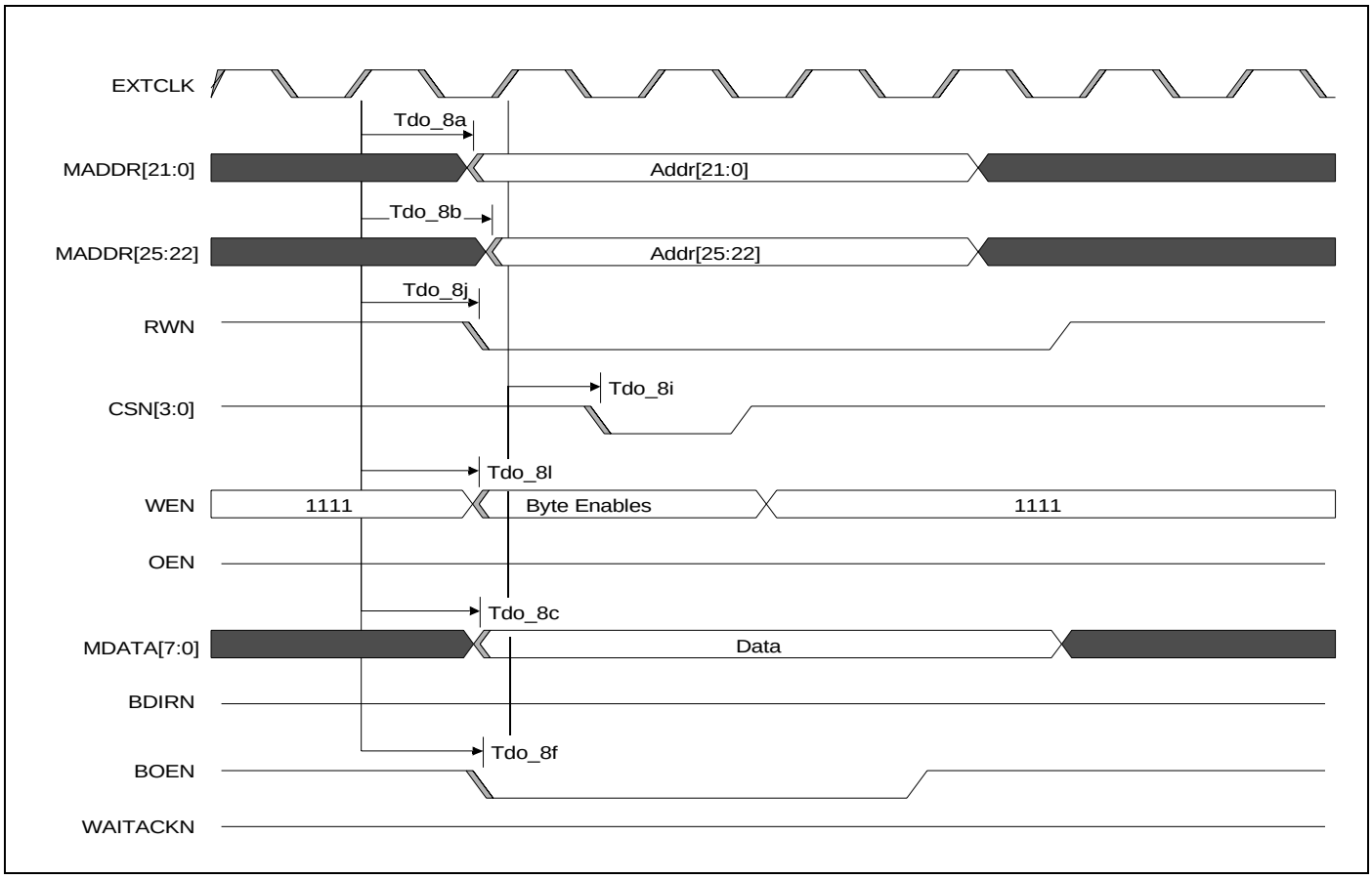



**Figure 9 Memory and Peripheral Bus AC Timing Waveform — Write Access**

| Signal | Symbol | Reference Edge | 266MHz | | 300MHz | | 350MHz | | 400MHz | | Unit | Conditions | Timing Diagram Reference |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | | | |
| **Ethernet** | | | | | | | | | | | | | |
| MIIMDC | Tper_9a | None | 30.0 | — | 30.0 | — | 30.0 | — | 30.0 | — | ns | | See Figure 10. |
| | Thigh_9a, Tlow_9a | | 12.0 | — | 12.0 | — | 12.0 | — | 12.0 | — | ns | | |
| MIIMDIO | Tsu_9b | MIIMDC rising | 10.0 | — | 10.0 | — | 10.0 | — | 10.0 | — | ns | | |
| | Thld_9b | | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | — | ns | | |
| | Tdo_9b[1] | | 10 | 300 | 10 | 300 | 10 | 300 | 10 | 300 | ns | | |
| **Ethernet — MII Mode** | | | | | | | | | | | | | |
| MIIRXCLK, MIITXCLK[2] | Tper_9c | None | 399.96 | 400.4 | 399.96 | 400.4 | 399.96 | 400.4 | 399.96 | 400.4 | ns | 10 Mbps | See Figure 10. |
| | Thigh_9c, Tlow_9c | | 140 | 260 | 140 | 260 | 140 | 260 | 140 | 260 | ns | | |
| | Trise_9c, Tfall_9c | | — | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | ns | | |
| MIIRXCLK, MIITXCLK[2] | Tper_9d | None | 39.9 | 40.0 | 39.9 | 40.0 | 39.9 | 40.0 | 39.9 | 40.0 | ns | 100 Mbps | |
| | Thigh_9d, Tlow_9d | | 14.0 | 26.0 | 14.0 | 26.0 | 14.0 | 26.0 | 14.0 | 26.0 | ns | | |
| | Trise_9d, Tfall_9d | | — | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | ns | | |
| MIIRXD[3:0], MIIRXDV, MIIRXER | Tsu_9e | MIIxRXCLK rising | 10.0 | — | 10.0 | — | 10.0 | — | 10.0 | — | ns | | |
| | Thld_9e | | 10.0 | — | 10.0 | — | 10.0 | — | 10.0 | — | ns | | |
| MIITXD[3:0], MIITXENP, MIITXER | Tdo_9f | MIIxTXCLK rising | 0.0 | 25.0 | 0.0 | 25.0 | 0.0 | 25.0 | 0.0 | 25.0 | ns | | |
| **Ethernet — RMII Mode** | | | | | | | | | | | | | |
| RMIIREFCLK | Tper_9i | None | 19.9 | 20.1 | 19.9 | 20.1 | 19.9 | 20.1 | 19.9 | 20.1 | ns | | See Figure 10. |
| | Thigh_9i, Tlow_9i | | 7.0 | 13.0 | 7.0 | 13.0 | 7.0 | 13.0 | 7.0 | 13.0 | ns | | |
| RMIITXEN, RMIITXD[1:0] | Tdo_9j | MIIRXCLK rising | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | ns | | |
| RMIICRSDV, RMIIRXER, RMIIRXD[1:0] | Tsu_9k | | 5.5 | 14.5 | 5.5 | 14.5 | 5.5 | 14.5 | 5.5 | 14.5 | ns | | |

**Table 9 Ethernet AC Timing Characteristics**

1. The values for this symbol were determined by calculation, not by testing.

2. The ethernet clock (MIIRXCLK and MIITXCLK) frequency must be equal to or less than 1/2 ICLK (MIIRXCLK and MIITXCLK <= 1/2(ICLK)).

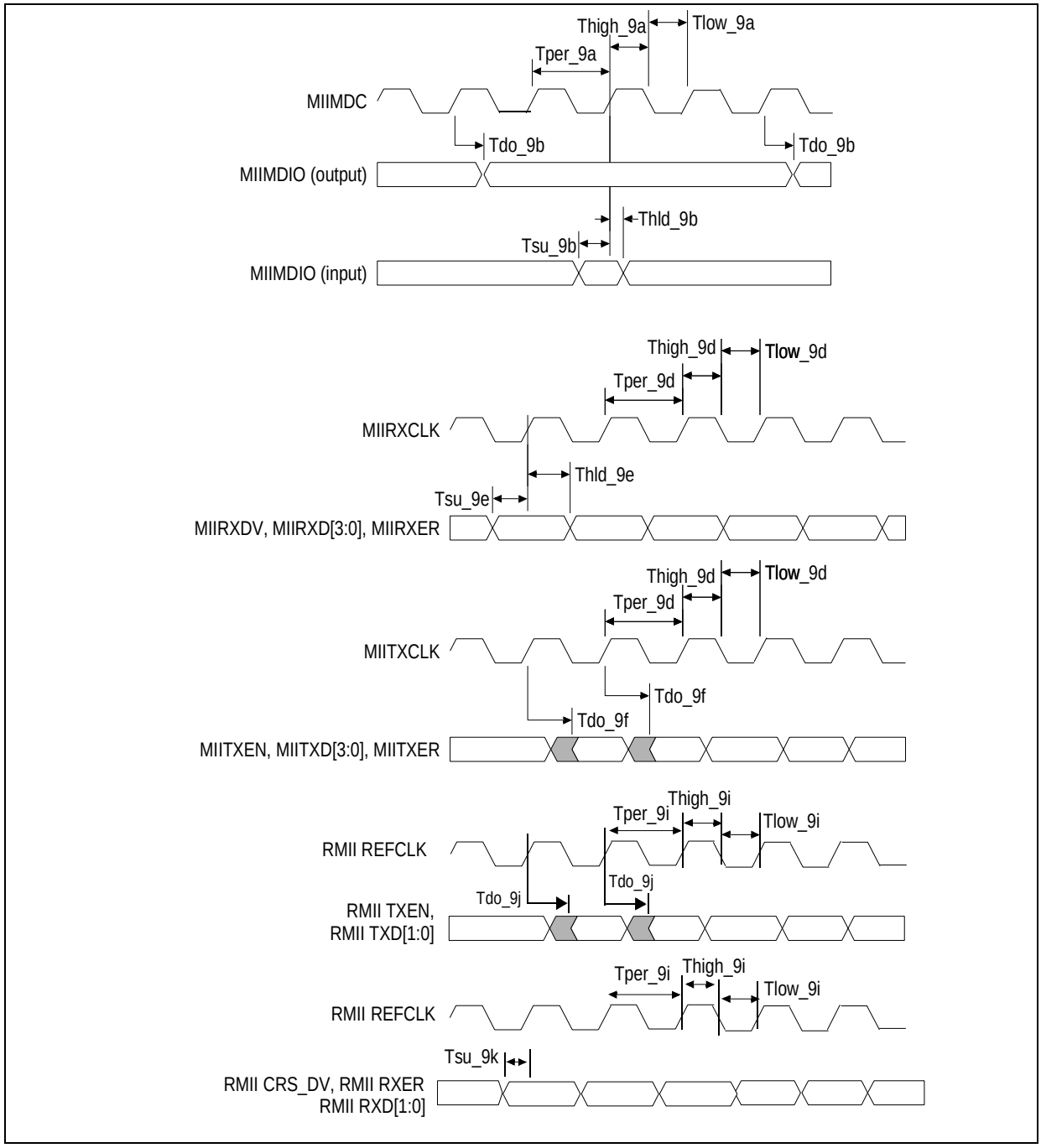



**Figure 10 Ethernet AC Timing Waveform**

| Signal | Symbol | Reference Edge | 266MHz | | 300MHz | | 350MHz | | 400MHz | | Unit | Conditions | Timing Diagram Reference |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | | | |
| **PCI**[1] | | | | | | | | | | | | | |
| PCICLK[2] | Tper_10a | none | 15.0 | 30.0 | 15.0 | 30.0 | 15.0 | 30.0 | 15.0 | 30.0 | ns | 66 MHz PCI | See Figure 11. |
| | Thigh_10a, Tlow_10a | | 6.0 | — | 6.0 | — | 6.0 | — | 6.0 | — | ns | | |
| | Tslew_10a | | 1.5 | 4.0 | 1.5 | 4.0 | 1.5 | 4.0 | 1.5 | 4.0 | V/ns | | |
| PCIAD[31:0], PCIBEN[3:0], PCIDEVSELN, PCIFRAMEN,PCIIRDYN, PCILOCKN, PCIPAR, PCIPERRN, PCISTOPN, PCITRDY | Tsu_10b | PCICLK rising | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | — | ns | | |
| | Thld_10b | | 0 | — | 0 | — | 0 | — | 0 | — | ns | | |
| | Tdo_10b | | 2.0 | 6.0 | 2.0 | 6.0 | 2.0 | 6.0 | 2.0 | 6.0 | ns | | |
| | Tdz_10b[3] | | — | 14.0 | — | 14.0 | — | 14.0 | — | 14.0 | ns | | |
| | Tzd_10b[3] | | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | ns | | |
| PCIGNTN[3:0], PCIREQN[3:0] | Tsu_10c | PCICLK rising | 5.0 | — | 5.0 | — | 5.0 | — | 5.0 | — | ns | | |
| | Thld_10c | | 0 | — | 0 | — | 0 | — | 0 | — | ns | | |
| | Tdo_10c | | 2.0 | 6.0 | 2.0 | 6.0 | 2.0 | 6.0 | 2.0 | 6.0 | ns | | |
| PCIRSTN (output)[4] | Tpw_10d[3] | None | 4000 (CLK) | — | 4000 (CLK) | — | 4000 (CLK) | — | 4000 (CLK) | — | ns | | See Figures 15 and 16 |
| PCIRSTN (input)[4,5] | Tpw_10e[3] | None | 2(CLK) | — | 2(CLK) | — | 2(CLK) | — | 2(CLK) | — | ns | | |
| | Tdz_10e[3] | PCIRSTN falling | 6(CLK) | — | 6(CLK) | — | 6(CLK) | — | 6(CLK) | — | ns | | |
| PCISERRN[6] | Tsu_10f | PCICLK rising | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | — | ns | | See Figure 11 |
| | Thld_10f | | 0 | — | 0 | — | 0 | — | 0 | — | ns | | |
| | Tdo_10f | | 2.0 | 6.0 | 2.0 | 6.0 | 2.0 | 6.0 | 2.0 | 6.0 | ns | | |
| PCIMUINTN[6] | Tdo_10g | PCICLK rising | 4.7 | 11.1 | 4.7 | 11.1 | 4.7 | 11.1 | 4.7 | 11.1 | ns | | |

**Table 10 PCI AC Timing Characteristics**

1. This PCI interface conforms to the PCI Local Bus Specification, Rev 2.2.

2. PCICLK must be equal to or less than two times ICLK (PCICLK <= 2(ICLK)) with a maximum PCICLK of 66 MHz.

3. The values for this symbol were determined by calculation, not by testing.

4. PCIRSTN is an output in host mode and an input in satellite mode.

5. To meet the PCI delay specification from reset asserted to outputs floating, the PCI reset should be logically combined with the COLDRSTN input, instead of input on PCIRSTN.

6. PCISERRN and PCIMUINTN use open collector I/O types.

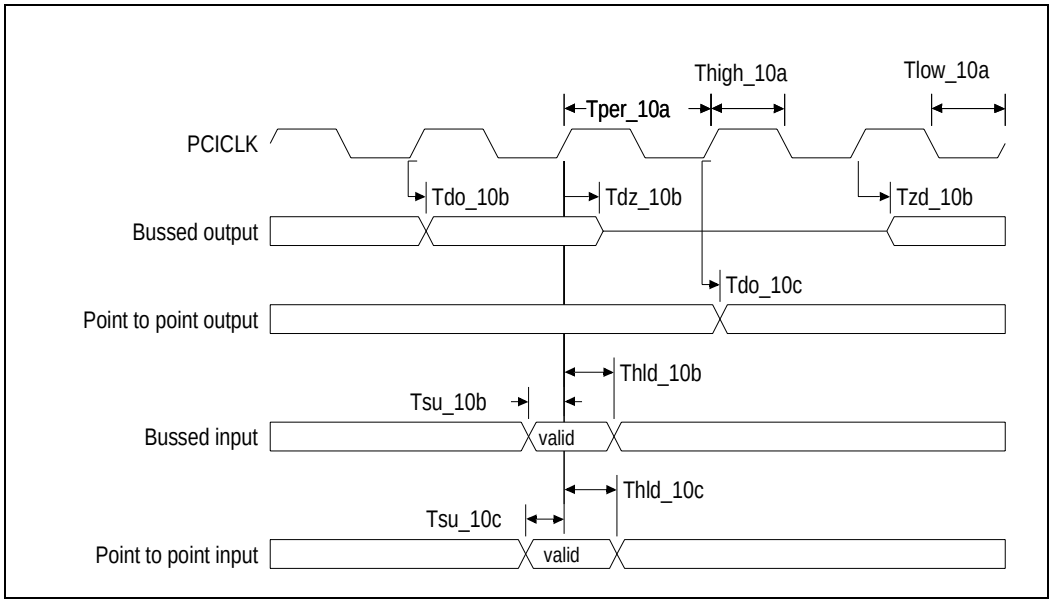
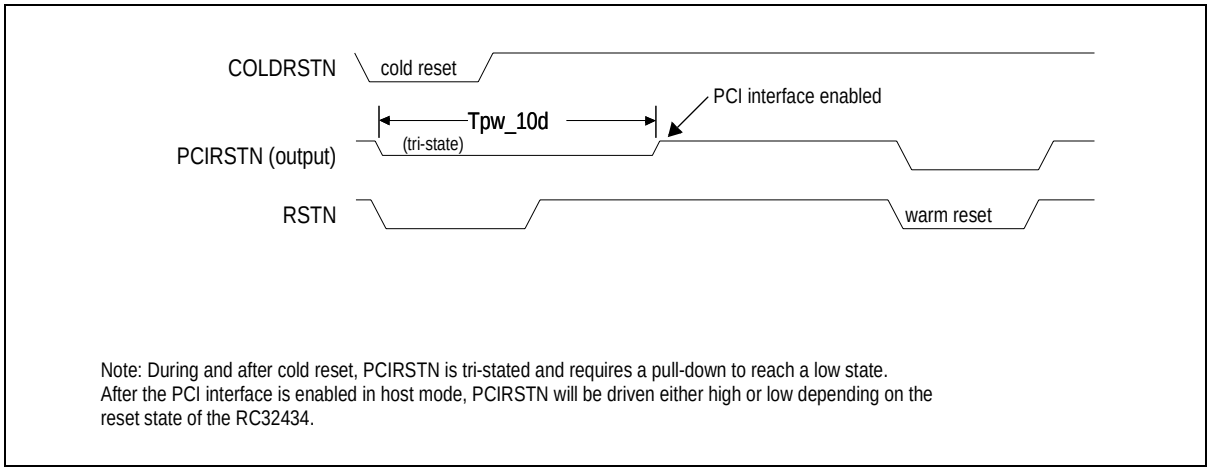



**Figure 11 PCI AC Timing Waveform**




Note: During and after cold reset, PCIRSTN is tri-stated and requires a pull-down to reach a low state. After the PCI interface is enabled in host mode, PCIRSTN will be driven either high or low depending on the reset state of the RC32434.

**Figure 12 PCI AC Timing Waveform — PCI Reset in Host Mode**

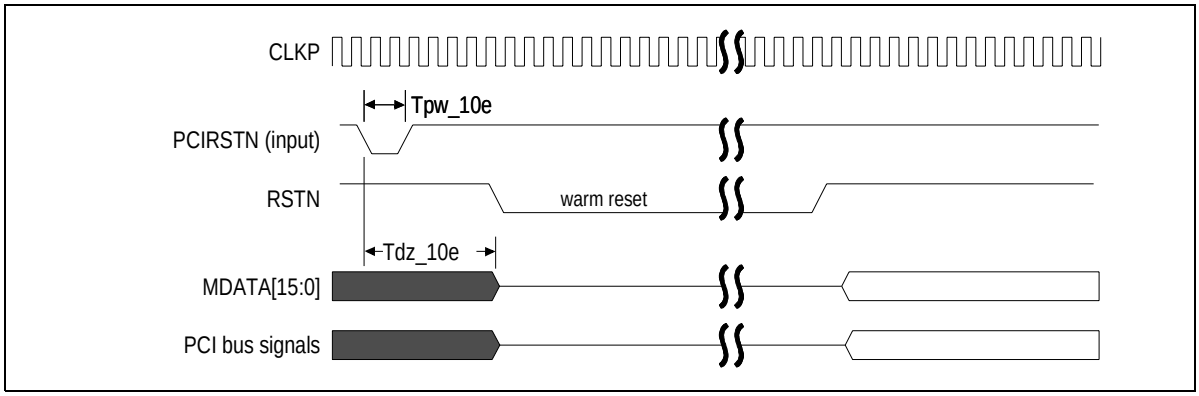



**Figure 13 PCI AC Timing Waveform — PCI Reset in Satellite Mode**

| Signal | Symbol | Reference Edge | 266MHz | | 300MHz | | 350MHz | | 400MHz | | Unit | Conditions | Timing Diagram Reference |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | | | |
| **I²C[1]** | | | | | | | | | | | | | |
| SCL | Frequency | none | 0 | 100 | 0 | 100 | 0 | 100 | 0 | 100 | kHz | 100 KHz | See Figure 14. |
| | Thigh_12a, Tlow_12a | | 4.0 | — | 4.0 | — | 4.0 | — | 4.0 | — | µs | | |
| | Trise_12a | | — | 1000 | — | 1000 | — | 1000 | — | 1000 | ns | | |
| | Tfall_12a | | — | 300 | — | 300 | — | 300 | — | 300 | ns | | |
| SDA | Tsu_12b | SCL rising | 250 | — | 250 | — | 250 | — | 250 | — | ns | | |
| | Thld_12b | | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | µs | | |
| | Trise_12b | | — | 1000 | — | 1000 | — | 1000 | — | 1000 | ns | | |
| | Tfall_12b | | — | 300 | — | 300 | — | 300 | — | 300 | ns | | |
| Start or repeated start condition | Tsu_12c | SDA falling | 4.7 | — | 4.7 | — | 4.7 | — | 4.7 | — | µs | | |
| | Thld_12c | | 4.0 | — | 4.0 | — | 4.0 | — | 4.0 | — | µs | | |
| Stop condition | Tsu_12d | SDA rising | 4.0 | — | 4.0 | — | 4.0 | — | 4.0 | — | µs | | |
| Bus free time between a stop and start condition | Tdelay_12e | | 4.7 | — | 4.7 | — | 4.7 | — | 4.7 | — | µs | | |
| SCL | Frequency | none | 0 | 400 | 0 | 400 | 0 | 400 | 0 | 400 | kHz | 400 KHz | |
| | Thigh_12a, Tlow_12a | | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | — | µs | | |
| | Trise_12a | | — | 300 | — | 300 | — | 300 | — | 300 | ns | | |
| | Tfall_12a | | — | 300 | — | 300 | — | 300 | — | 300 | ns | | |
| SDA | Tsu_12b | SCL rising | 100 | — | 100 | — | 100 | — | 100 | — | ns | | |
| | Thld_12b | | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | µs | | |
| | Trise_12b | | — | 300 | — | 300 | — | 300 | — | 300 | ns | | |
| | Tfall_12ba | | — | 300 | — | 300 | — | 300 | — | 300 | ns | | |

**Table 11 I²C AC Timing Characteristics (Part 1 of 2)**

| Signal | Symbol | Reference Edge | 266MHz | | 300MHz | | 350MHz | | 400MHz | | Unit | Conditions | Timing Diagram Reference |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | | | |
| Start or repeated start condition | Tsu_12c | SDA falling | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | — | µs | 400 KHz | See Figure 14. |
| | Thld_12c | | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | — | µs | | |
| Stop condition | Tsu_12d | SDA rising | 0.6 | — | 0.6 | — | 0.6 | — | 0.6 | — | µs | | |
| Bus free time between a stop and start condition | Tdelay_12e | | 1.3 | — | 1.3 | — | 1.3 | — | 1.3 | — | µs | | |

**Table 11 I²C AC Timing Characteristics (Part 2 of 2)**

1. For more information, see the I²C-Bus specification by Philips Semiconductor.

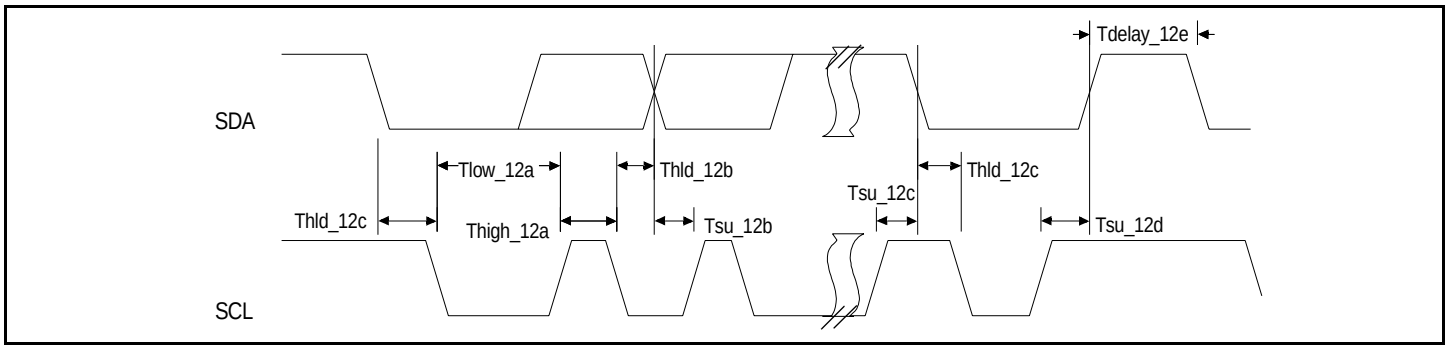



**Figure 14 I2C AC Timing Waveform**

| Signal | Symbol | Reference Edge | 266MHz | | 300MHz | | 350MHz | | 400MHz | | Unit | Conditions | Timing Diagram Reference |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | | | |
| **GPIO** | | | | | | | | | | | | | |
| GPIO[13:0] | Tpw_13b[1] | None | 2(ICLK) | — | 2(ICLK) | — | 2(ICLK) | — | 2(ICLK) | — | ns | | See Figure 15. |

**Table 12 GPIO AC Timing Characteristics**

1. The values for this symbol were determined by calculation, not by testing.

\

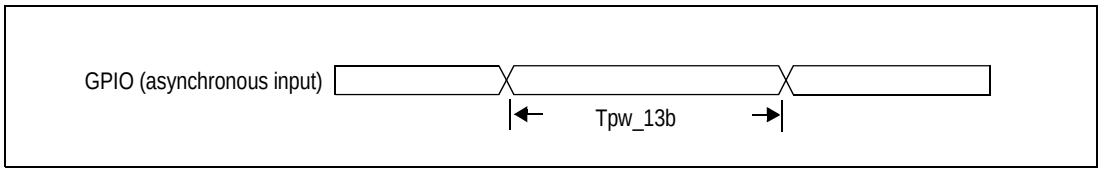



**Figure 15 GPIO AC Timing Waveform**

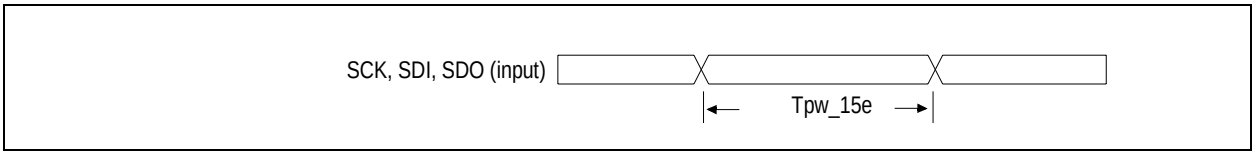



**Figure 18 SPI AC Timing Waveform — Bit I/O Mode**

| Signal | Symbol | Reference Edge | 266MHz | | 300MHz | | 350MHz | | 400MHz | | Unit | Condi-tions | Timing Diagram Reference |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | | | |
| **EJTAG and JTAG** | | | | | | | | | | | | | |
| JTAG_TCK | Tper_16a | none | 25.0 | 50.0 | 25.0 | 50.0 | 25.0 | 50.0 | 25.0 | 50.0 | ns | | See Figure 19. |
| | Thigh_16a, Tlow_16a | | 10.0 | 25.0 | 10.0 | 25.0 | 10.0 | 25.0 | 10.0 | 25.0 | ns | | |
| JTAG_TMS[1], JTAG_TDI | Tsu_16b | JTAG_TCK rising | 2.4 | — | 2.4 | — | 2.4 | — | 2.4 | — | ns | | |
| | Thld_16b | | 1.0 | — | 1.0 | — | 1.0 | — | 1.0 | — | ns | | |
| JTAG_TDO | Tdo_16c | JTAG_TCK fall-ing | — | 11.3 | — | 11.3 | — | 11.3 | — | 11.3 | ns | | |
| | Tdz_16c[2] | | — | 11.3 | — | 11.3 | — | 11.3 | — | 11.3 | ns | | |
| JTAG_TRST_N | Tpw_16d[2] | none | 25.0 | — | 25.0 | — | 25.0 | — | 25.0 | — | ns | | |
| EJTAG_TMS[1] | Tsu_16e | JTAG_TCK rising | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | ns | | |
| | Thld_6e | | 1.0 | — | 1.0 | — | 1.0 | — | 1.0 | — | ns | | |

**Table 14 JTAG AC Timing Characteristics**

1. The JTAG specification, IEEE 1149.1, recommends that both JTAG_TMS and EJTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when either JTAG_TMS or EJTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

# Power Consumption

| Parameter | | 266MHz | | 300MHz | | 350MHz | | 400MHz | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | **Typ.** | **Max.** | **Typ.** | **Max.** | **Typ.** | **Max.** | **Typ.** | **Max.** | | |
| $I_{CC}$ I/O | | 215 | 270 | 220 | 275 | 225 | 280 | 230 | 285 | mA | $C_L$ = 35 pF<br>$T_{ambient}$ = 25°C<br>Max. values use the maximum voltages listed in Table 15. Typical values use the typical voltages listed in that table.<br>Note: For additional information, see Power Considerations for IDT Processors on the IDT web site www.idt.com. |
| $I_{CC}$ SI/O (DDR) | | 70 | 85 | 75 | 90 | 85 | 100 | 95 | 110 | mA | |
| $I_{CC}$ Core, $I_{CC}$ PLL | Normal mode | 325 | 510 | 350 | 550 | 400 | 610 | 450 | 670 | mA | |
| | Standby mode[1] | 220 | — | 240 | — | 260 | — | 280 | — | mA | |
| Power Dissipation | Normal mode | 1.27 | 1.82 | 1.36 | 1.90 | 1.45 | 2.02 | 1.54 | 2.15 | W | |
| | Standby mode[1] | 0.73 | — | 0.78 | — | 0.84 | — | 0.90 | — | W | |

**Table 17 RC32434 Power Consumption**

1. The RC32434 enter Standby mode by executing WAIT instructions. Minimal I/O switching is assumed. On-chip logic outside the CPU core continues to function.

# Power Curve

The following graph contains a power curve that shows power consumption at various core frequencies.

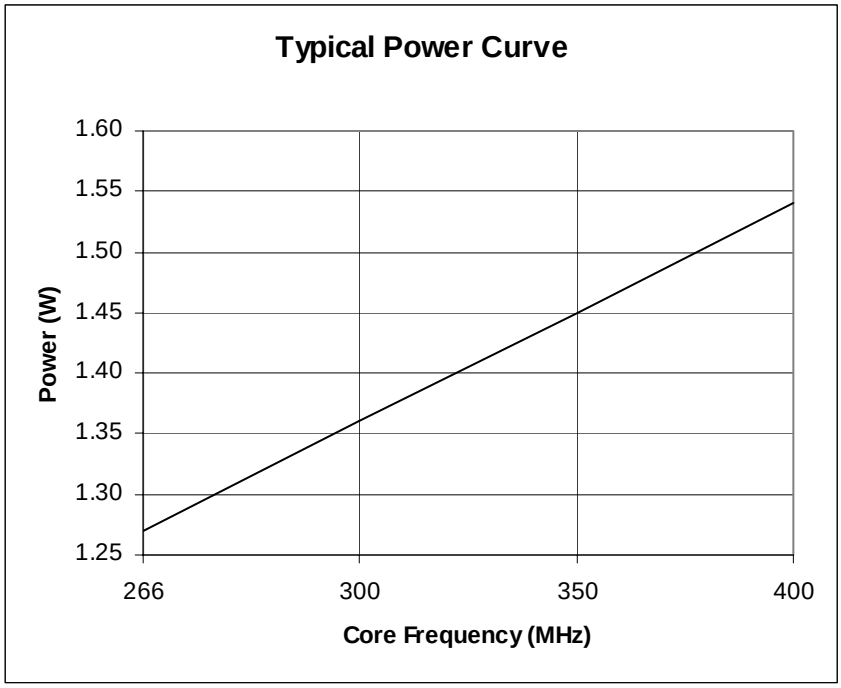



**Figure 22 RC32434 Typical Power Usage**

# Absolute Maximum Ratings

| Symbol | Parameter | Min[1] | Max[1] | Unit |
|---|---|---|---|---|
| $V_{CC}$I/O | I/O supply except for SSTL_2[2] | -0.6 | 4.0 | V |
| $V_{CC}$SI/O (DDR) | I/O supply for SSTL_2[2] | -0.6 | 4.0 | V |
| $V_{CC}$Core | Core Supply Voltage | -0.6 | 2.0 | V |
| $V_{CC}$PLL | PLL supply (digital) | -0.6 | 2.0 | V |
| $V_{CC}$APLL | PLL supply (analog) | -0.6 | 4.0 | V |
| VinI/O | I/O Input Voltage except for SSTL_2 | -0.6 | $V_{cc}$I/O+ 0.5 | V |
| VinSI/O | I/O Input Voltage for SSTL_2 | -0.6 | $V_{cc}$SI/O+ 0.5 | V |
| $T_a$ Industrial | Ambient Operating Temperature | -40 | +85 | °C |
| $T_a$ Commercial | Ambient Operating Temperature | 0 | +70 | °C |
| $T_s$ | Storage Temperature | -40 | +125 | °C |

**Table 19 Absolute Maximum Ratings**

1. Functional and tested operating conditions are given in Table 15. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. SSTL_2 I/Os are used to connect to DDR SDRAM.

# Package Pin-out — 256-BGA Signal Pinout for the RC32434

The following table lists the pin numbers, signal names, and number of alternate functions for the RC32434 device. Signal names ending with an "_n" or "n" are active when low.

| Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 | RWN | | E1 | MIIRXD[3] | | J1 | GPIO[3] | 1 | N1 | PCIAD[29] | |
| A2 | OEN | | E2 | MIIRXD[2] | | J2 | JTAG_TCK | | N2 | PCIAD[28] | |
| A3 | CSN[2] | | E3 | MIITXD[0] | | J3 | GPIO[2] | 1 | N3 | PCIAD[30] | |
| A4 | CSN[0] | | E4 | MIITXD[1] | | J4 | EJTAG_TMS | | N4 | PCIAD[18] | |
| A5 | MADDR[10] | | E5 | $V_{cc}$ I/0 | | J5 | $V_{cc}$ CORE | | N5 | PCIREQN[1] | |
| A6 | MDATA[6] | | E6 | $V_{cc}$ I/0 | | J6 | $V_{ss}$ | | N6 | PCIREQN[2] | |
| A7 | GPIO[7] | 1 | E7 | $V_{cc}$ I/0 | | J7 | $V_{ss}$ | | N7 | PCIIRDYN | |
| A8 | GPIO[4] | 1 | E8 | $V_{cc}$ CORE | | J8 | $V_{ss}$ | | N8 | PCILOCKN | |
| A9 | MADDR[16] | | E9 | $V_{cc}$ CORE | | J9 | $V_{ss}$ | | N9 | PCIPERRN | |
| A10 | MADDR[13] | | E10 | $V_{cc}$ I/0 | | J10 | $V_{ss}$ | | N10 | PCIAD[15] | |
| A11 | $V_{ss}$ PLL | | E11 | $V_{cc}$ DDR | | J11 | $V_{cc}$ CORE | | N11 | PCIAD[11] | |
| A12 | JTAG_TDI | | E12 | $V_{cc}$ DDR | | J12 | $V_{cc}$ CORE | | N12 | PCICBEN[0] | |
| A13 | MADDR[9] | | E13 | DDRDATA[6] | | J13 | DDRCKN | | N13 | DDRADDR[5] | |
| A14 | MADDR[7] | | E14 | DDRDATA[5] | | J14 | DDRVREF | | N14 | DDRADDR[4] | |
| A15 | MADDR[5] | | E15 | DDRADDR[13] | | J15 | DDRCKP | | N15 | DDRADDR[3] | |
| A16 | MADDR[2] | | E16 | DDRDATA[4] | | J16 | DDRDQS[0] | | N16 | DDRBA[0] | |
| B1 | BOEN | | F1 | MIITXD[2] | | K1 | JTG_TDO | | P1 | PCIAD[27] | |
| B2 | RSTN | | F2 | MIIRXCLK | | K2 | SCK | | P2 | PCIAD[26] | |
| B3 | CSN[3] | | F3 | MIITXD[3] | | K3 | Reserved | | P3 | GPIO[10] | 1 |
| B4 | CSN[1] | | F4 | MIITXENP | | K4 | SDO | | P4 | PCIAD[20] | |
| B5 | MADDR[11] | | F5 | $V_{cc}$ I/0 | | K5 | $V_{cc}$ I/0 | | P5 | PCIREQN[3] | |
| B6 | MDATA[1] | | F6 | $V_{ss}$ | | K6 | $V_{cc}$ I/0 | | P6 | PCIREQN[0] | |
| B7 | MDATA[4] | | F7 | $V_{ss}$ | | K7 | $V_{ss}$ | | P7 | PCIFRAMEN | |
| B8 | GPIO[5] | 1 | F8 | $V_{ss}$ | | K8 | $V_{ss}$ | | P8 | PCISTOPN | |
| B9 | MADDR[17] | | F9 | $V_{cc}$ CORE | | K9 | $V_{ss}$ | | P9 | PCISERRN | |
| B10 | MADDR[12] | | F10 | $V_{ss}$ | | K10 | $V_{ss}$ | | P10 | PCIAD[14] | |
| B11 | $V_{cc}$ PLL | | F11 | $V_{ss}$ | | K11 | $V_{ss}$ | | P11 | PCIAD[10] | |
| B12 | $V_{ss}$ APLL | | F12 | $V_{cc}$ DDR | | K12 | $V_{cc}$ DDR | | P12 | PCIAD[7] | |
| B13 | MADDR[8] | | F13 | DDRDATA[9] | | K13 | DDRCKE | | P13 | PCIAD[4] | |
| B14 | MADDR[6] | | F14 | DDRDATA[8] | | K14 | DDRADDR[11] | | P14 | DDRADDR[0] | |
| B15 | MADDR[3] | | F15 | DDRDM[0] | | K15 | DDRADDR[10] | | P15 | DDRADDR[2] | |
| B16 | MADDR[1] | | F16 | DDRDATA[7] | | K16 | DDRADDR[12] | | P16 | DDRCSN | |
| C1 | EXTCLK | | G1 | MIIRXDV | | L1 | SDA | | R1 | PCIAD[25] | |

**Table 20 RC32434 Pinout (Part 1 of 2)**

| Signal Name | I/O Type | Location | Signal Category |
|---|---|---|---|
| DDRADDR[0] | O | P14 | DDR Bus |
| DDRADDR[1] | O | R16 | |
| DDRADDR[2] | O | P15 | |
| DDRADDR[3] | O | N15 | |
| DDRADDR[4] | O | N14 | |
| DDRADDR[5] | O | N13 | |
| DDRADDR[6] | O | M15 | |
| DDRADDR[7] | O | M16 | |
| DDRADDR[8] | O | L16 | |
| DDRADDR[9] | O | L13 | |
| DDRADDR[10] | O | K15 | |
| DDRADDR[11] | O | K14 | |
| DDRADDR[12] | O | K16 | |
| DDRADDR[13] | O | E15 | |
| DDRBA[0] | O | N16 | |
| DDRBA[1] | O | M14 | |
| DDRCASN | O | L15 | |
| DDRCKE | O | K13 | |
| DDRCKN | O | J13 | |
| DDRCKP | O | J15 | |
| DDRCSN | O | P16 | |
| DDRDATA[0] | I/O | C16 | |
| DDRDATA[1] | I/O | D16 | |
| DDRDATA[2] | I/O | D14 | |
| DDRDATA[3] | I/O | D15 | |
| DDRDATA[4] | I/O | E16 | |
| DDRDATA[5] | I/O | E14 | |
| DDRDATA[6] | I/O | E13 | |
| DDRDATA[7] | I/O | F16 | |
| DDRDATA[8] | I/O | F14 | |
| DDRDATA[9] | I/O | F13 | |
| DDRDATA[10] | I/O | G15 | |
| DDRDATA[11] | I/O | G16 | |
| DDRDATA[12] | I/O | H15 | |
| DDRDATA[13] | I/O | H16 | |
| DDRDATA[14] | I/O | H14 | |

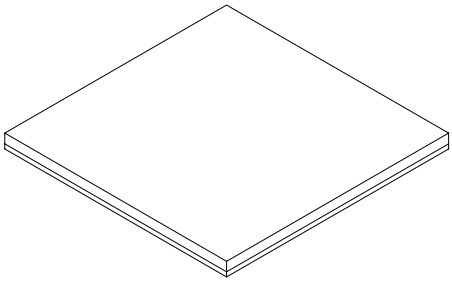
**Table 24 RC32434 Alphabetical Signal List (Part 2 of 7)**

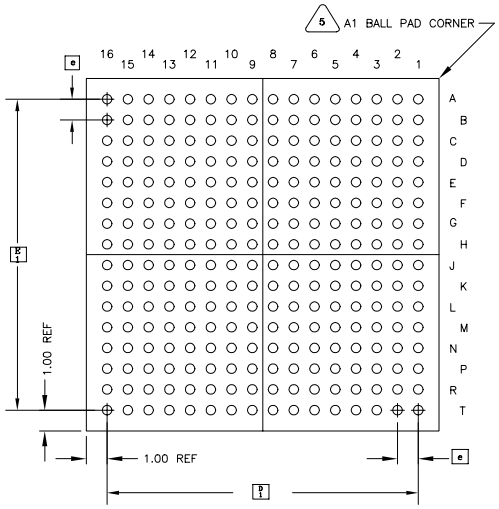
| Signal Name | I/O Type | Location | Signal Category |
|---|---|---|---|
| PCIAD[17] | I/O | R5 | PCI Bus Interface |
| PCIAD[18] | I/O | N4 | |
| PCIAD[19] | I/O | T4 | |
| PCIAD[20] | I/O | P4 | |
| PCIAD[21] | I/O | R4 | |
| PCIAD[22] | I/O | T3 | |
| PCIAD[23] | I/O | R3 | |
| PCIAD[24] | I/O | T1 | |
| PCIAD[25] | I/O | R1 | |
| PCIAD[26] | I/O | P2 | |
| PCIAD[27] | I/O | P1 | |
| PCIAD[28] | I/O | N2 | |
| PCIAD[29] | I/O | N1 | |
| PCIAD[30] | I/O | N3 | |
| PCIAD[31] | I/O | M2 | |
| PCIBEN[0] | I/O | N12 | |
| PCIBEN[1] | I/O | R9 | |
| PCIBEN[2] | I/O | R7 | |
| PCIBEN[3] | I/O | R2 | |
| PCICLK | I | T6 | |
| PCIDEVSELN | I/O | T8 | |
| PCIFRAMEN | I/O | P7 | |
| PCIGNTN[0] | I/O | T7 | |
| PCIGNTN[1] | I/O | T15 | |
| PCIGNTN[2] | I/O | R15 | |
| PCIGNTN[3] | I/O | T16 | |
| PCIIRDYN | I/O | N7 | |
| PCILOCKN | I/O | N8 | |
| PCIPAR | I/O | T9 | |
| PCIPERRN | I/O | N9 | |
| PCIREQN[0] | I/O | P6 | |
| PCIREQN[1] | I/O | N5 | |
| PCIREQN[2] | I/O | N6 | |
| PCIREQN[3] | I/O | P5 | |
| PCIRSTN | I/O | R6 | |
| PCISERRN | I/O | P9 | |

**Table 24 RC32434 Alphabetical Signal List (Part 6 of 7)**

## RC32434 Package Drawing — Page Two

| REVISIONS | | | | |
|---|---|---|---|---|
| DCN | REV | DESCRIPTION | DATE | APPROVED |
| | 00 | INITIAL RELEASE | 06/09/00 | D.G |
| | 01 | JEDEC VARIATION MODIFICATION | 07/11/00 | D.G |
| | 02 | UPDATE MAX. THICKNESS A | 10/02/02 | |






BOTTOM VIEW
256 SOLDER BALLS

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "MD" IS THE MAXIMUM SOLDER BALL MATRIX SIZE IN THE "D" DIRECTION.
   "ME" IS THE MAXIMUM SOLDER BALL MATRIX SIZE IN THE "E" DIRECTION.
4. "N" IS THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.
6. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. "A1" ID CORNER MUST BE IDENTIFIED. IDENTIFICATION MAY BE BY MEANS OF CHAMFER, METALLIZED OR INK MARK, INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY.
8. ALL DIMENSIONS ARE IN MILLIMETERS.
9. THIS DRAWING CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–192 VARIATION AAF–1
   EXCEPTIONS:
   b MIN=0.41 NOM=0.46 MAX=0.51

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS
DECIMAL: X.X ±0.10, X.XX ±0.05, X.XXX ±0.00
ANGULAR: ±1°

| APPROVALS | DATE |
|---|---|
| DRAWN BX | 06/09/00 |
| CHECKED | |

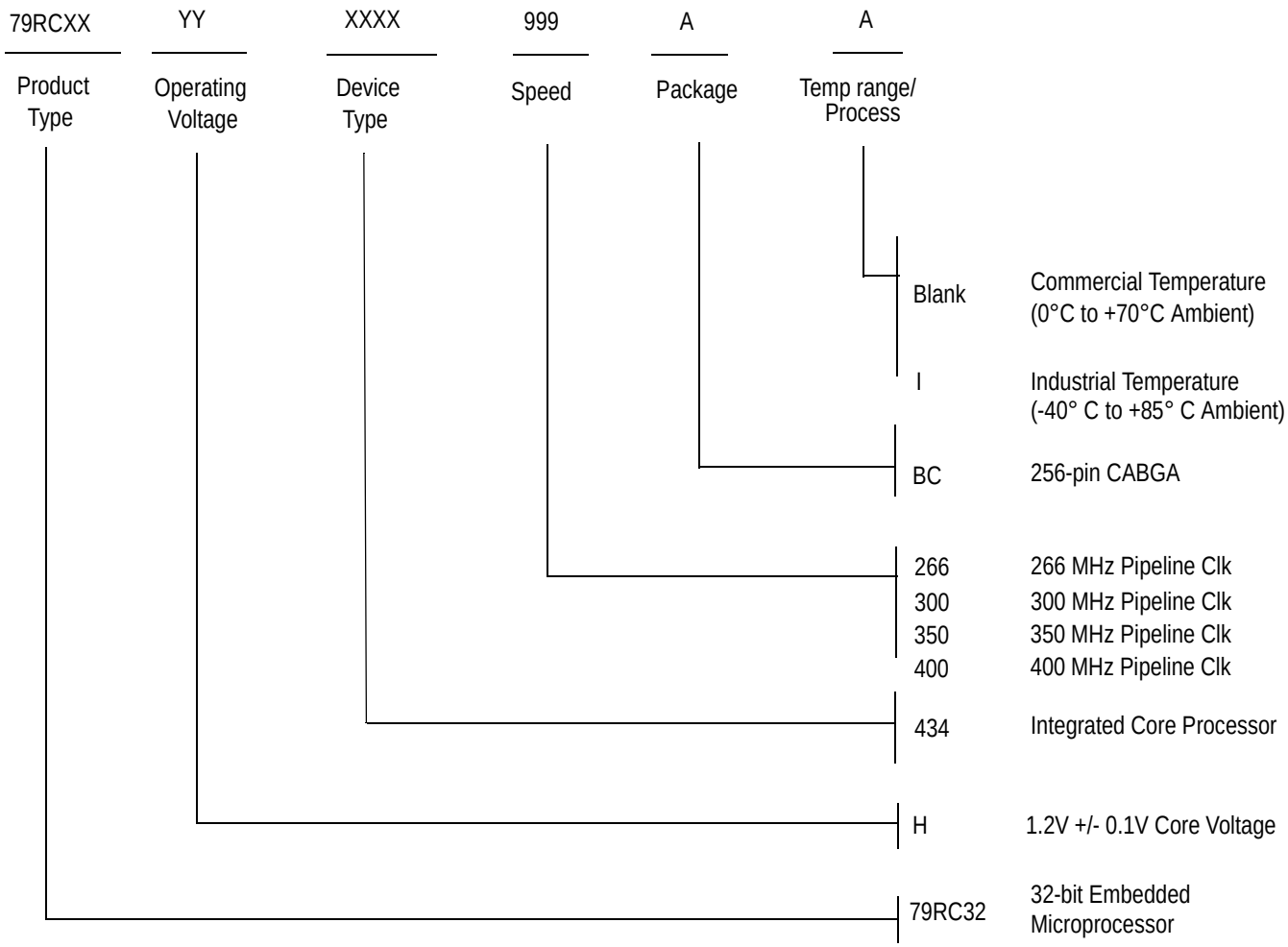
Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
(408) 727–6116 FAX (408) 492–8074

BC256 PACKAGE OUTLINE
17.0 X 17.0 mm BODY CABGA

| DRAWING No. | SIZE | SCALE | REV |
|---|---|---|---|
| PSC–4093 | C | N/A | 02 |

DO NOT SCALE DRAWING — SHEET 2 OF 2

# Ordering Information




## Valid Combinations

| | |
|---|---|
| 79RC32H434 - 266BC, 300BC, 350BC, 400BC | 256-pin CABGA package, Commercial Temperature |
| 79RC32H434 - 266BCI, 300BCI, 350BCI | 256-pin CABGA package, Industrial Temperature |

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