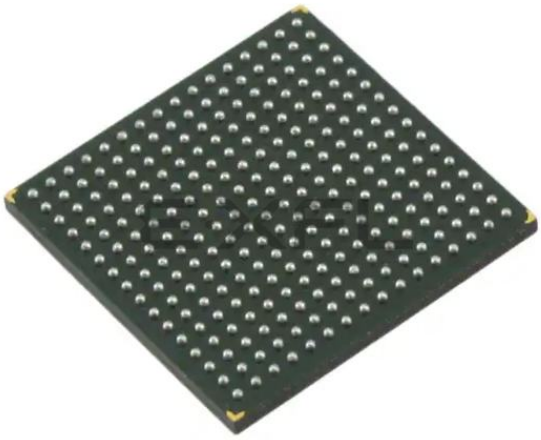
Renesas Electronics America Inc - 79RC32H434-350BCG Datasheet



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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS32
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	350MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	256-LBGA
Supplier Device Package	256-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/79rc32h434-350bcg

Pin Description Table

The following table lists the functions of the pins provided on the RC32434. Some of the functions listed may be multiplexed onto the same pin.

The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
Memory and Peripheral Bus		
BDIRN	O	**External Buffer Direction.** Controls the direction of the external data bus buffer for the memory and peripheral bus. If the RC32434 memory and peripheral bus is connected to the A side of a transceiver, such as an IDT74FCT245, then this pin may be directly connected to the direction control (e.g., BDIR) pin of the transceiver.
BOEN	O	**External Buffer Enable.** This signal provides an output enable control for an external buffer on the memory and peripheral data bus.
WEN	O	**Write Enables.** This signal is the memory and peripheral bus write enable signal.
CSN[3:0]	O	**Chip Selects.** These signals are used to select an external device on the memory and peripheral bus.
MADDR[21:0]	O	**Address Bus.** 22-bit memory and peripheral bus address bus. MADDR[25:22] are available as GPIO alternate functions.
MDATA[7:0]	I/O	**Data Bus.** 8-bit memory and peripheral data bus. During a cold reset, these pins function as inputs that are used to load the boot configuration vector.
OEN	O	**Output Enable.** This signal is asserted when data should be driven by an external device on the memory and peripheral bus.
RWN	O	**Read Write.** This signal indicates whether the transaction on the memory and peripheral bus is a read transaction or a write transaction. A high level indicates a read from an external device. A low level indicates a write to an external device.
WAITACKN	I	**Wait or Transfer Acknowledge.** When configured as wait, this signal is asserted during a memory and peripheral bus transaction to extend the bus cycle. When configured as a transfer acknowledge, this signal is asserted during a transaction to signal the completion of the transaction.
DDR Bus		
DDRADDR[13:0]	O	**DDR Address Bus.** 14-bit multiplexed DDR address bus. This bus is used to transfer the addresses to the DDR devices.
DDRBA[1:0]	O	**DDR Bank Address.** These signals are used to transfer the bank address to the DDRs.
DDRCASN	O	**DDR Column Address Strobe.** This signal is asserted during DDR transactions.
DDRCKE	O	**DDR Clock Enable.** The DDR clock enable signal is asserted during normal DDR operation. This signal is negated following a cold reset or during a power down operation.
DDRCKN	O	**DDR Negative DDR clock.** This signal is the negative clock of the differential DDR clock pair.

Table 1 Pin Description (Part 1 of 6)

Signal	Type	Name/Description
PCILOCKN	I/O	**PCI Lock**. This signal is asserted by an external bus master to indicate that an exclusive operation is occurring.
PCIPAR	I/O	**PCI Parity**. Even parity of the PCIAD[31:0] bus. Driven by the bus master during address and write Data phases. Driven by the bus target during the read data phase.
PCIPERRN	I/O	**PCI Parity Error**. If a parity error is detected, this signal is asserted by the receiving bus agent 2 clocks after the data is received.
PCIREQN[3:0]	I/O	**PCI Bus Request.** **In PCI host mode with internal arbiter:** These signals are inputs whose assertion indicates to the internal RC32434 arbiter that an agent desires ownership of the PCI bus. **In PCI host mode with external arbiter:** PCIREQN[0]: asserted by the RC32434 to request ownership of the PCI bus. PCIREQN[3:1]: unused and driven high. **In PCI satellite mode:** PCIREQN[0]: this signal is asserted by the RC32434 to request use of the PCI bus. PCIREQN[1]: function changes to PCIIDSEL and is used as a chip select during configuration read and write transactions. PCIREQN[3:2]: unused and driven high.
PCIRSTN	I/O	**PCI Reset**. In host mode, this signal is asserted by the RC32434 to generate a PCI reset. In satellite mode, assertion of this signal initiates a warm reset.
PCISERRN	I/O	**PCI System Error**. This signal is driven by an agent to indicate an address parity error, data parity error during a special cycle command, or any other system error. Requires an external pull-up.
PCISTOPN	I/O	**PCI Stop**. Driven by the bus target to terminate the current bus transaction. For example, to indicate a retry.
PCITRDYN	I/O	**PCI Target Ready**. Driven by the bus target to indicate that the current data can complete.
General Purpose Input/Output		
GPIO[0]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0SOUT Alternate function: UART channel 0 serial output.
GPIO[1]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0SINP Alternate function: UART channel 0 serial input.
GPIO[2]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0RTSN Alternate function: UART channel 0 request to send.
GPIO[3]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0CTSN Alternate function: UART channel 0 clear to send.

Table 1 Pin Description (Part 3 of 6)

Signal	Type	Name/Description
GPIO[4]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[22] Alternate function: Memory and peripheral bus address.
GPIO[5]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[23] Alternate function: Memory and peripheral bus address.
GPIO[6]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[24] Alternate function: Memory and peripheral bus address. The value of this pin may be used as a counter timer clock input (see Counter Timer Clock Select Register in Chapter 14, Counter/Timers, of the RC32434 User Manual).
GPIO[7]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[25] Alternate function: Memory and peripheral bus address. The value of this pin may be used as a counter timer clock input (see Counter Timer Clock Select Register in Chapter 14, Counter/Timers, of the RC32434 User Manual).
GPIO[8]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: CPU Alternate function: CPU or DMA debug output pin.
GPIO[9]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIREQN[4] Alternate function: PCI Request 4.
GPIO[10]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIGNTN[4] Alternate function: PCI Grant 4.
GPIO[11]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIREQN[5] Alternate function: PCI Request 5.
GPIO[12]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIGNTN[5] Alternate function: PCI Grant 5.
GPIO[13]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIMUINTN Alternate function: PCI Messaging unit interrupt output.
SPI Interface		
SCK	I/O	**Serial Clock**. This signal is used as the serial clock output. This pin may be used as a bit input/output port.

Table 1 Pin Description (Part 4 of 6)

Signal	Type	Name/Description
EJTAG_TMS	I	**EJTAG Mode**. The value on this signal controls the test mode select of the EJTAG Controller. When using the JTAG boundary scan, this pin should be left disconnected (since there is an internal pull-up) or driven high.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic, JTAG TAP Controller, and the EJTAG Debug TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board 3) clock JTAG_TCK while holding EJTAG_TMS and/or JTAG_TMS high.
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic, JTAG Controller, or the EJTAG Controller. JTAG_TCK is independent of the system and the processor clock with a nominal 50% duty cycle.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic, JTAG Controller, or the EJTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic, JTAG Controller, or the EJTAG Controller.
System		
CLK	I	**Master Clock.** This is the master clock input. The processor frequency is a multiple of this clock frequency. This clock is used as the system clock for all memory and peripheral bus operations.
EXTBCV	I	**Load External Boot Configuration Vector.** When this pin is asserted (i.e., high) the boot configuration vector is loaded from an externally supplied value during a cold reset.
EXTCLK	O	**External Clock.** This clock is used for all memory and peripheral bus operations.
COLDRSTN	I	**Cold Reset.** The assertion of this signal initiates a cold reset. This causes the processor state to be initialized, boot configuration to be loaded, and the internal PLL to lock onto the master clock (CLK).
RSTN	I/O	**Reset.** The assertion of this bidirectional signal initiates a warm reset. This signal is asserted by the RC32434 during a warm reset.

Table 1 Pin Description (Part 6 of 6)

Pin Characteristics

Note: Some input pads of the RC32434 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs (such as WAITACKN) which, if left floating, could adversely affect the RC32434's operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes[1]
Ethernet Interfaces	MIICL	I	LVTTL	STI	pull-down	
	MIICRS	I	LVTTL	STI	pull-down	
	MIIRXCLK	I	LVTTL	STI	pull-up	
	MIIRXD[3:0]	I	LVTTL	STI	pull-up	
	MIIRXDV	I	LVTTL	STI	pull-down	
	MIIRXER	I	LVTTL	STI	pull-down	
	MIITXCLK	I	LVTTL	STI	pull-up	
	MIITXD[3:0]	O	LVTTL	Low Drive		
	MIITXENP	O	LVTTL	Low Drive		
	MIITXER	O	LVTTL	Low Drive		
	MIIMDC	O	LVTTL	Low Drive		
	MIIMDIO	I/O	LVTTL	Low Drive	pull-up	
EJTAG / JTAG	JTAG_TMS	I	LVTTL	STI	pull-up	
	EJTAG_TMS	I	LVTTL	STI	pull-up	
	JTAG_TRST_N	I	LVTTL	STI	pull-up	
	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDO	O	LVTTL	Low Drive		
	JTAG_TDI	I	LVTTL	STI	pull-up	
System	CLK	I	LVTTL	STI		
	EXTBCV	I	LVTTL	STI	pull-down	
	EXTCLK	O	LVTTL	High Drive		
	COLDRSTN	I	LVTTL	STI		
	RSTN	I/O	LVTTL	Low Drive / STI	pull-up	pull-up on board

Table 2 Pin Characteristics (Part 2 of 2)

1. External pull-up required in most system applications. Some applications may require additional pull-ups not identified in this table.

2. Use a 2.2K pull-up resistor for I2C pins.

Boot Configuration Vector

The encoding of the boot configuration vector is described in Table 3, and the vector input is illustrated in Figure 4. The value of the boot configuration vector read in by the RC32434 during a cold reset may be determined by reading the Boot Configuration Vector (BCV) Register.

Signal	Name/Description
MADDR[3:0]	**CPU Pipeline Clock Multiplier**. This field specifies the value by which the PLL multiplies the master clock input (CLK) to obtain the processor clock frequency (PCLK). For master clock input frequency constraints, refer to Table 3.2 in the RC32434 User Manual. 0x0 - PLL Bypass 0x1 - Multiply by 3 0x2 - Multiply by 4 0x3 - Multiply by 5 - Reserved 0x4 - Multiply by 5 0x5 - Multiply by 6 - Reserved 0x6 - Multiply by 6 0x7 - Multiply by 8 0x8 - Multiply by 10 0x9 through 0xF - Reserved
MADDR[5:4]	**External Clock Divider**. This field specifies the value by which the IPBus clock (ICLK), which is always 1/2 PCLK, is divided in order to generate the external clock output on the EXTCLK pin. 0x0 - Divide by 1 0x1 - Divide by 2 0x2 - Divide by 4 0x3 - reserved
MADDR[6]	**Endian.** This bit specifies the endianness. 0x0 - little endian 0x1 - big endian
MADDR[7]	**Reset Mode**. This bit specifies the length of time the RSTN signal is driven. 0x0 - Normal reset: RSTN driven for minimum of 4000 clock cycles. If the internal boot configuration vector is selected, the expiration of an 18-bit counter operating at the master clock input (CLK) frequency is used as the PLL stabilization delay. 0x1 - Reserved
MADDR[10:8]	**PCI Mode**. This bit controls the operating mode of the PCI bus interface. The initial value of the EN bit in the PCIC register is determined by the PCI mode. 0x0 - Disabled (EN initial value is zero) 0x1 - PCI satellite mode with PCI target not ready (EN initial value is one) 0x2 - PCI satellite mode with suspended CPU execution (EN initial value is one) 0x3 - PCI host mode with external arbiter (EN initial value is zero) 0x4 - PCI host mode with internal arbiter using fixed priority arbitration algorithm (EN initial value is zero) 0x5 - PCI host mode with internal arbiter using round robin arbitration algorithm (EN initial value is zero) 0x6 - *reserved* 0x7 - *reserved*

Table 3 Boot Configuration Encoding (Part 1 of 2)

Logic Diagram — RC32434

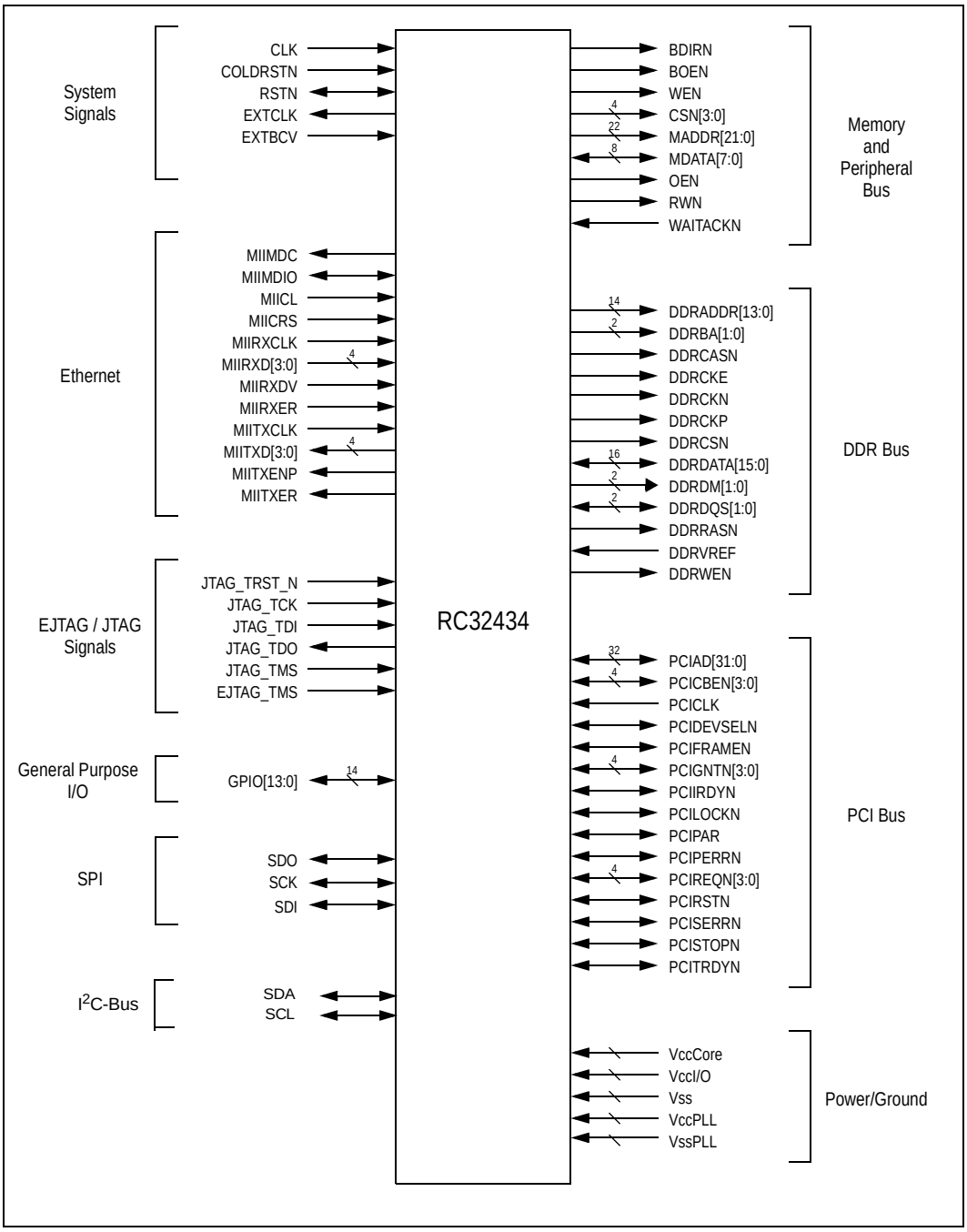


Figure 1 Logic Diagram

AC Timing Characteristics

(Values given below are based on systems running at recommended operating temperatures and supply voltages, shown in Tables 15 and 16.)

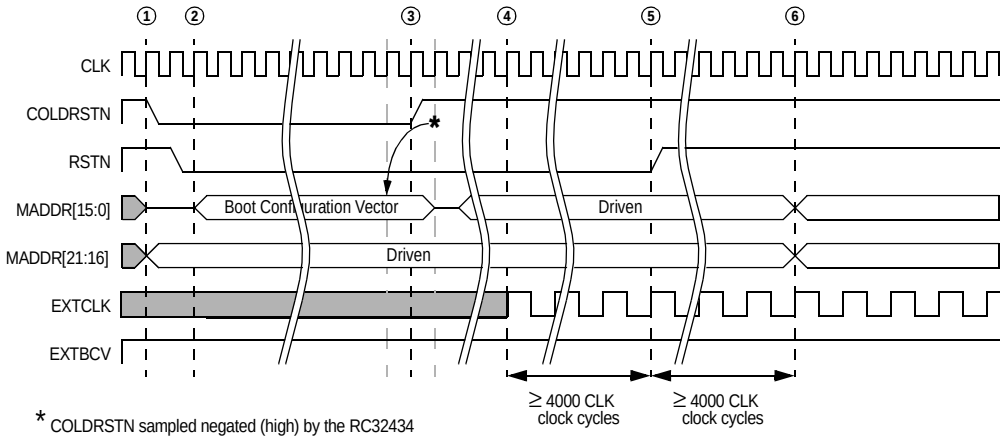
Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Reset													
COLDRSTN[1]	Tpw_6a[2]	none	OSC	—	OSC	—	OSC	—	OSC	—	ms	Cold reset	See Figures 4 and 5.
	Trise_6a	none	—	5.0	—	5.0	—	5.0	—	5.0	ns	Cold reset	
RSTN[3] (input)	Tpw_6b[2]	none	2(CLK)	—	2(CLK)	—	2(CLK)	—	2(CLK)	—	ns	Warm reset	
RSTN[3] (output)	Tdo_6c	COLDRSTN falling	—	15.0	—	15.0	—	15.0	—	15.0	ns	Cold reset	
MADDR[15:0] (boot vector)	Tdz_6d[2]	COLDRSTN falling	—	30.0	—	30.0	—	30.0	—	30.0	ns	Cold reset	
	Tdz_6d[2]	RSTN falling	—	5(CLK)	—	5(CLK)	—	5(CLK)	—	5(CLK)	ns	Warm reset	
	Tzd_6d[2]	RSTN rising	2(CLK)	—	2(CLK)	—	2(CLK)	—	2(CLK)	—	ns	Warm reset	

Table 6 Reset and System AC Timing Characteristics

1. The COLDRSTN minimum pulse width is the oscillator stabilization time (OSC) with V_{cc} stable.

2. The values for this symbol were determined by calculation, not by testing.

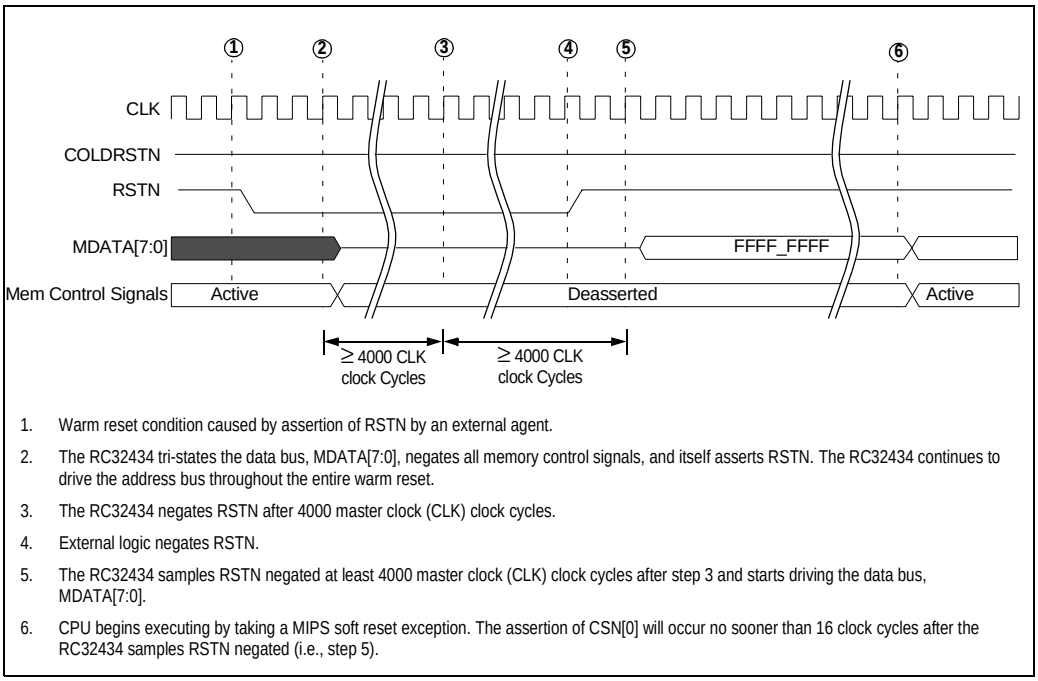
3. RSTN is a bidirectional signal. It is treated as an asynchronous input.



1. EXTBCV is asserted (i.e., pulled-up). COLDRSTN is asserted by external logic. The RC32434 responds by immediately tri-stating the bottom 16-bits of the memory and peripheral address bus (MADDR[15:0]), driving the remaining address bus signals (i.e., MADDR[21:16]), and asserting RSTN. EXTCLK is undefined at this point.
2. External logic drives the boot configuration vector on MADDR[15:0].
3. External logic negates COLDRSTN and tri-states the boot configuration vector on MADDR[15:0]. In response, the RC32434 stops sampling the boot configuration vector and retains the boot configuration vector value seen two clock cycles earlier (i.e., the value on the MADDR[15:0] lines two rising edges of CLK earlier). Within 16 CLK clock cycles after COLDRSTN is sampled negated, the RC32434 begins driving MADDR[15:0].
4. The RC32434 waits for the PLL to stabilize.
5. The RC32434 then begins generating EXTCLK.
6. After at least 4000 CLK clock cycles, the RC32434 tri-states RSTN.
7. At least 4000 CLK clock cycles after negating RSTN, the RC32434 samples RSTN. If RSTN is negated, cold reset has completed and the RC32434 CPU begins executing by taking MIPS reset exception.

Figure 4 COLD Reset Operation with External Boot Configuration Vector AC Timing Waveform

Note: For a diagram showing the COLD Reset Operation with Internal Boot Configuration Vector, see Figure 3.6 in the RC32434 User Reference Manual.



1. Warm reset condition caused by assertion of RSTN by an external agent.
2. The RC32434 tri-states the data bus, MDATA[7:0], negates all memory control signals, and itself asserts RSTN. The RC32434 continues to drive the address bus throughout the entire warm reset.
3. The RC32434 negates RSTN after 4000 master clock (CLK) clock cycles.
4. External logic negates RSTN.
5. The RC32434 samples RSTN negated at least 4000 master clock (CLK) clock cycles after step 3 and starts driving the data bus, MDATA[7:0].
6. CPU begins executing by taking a MIPS soft reset exception. The assertion of CSN[0] will occur no sooner than 16 clock cycles after the RC32434 samples RSTN negated (i.e., step 5).

Figure 5 Externally Initiated Warm Reset AC Timing Waveform

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max		
Memory Bus - DDR Access												
DDRDATA[15:0]	Tskew_7g	DDRDQSx	0	0.9	0	0.8[1]	0	0.7	0.0	0.6	ns	See Figures 6 and 7.
	Tdo_7k[2]		1.2	1.9	1.0	1.7	0.7	1.5	0.5	1.4	ns	
DDRDM[1:0]	Tdo_7l	DDRDQSx	1.2	1.9	1.0	1.7	0.7	1.5	0.5	1.4	ns	
DDRDQS[1:0]	Tdo_7i	DDRCKP	-0.75	0.75	-0.75	0.75	-0.7	0.7	-0.7	0.7	ns	
DDRADDR[13:0], DDRBA[1:0], DDRCASN, DDRCKE, DDRCSN, DDRRASN, DDRWEN	Tdo_7m	DDRCKP	1.0	4.0	1.0	4.3	1.0	4.0	1.0	4.0	ns	

Table 7 DDR SDRAM Timing Characteristics

1. Meets DDR timing requirements for 150MHz clock rate DDR SDRAMs with 300 ps remaining margin to compensate for PCB propagation mismatches, which is adequate to guarantee functional timing, provided the RC32434 DDR layout guidelines are adhered to.

2. Setup times are calculated as applicable clock period - Tdo max. For example, if the DDR is running at 266MHz, it uses a 133MHz input clock. The period for a 133MHz clock is 7.5ns. If the Tdo max value is 4.6ns, the T_{IS} parameter is 7.5ns minus 4.6ns = 2.9ns. The DDR spec for this parameter is 1ns, so there is 1.9ns of slack left over for board propagation. Calculations for T_{DS} are similar, but since this parameter is taken relative to the DDRDQS signals, which are referenced on both edges, the effective period with a 133MHz input clock is only 3.75ns. So, if the max Tdo is 1.9ns, we have 3.75ns minus 1.9ns = 1.85ns for T_{DS}. The DDR data sheet specs a value of 0.5ns for 266MHz, so this leaves 1.35ns slack for board propagation delays.

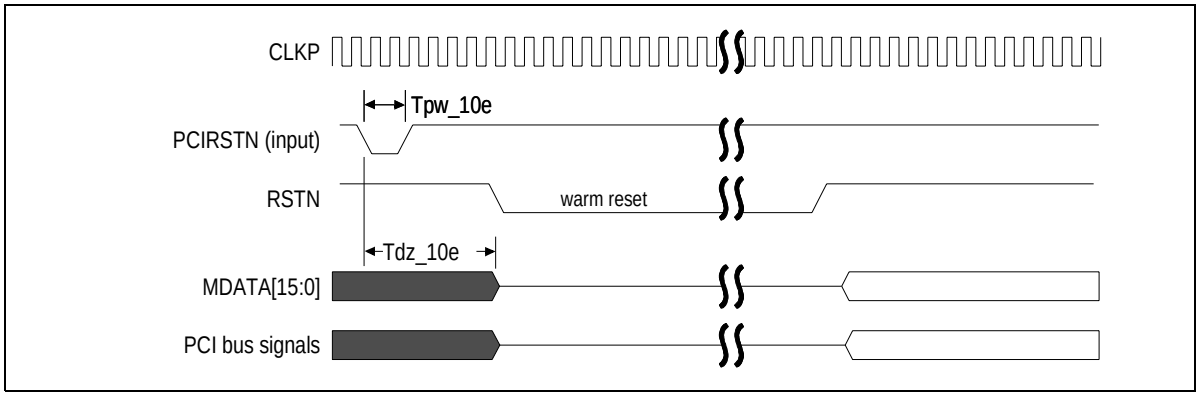


Figure 13 PCI AC Timing Waveform — PCI Reset in Satellite Mode

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
I²C[1]													
SCL	Frequency	none	0	100	0	100	0	100	0	100	kHz	100 KHz	See Figure 14.
	Thigh_12a, Tlow_12a		4.0	—	4.0	—	4.0	—	4.0	—	µs		
	Trise_12a		—	1000	—	1000	—	1000	—	1000	ns		
	Tfall_12a		—	300	—	300	—	300	—	300	ns		
SDA	Tsu_12b	SCL rising	250	—	250	—	250	—	250	—	ns		
	Thld_12b		0	3.45	0	3.45	0	3.45	0	3.45	µs		
	Trise_12b		—	1000	—	1000	—	1000	—	1000	ns		
	Tfall_12b		—	300	—	300	—	300	—	300	ns		
Start or repeated start condition	Tsu_12c	SDA falling	4.7	—	4.7	—	4.7	—	4.7	—	µs		
	Thld_12c		4.0	—	4.0	—	4.0	—	4.0	—	µs		
Stop condition	Tsu_12d	SDA rising	4.0	—	4.0	—	4.0	—	4.0	—	µs		
Bus free time between a stop and start condition	Tdelay_12e		4.7	—	4.7	—	4.7	—	4.7	—	µs		
SCL	Frequency	none	0	400	0	400	0	400	0	400	kHz	400 KHz	
	Thigh_12a, Tlow_12a		0.6	—	0.6	—	0.6	—	0.6	—	µs		
	Trise_12a		—	300	—	300	—	300	—	300	ns		
	Tfall_12a		—	300	—	300	—	300	—	300	ns		
SDA	Tsu_12b	SCL rising	100	—	100	—	100	—	100	—	ns		
	Thld_12b		0	0.9	0	0.9	0	0.9	0	0.9	µs		
	Trise_12b		—	300	—	300	—	300	—	300	ns		
	Tfall_12ba		—	300	—	300	—	300	—	300	ns		

Table 11 I²C AC Timing Characteristics (Part 1 of 2)

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Start or repeated start condition	Tsu_12c	SDA falling	0.6	—	0.6	—	0.6	—	0.6	—	µs	400 KHz	See Figure 14.
	Thld_12c		0.6	—	0.6	—	0.6	—	0.6	—	µs		
Stop condition	Tsu_12d	SDA rising	0.6	—	0.6	—	0.6	—	0.6	—	µs		
Bus free time between a stop and start condition	Tdelay_12e		1.3	—	1.3	—	1.3	—	1.3	—	µs		

Table 11 I²C AC Timing Characteristics (Part 2 of 2)

1. For more information, see the I²C-Bus specification by Philips Semiconductor.

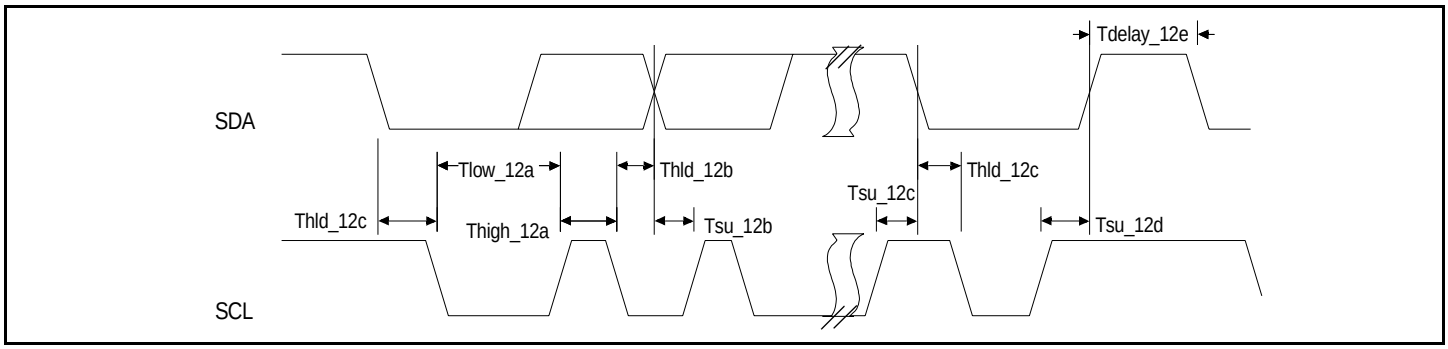


Figure 14 I2C AC Timing Waveform

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
GPIO													
GPIO[13:0]	Tpw_13b[1]	None	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	ns		See Figure 15.

Table 12 GPIO AC Timing Characteristics

1. The values for this symbol were determined by calculation, not by testing.

\

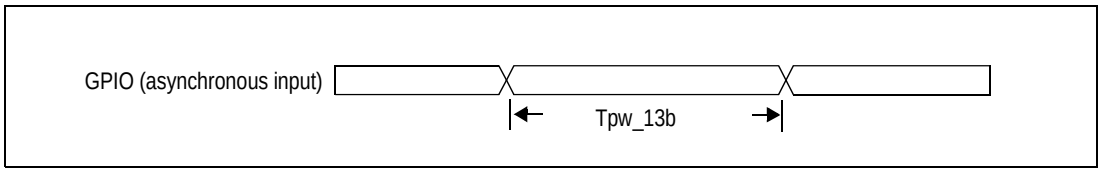


Figure 15 GPIO AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{SS}	Common ground	0	0	0	V
V_{SS}PLL	PLL ground				
V_{CC}I/O	I/O supply except for SSTL_2[1]	3.135	3.3	3.465	V
V_{CC}SI/O (DDR)	I/O supply for SSTL_2[1]	2.375	2.5	2.625	V
V_{CC}PLL	PLL supply (digital)	1.1	1.2	1.3	V
V_{CC}APLL	PLL supply (analog)	3.135	3.3	3.465	V
V_{CC}Core	Internal logic supply	1.1	1.2	1.3	V
DDRVREF[2]	SSTL_2 input reference voltage	0.5(VccSI/O)	0.5(VccSI/O)	0.5(VccSI/O)	V
V_{TT}[3]	SSTL_2 termination voltage	DDRVREF - 0.04	DDRVREF	DDRVREF + 0.04	V

Table 15 RC32434 Operating Voltages

1. SSTL_2 I/Os are used to connect to DDR SDRAM.
2. Peak-to-peak AC noise on DDRVREF may not exceed ± 2% DDRVREF (DC).
3. V_{TT} of the SSTL_2 transmitting device must track DDRVREF of the receiving device.

Recommended Operating Temperatures

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 16 RC32434 Operating Temperatures

Capacitive Load Deration

Refer to the 79RC32434 IBIS Model on the IDT web site (www.idt.com).

Power-on Sequence

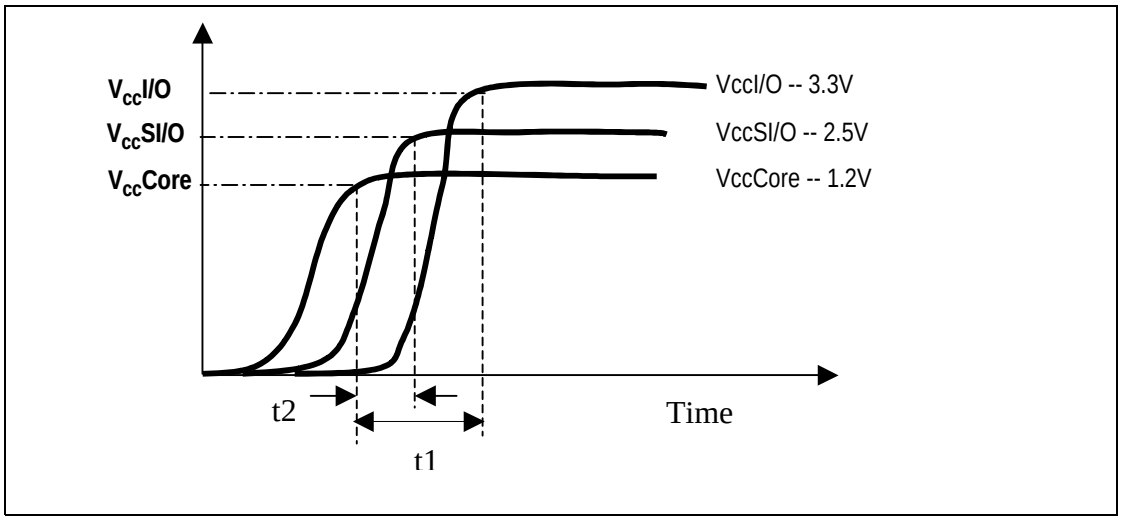
Three power-on sequences are given below. Sequence #1 is recommended because it will prevent I/O conflicts and will also allow the input signals to propagate when the I/O powers are brought up.

Note: The ESD diodes may be damaged if one of the voltages is applied and one of the other voltages is at a ground level.

A. Recommended Sequence

t2 > 0 whenever possible (V_{cc}Core)

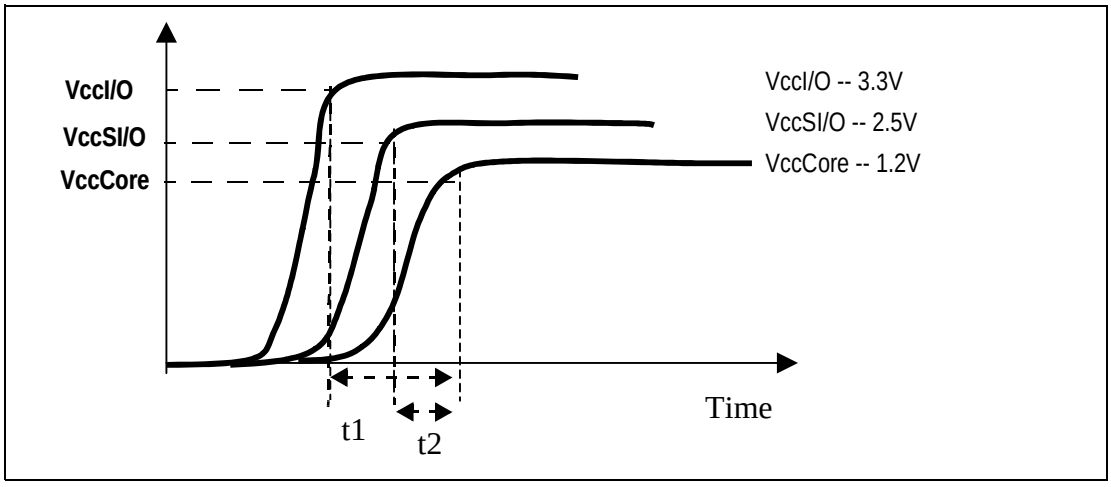
t1 - t2 can be 0 (V_{cc}SI/O followed by V_{cc}I/O)



B. Reverse Voltage Sequence

If sequence A is not feasible, then Sequence B can be used:

t1 <50ms and t2 <50ms to prevent damage.



C. Simultaneous Power-up

VccI/O, VccSI/O, and VccCore can be powered up simultaneously.

Power Consumption

Parameter		266MHz		300MHz		350MHz		400MHz		Unit	Conditions
		Typ.	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**		
I_{CC} I/O		215	270	220	275	225	280	230	285	mA	C_L = 35 pF $T_{ambient}$ = 25°C Max. values use the maximum voltages listed in Table 15. Typical values use the typical voltages listed in that table. Note: For additional information, see Power Considerations for IDT Processors on the IDT web site www.idt.com.
I_{CC} SI/O (DDR)		70	85	75	90	85	100	95	110	mA	
I_{CC} Core, I_{CC} PLL	Normal mode	325	510	350	550	400	610	450	670	mA	
	Standby mode[1]	220	—	240	—	260	—	280	—	mA	
Power Dissipation	Normal mode	1.27	1.82	1.36	1.90	1.45	2.02	1.54	2.15	W	
	Standby mode[1]	0.73	—	0.78	—	0.84	—	0.90	—	W	

Table 17 RC32434 Power Consumption

1. The RC32434 enter Standby mode by executing WAIT instructions. Minimal I/O switching is assumed. On-chip logic outside the CPU core continues to function.

Power Curve

The following graph contains a power curve that shows power consumption at various core frequencies.

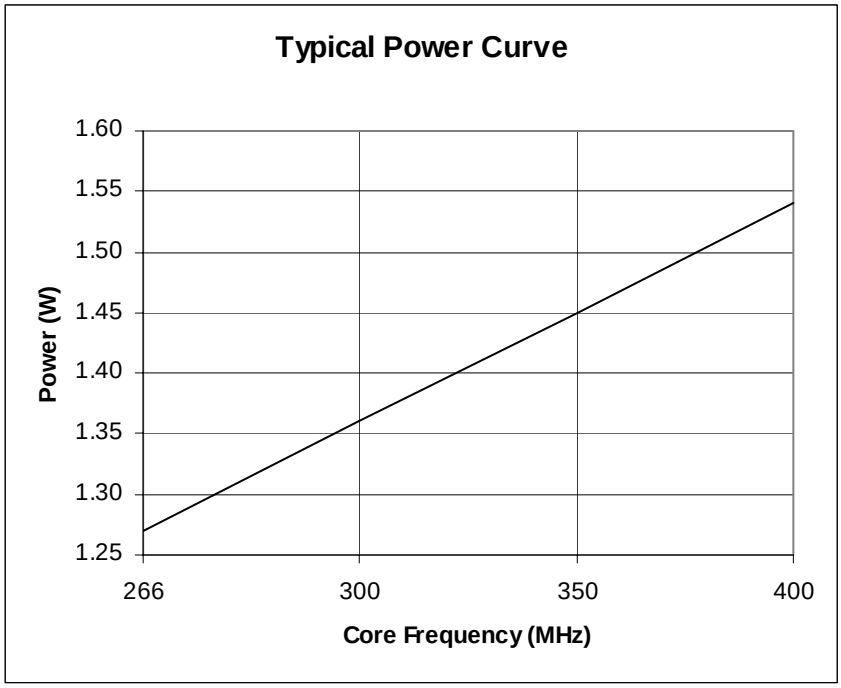


Figure 22 RC32434 Typical Power Usage

RC32434 Alternate Signal Functions

Pin	GPIO	Alternate	Pin	GPIO	Alternate
A7	GPIO[7]	MADDR[25]	J3	GPIO[2]	U0RTSN
A8	GPIO[4]	MADDR[22]	L3	GPIO[8]	CPU
B8	GPIO[5]	MADDR[23]	M1	GPIO[12]	PCIGNTN[5]
C7	GPIO[6]	MADDR[24]	M3	GPIO[11]	PCIREQN[5]
H3	GPIO[0]	U0SOUT	M4	GPIO[9]	PCIREQN[4]
H4	GPIO[1]	U0SINP	P3	GPIO[10]	PCIGNTN[4]
J1	GPIO[3]	U0CTSN	T2	GPIO[13]	PCIMUINTN

Table 21 RC32434 Alternate Signal Functions

RC32434 Power Pins

V_{cc} I/O	V_{cc} DDR	V_{cc} Core	V_{cc} PLL	V_{cc} APLL
E5	E11	E8	B11	C12
E6	E12	E9		
E7	F12	F9		
E10	G12	H5		
F5	K12	H6		
G5	L12	H12		
K5	M11	J5		
K6	M12	J11		
L5		J12		
M5		L8		
M6		M8		
M7		M9		
M10				

Table 22 RC32434 Power Pins

Signal Name	I/O Type	Location	Signal Category
DDRADDR[0]	O	P14	DDR Bus
DDRADDR[1]	O	R16	
DDRADDR[2]	O	P15	
DDRADDR[3]	O	N15	
DDRADDR[4]	O	N14	
DDRADDR[5]	O	N13	
DDRADDR[6]	O	M15	
DDRADDR[7]	O	M16	
DDRADDR[8]	O	L16	
DDRADDR[9]	O	L13	
DDRADDR[10]	O	K15	
DDRADDR[11]	O	K14	
DDRADDR[12]	O	K16	
DDRADDR[13]	O	E15	
DDRBA[0]	O	N16	
DDRBA[1]	O	M14	
DDRCASN	O	L15	
DDRCKE	O	K13	
DDRCKN	O	J13	
DDRCKP	O	J15	
DDRCSN	O	P16	
DDRDATA[0]	I/O	C16	
DDRDATA[1]	I/O	D16	
DDRDATA[2]	I/O	D14	
DDRDATA[3]	I/O	D15	
DDRDATA[4]	I/O	E16	
DDRDATA[5]	I/O	E14	
DDRDATA[6]	I/O	E13	
DDRDATA[7]	I/O	F16	
DDRDATA[8]	I/O	F14	
DDRDATA[9]	I/O	F13	
DDRDATA[10]	I/O	G15	
DDRDATA[11]	I/O	G16	
DDRDATA[12]	I/O	H15	
DDRDATA[13]	I/O	H16	
DDRDATA[14]	I/O	H14	

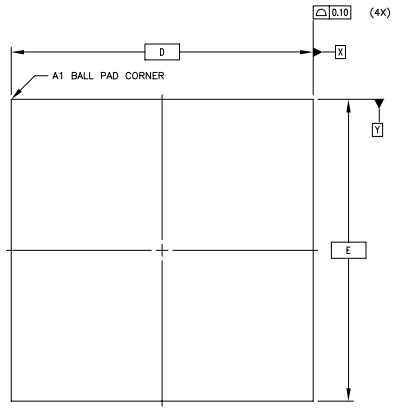
Table 24 RC32434 Alphabetical Signal List (Part 2 of 7)

Signal Name	I/O Type	Location	Signal Category
MADDR[0]	O	C15	Memory and Peripheral Bus
MADDR[1]	O	B16	
MADDR[2]	O	A16	
MADDR[3]	O	B15	
MADDR[4]	O	C14	
MADDR[5]	O	A15	
MADDR[6]	O	B14	
MADDR[7]	O	A14	
MADDR[8]	O	B13	
MADDR[9]	O	A13	
MADDR[10]	O	A5	
MADDR[11]	O	B5	
MADDR[12]	O	B10	
MADDR[13]	O	A10	
MADDR[14]	O	C10	
MADDR[15]	O	D10	
MADDR[16]	O	A9	
MADDR[17]	O	B9	
MADDR[18]	O	C9	
MADDR[19]	O	D9	
MADDR[20]	O	D8	
MADDR[21]	O	C8	
MDATA[0]	I/O	D7	
MDATA[1]	I/O	B6	
MDATA[2]	I/O	D6	
MDATA[3]	I/O	C5	
MDATA[4]	I/O	B7	
MDATA[5]	I/O	C6	
MDATA[6]	I/O	A6	
MDATA[7]	I/O	D5	

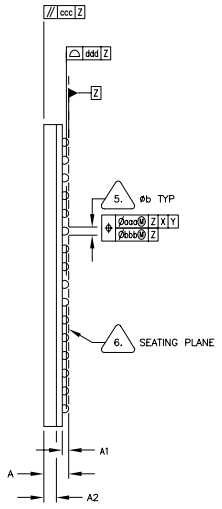
Table 24 RC32434 Alphabetical Signal List (Part 4 of 7)

RC32434 Package Drawing — 256-pin CABGA

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	06/09/00	D.G
	01	JEDEC VARIATION MODIFICATION	07/11/00	D.G
	02	UPDATE MAX. THICKNESS A	10/02/02	



TOP VIEW



SIDE VIEW

SYMBOL	JEDEC VARIATION AAF-1 MIN	NOM	MAX	NOTE
A	1.30	1.40	1.70	
A1	.31	.36	.41	
A2	.65	.70	.75	
D		17.00 BSC		
D1		15.00 BSC		
E		17.00 BSC		
E1		15.00 BSC		
MD		16		3
ME		16		3
N		256		4
e		1.00 BSC		
b	.41	.46	.51	5
aaa	–	–	.15	
bbb	–	–	.08	
ccc	–	–	.10	
ddd	–	–	.12	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS
DECIMAL: XX ±0.10, XXX ±0.05, XXXX ±0.08
ANGULAR: ±1°

APPROVALS	DATE
DRAWN .SX	06/09/00
CHECKED	

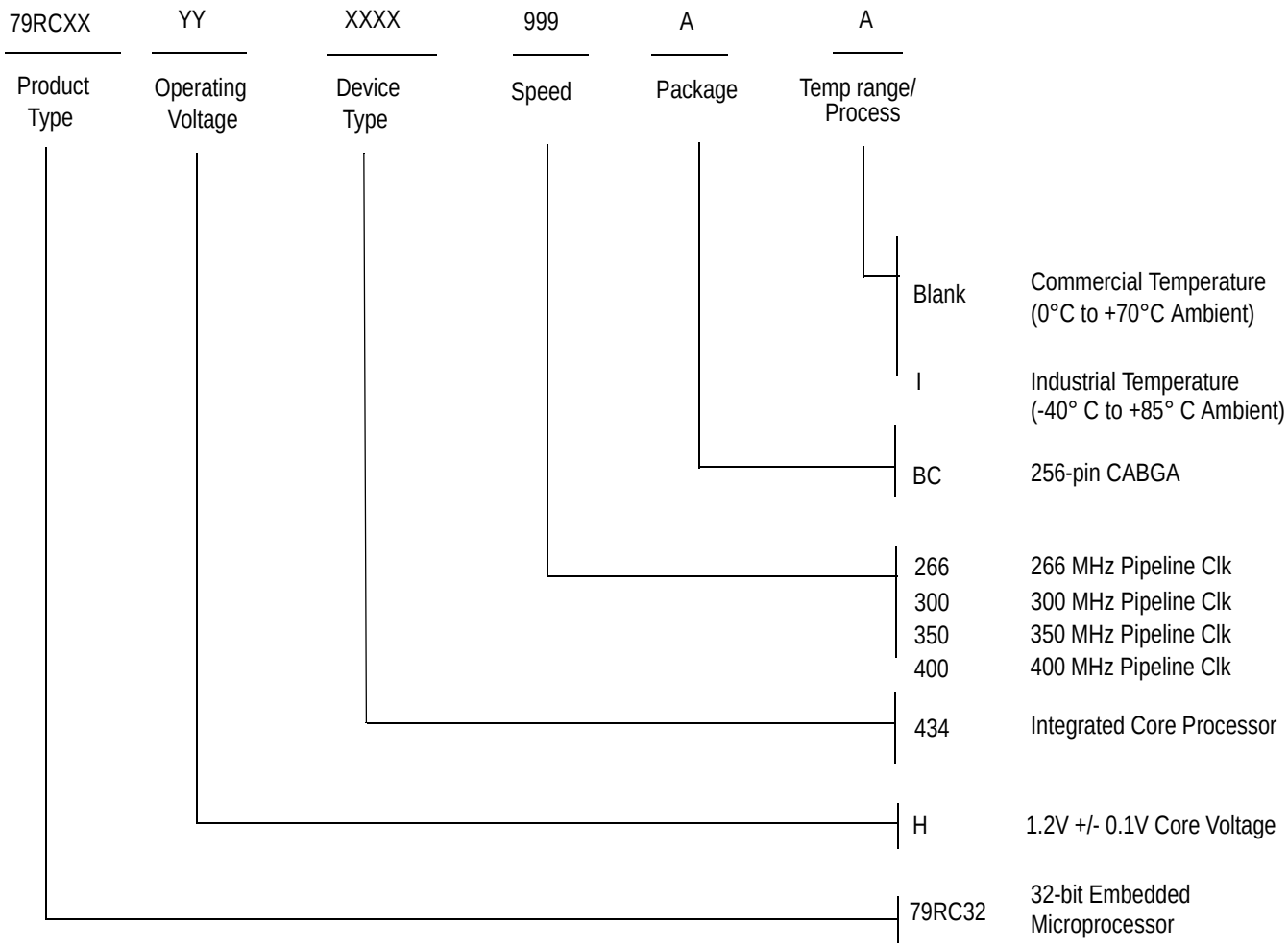
Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
(408) 727-6116 FAX (408) 492-8074

BC256 PACKAGE OUTLINE
17.0 X 17.0 mm BODY CABGA

DRAWING No.	SIZE	SCALE	REV
PSC-4093	C	N/A	02

DO NOT SCALE DRAWING — SHEET 1 OF 2

Ordering Information



Valid Combinations

79RC32H434 - 266BC, 300BC, 350BC, 400BC	256-pin CABGA package, Commercial Temperature
79RC32H434 - 266BCI, 300BCI, 350BCI	256-pin CABGA package, Industrial Temperature

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