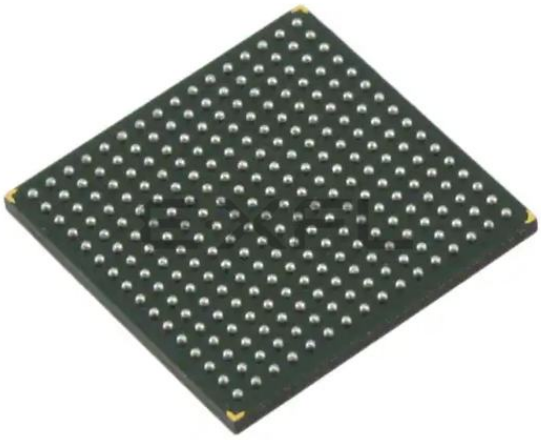
Renesas Electronics America Inc - 79RC32H434-400BC Datasheet



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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS32
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	256-LBGA
Supplier Device Package	256-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/79rc32h434-400bc

Pin Description Table

The following table lists the functions of the pins provided on the RC32434. Some of the functions listed may be multiplexed onto the same pin.

The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
Memory and Peripheral Bus		
BDIRN	O	**External Buffer Direction.** Controls the direction of the external data bus buffer for the memory and peripheral bus. If the RC32434 memory and peripheral bus is connected to the A side of a transceiver, such as an IDT74FCT245, then this pin may be directly connected to the direction control (e.g., BDIR) pin of the transceiver.
BOEN	O	**External Buffer Enable.** This signal provides an output enable control for an external buffer on the memory and peripheral data bus.
WEN	O	**Write Enables.** This signal is the memory and peripheral bus write enable signal.
CSN[3:0]	O	**Chip Selects.** These signals are used to select an external device on the memory and peripheral bus.
MADDR[21:0]	O	**Address Bus.** 22-bit memory and peripheral bus address bus. MADDR[25:22] are available as GPIO alternate functions.
MDATA[7:0]	I/O	**Data Bus.** 8-bit memory and peripheral data bus. During a cold reset, these pins function as inputs that are used to load the boot configuration vector.
OEN	O	**Output Enable.** This signal is asserted when data should be driven by an external device on the memory and peripheral bus.
RWN	O	**Read Write.** This signal indicates whether the transaction on the memory and peripheral bus is a read transaction or a write transaction. A high level indicates a read from an external device. A low level indicates a write to an external device.
WAITACKN	I	**Wait or Transfer Acknowledge.** When configured as wait, this signal is asserted during a memory and peripheral bus transaction to extend the bus cycle. When configured as a transfer acknowledge, this signal is asserted during a transaction to signal the completion of the transaction.
DDR Bus		
DDRADDR[13:0]	O	**DDR Address Bus.** 14-bit multiplexed DDR address bus. This bus is used to transfer the addresses to the DDR devices.
DDRBA[1:0]	O	**DDR Bank Address.** These signals are used to transfer the bank address to the DDRs.
DDRCASN	O	**DDR Column Address Strobe.** This signal is asserted during DDR transactions.
DDRCKE	O	**DDR Clock Enable.** The DDR clock enable signal is asserted during normal DDR operation. This signal is negated following a cold reset or during a power down operation.
DDRCKN	O	**DDR Negative DDR clock.** This signal is the negative clock of the differential DDR clock pair.

Table 1 Pin Description (Part 1 of 6)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes[1]
Memory and Peripheral Bus	BDIRN	O	LVTTL	High Drive		
	BOEN	O	LVTTL	High Drive		
	WEN	O	LVTTL	High Drive		
	CSN[3:0]	O	LVTTL	High Drive		
	MADDR[21:0]	I/O	LVTTL	High Drive		
	MDATA[7:0]	I/O	LVTTL	High Drive		
	OEN	O	LVTTL	High Drive		
	RWN	O	LVTTL	High Drive		
	WAITACKN	I	LVTTL	STI	pull-up	
DDR Bus	DDRADDR[13:0]	O	SSTL_2			
	DDRBA[1:0]	O	SSTL_2			
	DDRCASN	O	SSTL_2			
	DDRCKE	O	SSTL_2 / LVC-MOS			
	DDRCKN	O	SSTL_2			
	DDRCKP	O	SSTL_2			
	DDRCSN	O	SSTL_2			
	DDRDATA[15:0]	I/O	SSTL_2			
	DDRDM[1:0]	O	SSTL_2			
	DDRDQS[1:0]	I/O	SSTL_2			
	DDRRASN	O	SSTL_2			
	DDRVREF	I	Analog			
	DDRWEN	O	SSTL_2			
PCI Bus Interface	PCIAD[31:0]	I/O	PCI			
	PCICBEN[3:0]	I/O	PCI			
	PCICLK	I	PCI			
	PCIDEVSELN	I/O	PCI			pull-up on board
	PCIFRAMEN	I/O	PCI			pull-up on board
	PCIGNTN[3:0]	I/O	PCI			pull-up on board
	PCIIRDYN	I/O	PCI			pull-up on board
	PCILOCKN	I/O	PCI			
	PCIPAR	I/O	PCI			
	PCIPERRN	I/O	PCI			
	PCIREQN[3:0]	I/O	PCI			pull-up on board
	PCIRSTN	I/O	PCI			pull-down on board
	PCISERRN	I/O	PCI	Open Collector		pull-up on board
	PCISTOPN	I/O	PCI			pull-up on board
	PCITRDYN	I/O	PCI			pull-up on board
General Purpose I/O	GPIO[8:0]	I/O	LVTTL	High Drive	pull-up	
	GPIO[13:9]	I/O	PCI			pull-up on board
Serial Peripheral Interface	SCK	I/O	LVTTL	High Drive	pull-up	pull-up on board
	SDI	I/O	LVTTL	High Drive	pull-up	pull-up on board
	SDO	I/O	LVTTL	High Drive	pull-up	pull-up on board
I^2C-Bus Interface	SCL	I/O	LVTTL	Low Drive/STI		pull-up on board[2]
	SDA	I/O	LVTTL	Low Drive/STI		pull-up on board[2]

Table 2 Pin Characteristics (Part 1 of 2)

Signal	Name/Description
MADDR[11]	**Disable Watchdog Timer**. When this bit is set, the watchdog timer is disabled following a cold reset. 0x0 - Watchdog timer enabled 0x1 - Watchdog timer disabled
MADDR[13:12]	**Reserved**. These pins must be driven low during boot configuration.
MADDR[15:14]	**Reserved**. Must be set to zero.

Table 3 Boot Configuration Encoding (Part 2 of 2)

AC Timing Characteristics

(Values given below are based on systems running at recommended operating temperatures and supply voltages, shown in Tables 15 and 16.)

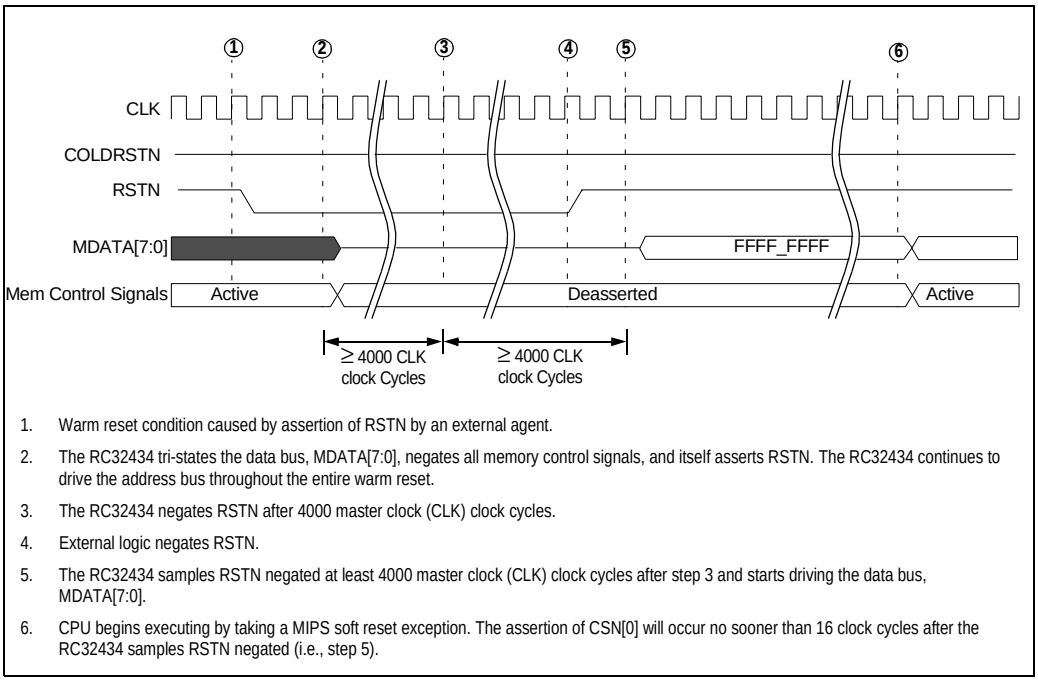
Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Reset													
COLDRSTN[1]	Tpw_6a[2]	none	OSC	—	OSC	—	OSC	—	OSC	—	ms	Cold reset	See Figures 4 and 5.
	Trise_6a	none	—	5.0	—	5.0	—	5.0	—	5.0	ns	Cold reset	
RSTN[3] (input)	Tpw_6b[2]	none	2(CLK)	—	2(CLK)	—	2(CLK)	—	2(CLK)	—	ns	Warm reset	
RSTN[3] (output)	Tdo_6c	COLDRSTN falling	—	15.0	—	15.0	—	15.0	—	15.0	ns	Cold reset	
MADDR[15:0] (boot vector)	Tdz_6d[2]	COLDRSTN falling	—	30.0	—	30.0	—	30.0	—	30.0	ns	Cold reset	
	Tdz_6d[2]	RSTN falling	—	5(CLK)	—	5(CLK)	—	5(CLK)	—	5(CLK)	ns	Warm reset	
	Tzd_6d[2]	RSTN rising	2(CLK)	—	2(CLK)	—	2(CLK)	—	2(CLK)	—	ns	Warm reset	

Table 6 Reset and System AC Timing Characteristics

1. The COLDRSTN minimum pulse width is the oscillator stabilization time (OSC) with V_{cc} stable.

2. The values for this symbol were determined by calculation, not by testing.

3. RSTN is a bidirectional signal. It is treated as an asynchronous input.



1. Warm reset condition caused by assertion of RSTN by an external agent.
2. The RC32434 tri-states the data bus, MDATA[7:0], negates all memory control signals, and itself asserts RSTN. The RC32434 continues to drive the address bus throughout the entire warm reset.
3. The RC32434 negates RSTN after 4000 master clock (CLK) clock cycles.
4. External logic negates RSTN.
5. The RC32434 samples RSTN negated at least 4000 master clock (CLK) clock cycles after step 3 and starts driving the data bus, MDATA[7:0].
6. CPU begins executing by taking a MIPS soft reset exception. The assertion of CSN[0] will occur no sooner than 16 clock cycles after the RC32434 samples RSTN negated (i.e., step 5).

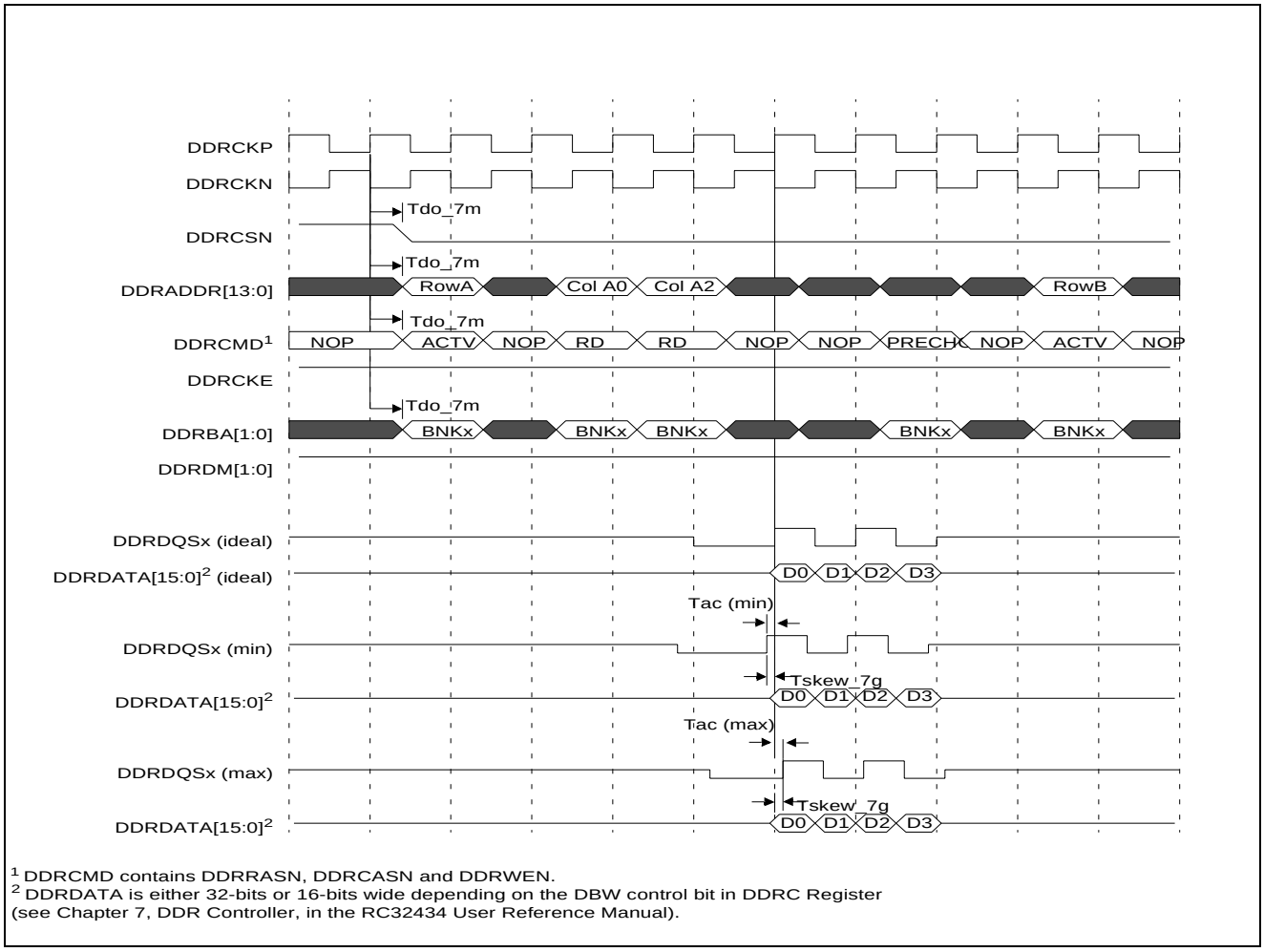
Figure 5 Externally Initiated Warm Reset AC Timing Waveform

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max		
Memory Bus - DDR Access												
DDRDATA[15:0]	Tskew_7g	DDRDQSx	0	0.9	0	0.8[1]	0	0.7	0.0	0.6	ns	See Figures 6 and 7.
	Tdo_7k[2]		1.2	1.9	1.0	1.7	0.7	1.5	0.5	1.4	ns	
DDRDM[1:0]	Tdo_7l	DDRDQSx	1.2	1.9	1.0	1.7	0.7	1.5	0.5	1.4	ns	
DDRDQS[1:0]	Tdo_7i	DDRCKP	-0.75	0.75	-0.75	0.75	-0.7	0.7	-0.7	0.7	ns	
DDRADDR[13:0], DDRBA[1:0], DDRCASN, DDRCKE, DDRCSN, DDRRASN, DDRWEN	Tdo_7m	DDRCKP	1.0	4.0	1.0	4.3	1.0	4.0	1.0	4.0	ns	

Table 7 DDR SDRAM Timing Characteristics

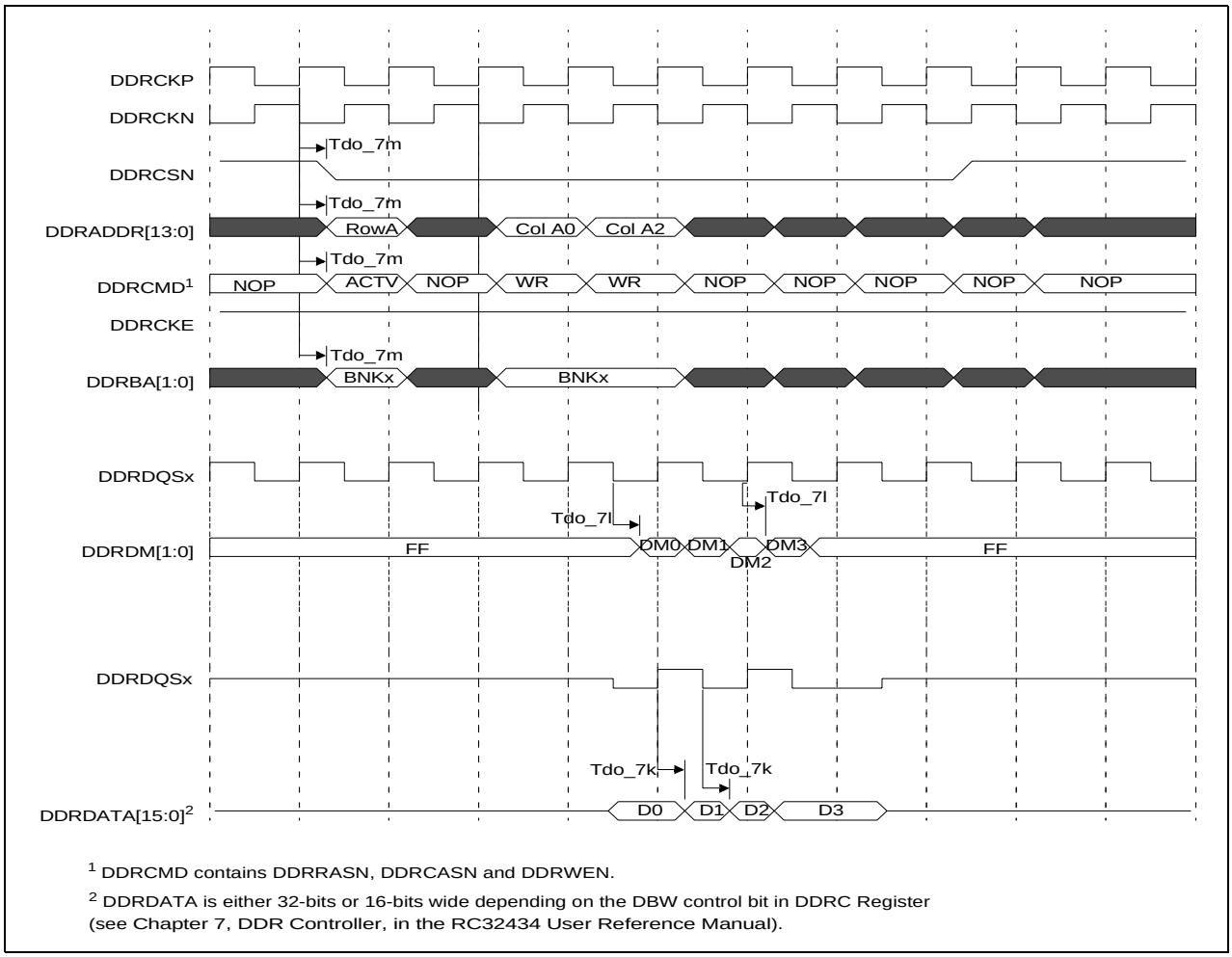
1. Meets DDR timing requirements for 150MHz clock rate DDR SDRAMs with 300 ps remaining margin to compensate for PCB propagation mismatches, which is adequate to guarantee functional timing, provided the RC32434 DDR layout guidelines are adhered to.

2. Setup times are calculated as applicable clock period - Tdo max. For example, if the DDR is running at 266MHz, it uses a 133MHz input clock. The period for a 133MHz clock is 7.5ns. If the Tdo max value is 4.6ns, the T_{IS} parameter is 7.5ns minus 4.6ns = 2.9ns. The DDR spec for this parameter is 1ns, so there is 1.9ns of slack left over for board propagation. Calculations for T_{DS} are similar, but since this parameter is taken relative to the DDRDQS signals, which are referenced on both edges, the effective period with a 133MHz input clock is only 3.75ns. So, if the max Tdo is 1.9ns, we have 3.75ns minus 1.9ns = 1.85ns for T_{DS}. The DDR data sheet specs a value of 0.5ns for 266MHz, so this leaves 1.35ns slack for board propagation delays.



[1] DDRCMD contains DDRRASN, DDRCASN and DDRWEN.
[2] DDRDATA is either 32-bits or 16-bits wide depending on the DBW control bit in DDRC Register (see Chapter 7, DDR Controller, in the RC32434 User Reference Manual).

Figure 6 DDR SDRAM AC Timing Waveform - SDRAM Read Access



[1] DDRCMD contains DDRRASN, DDRCASN and DDRWEN.

[2] DDRDATA is either 32-bits or 16-bits wide depending on the DBW control bit in DDRC Register (see Chapter 7, DDR Controller, in the RC32434 User Reference Manual).

Figure 7 DDR SDRAM Timing Waveform — Write Access

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Condi-tions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Memory and Peripheral Bus[1]													See Figures 8 and 9.
MADDR[21:0]	Tdo_8a	EXTCLK rising	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns		
	Tdz_8a[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8a[2]		—	—	—	—	—	—	—	—	ns		
MADDR[25:22]	Tdo_8b	EXTCLK rising	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns		
	Tdz_8b[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8b[2]		—	—	—	—	—	—	—	—	ns		

Table 8 Memory and Peripheral Bus AC Timing Characteristics (Part 1 of 2)

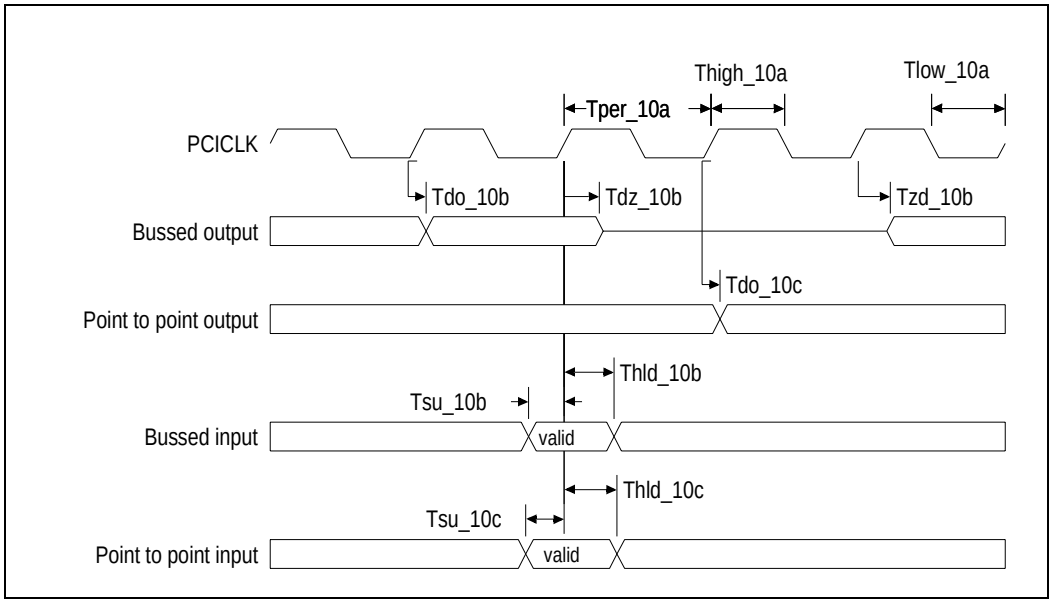
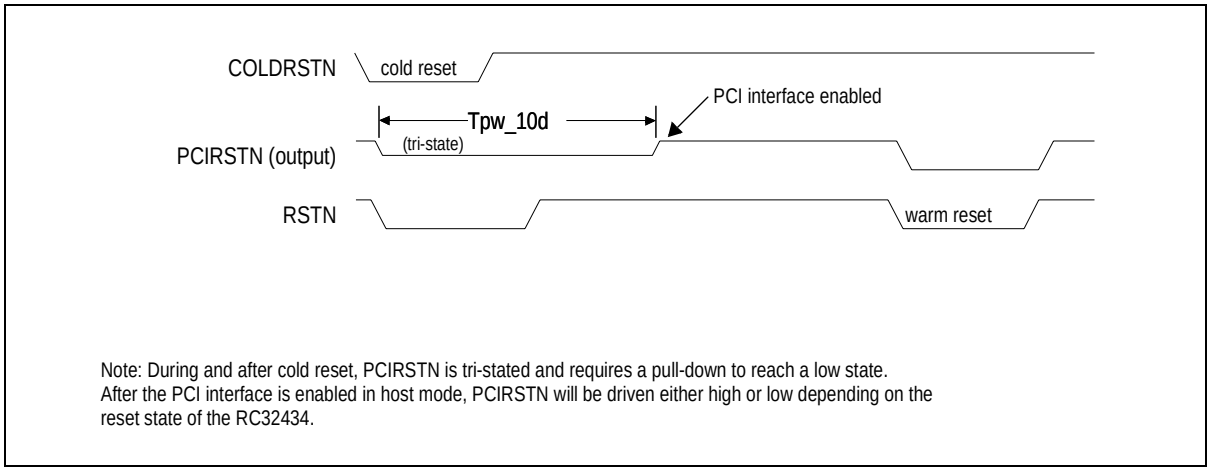


Figure 11 PCI AC Timing Waveform



Note: During and after cold reset, PCIRSTN is tri-stated and requires a pull-down to reach a low state. After the PCI interface is enabled in host mode, PCIRSTN will be driven either high or low depending on the reset state of the RC32434.

Figure 12 PCI AC Timing Waveform — PCI Reset in Host Mode

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Condi-tions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
SPI[1]													
SCK	Tper_15a	None	100	166667	100	166667	100	166667	100	166667	ns	SPI	See Figures 16, 17, and 18.
	Thigh_15a, Tlow_15a		40	83353	40	83353	40	83353	40	83353	ns	SPI	
SDI	Tsu_15b	SCK rising or falling	60	—	60	—	60	—	60	—	ns	SPI	See Figures 16, 17, and 18.
	Thld_15b		60	—	60	—	60	—	60	—	ns	SPI	
SDO	Tdo_15c	SCK rising or falling	0	60	0	60	0	60	0	60	ns	SPI	
SCK, SDI, SDO	Tpw_15e	None	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	ns	Bit I/O	

Table 13 SPI AC Timing Characteristics

1. In SPI mode, the SCK period and sampling edge are programmable. In PCI mode, the SCK period is fixed and the sampling edge is rising.

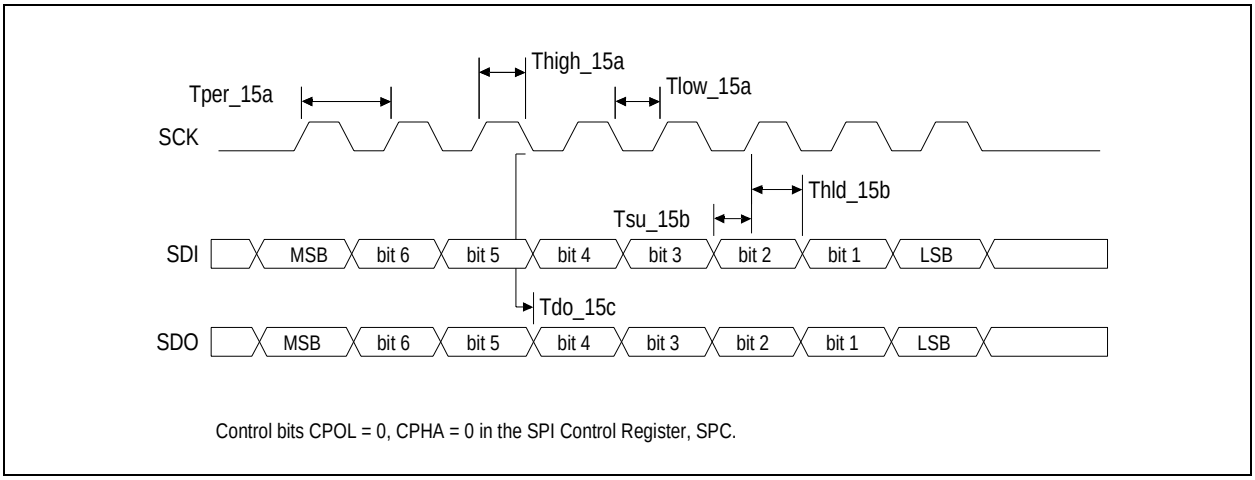


Figure 16 SPI AC Timing Waveform — Clock Polarity 0, Clock Phase 0

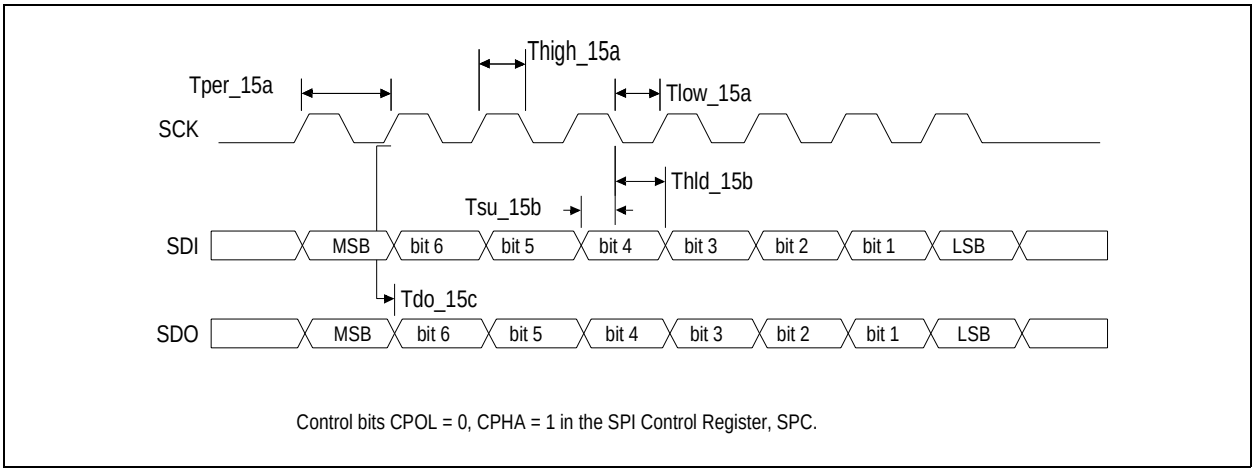


Figure 17 SPI AC Timing Waveform — Clock Polarity 0, Clock Phase 1

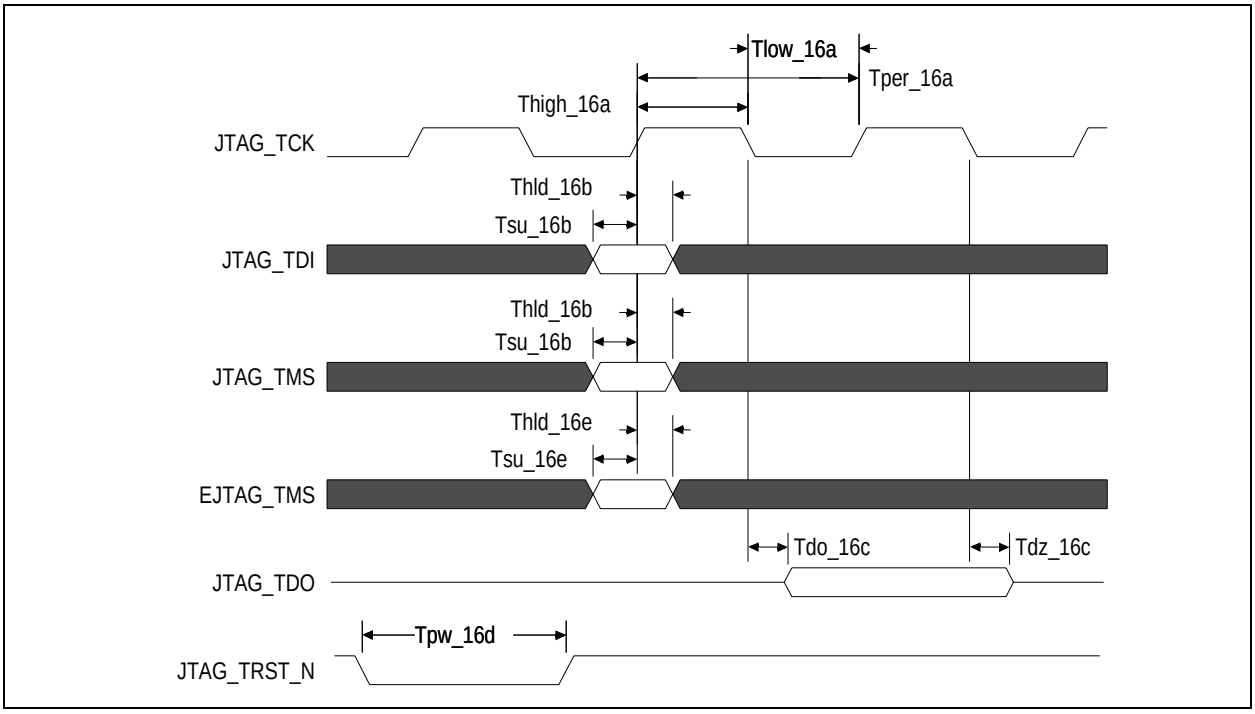


Figure 19 JTAG AC Timing Waveform

The IEEE 1149.1 specification requires that the JTAG and EJTAG TAP controllers be reset at power-up whether or not the interfaces are used for a boundary scan or a probe. Reset can occur through a pull-down resistor on JTAG_TRST_N if the probe is not connected. However, on-chip pull-up resistors are implemented on the RC32434 due to an IEEE 1149.1 requirement. Having on-chip pull-up and external pull-down resistors for the JTAG_TRST_N signal requires special care in the design to ensure that a valid logical level is provided to JTAG_TRST_N, such as using a small external pull-down resistor to ensure this level overrides the on-chip pull-up. An alternative is to use an active power-up reset circuit for JTAG_TRST_N, which drives JTAG_TRST_N low only at power-up and then holds JTAG_TRST_N high afterwards with a pull-up resistor.

Figure 20 shows the electrical connection of the EJTAG probe target system connector.

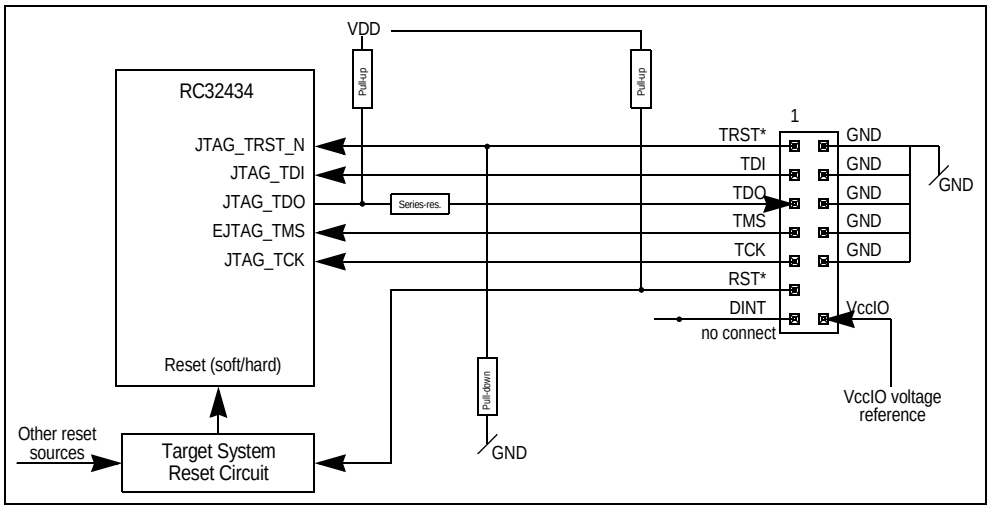
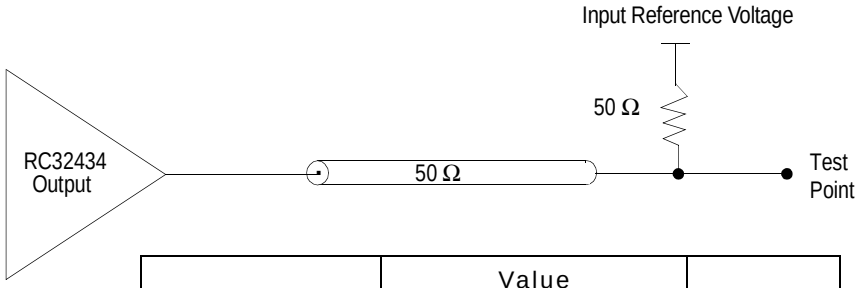


Figure 20 Target System Electrical EJTAG Connection

AC Test Conditions



Parameter	Value		Units
	SSTL I/O	Other I/O	
Input pulse levels	0 to 2.5	0 to 3.3	V
Input rise/fall	0.8	1.0	ns
Input reference level	0.5(VccSI/O)	0.5(VccI/O)	V
Output reference levels	1.25	1.5	V
AC test load	35	35	pF

Figure 23 AC Test Conditions

Absolute Maximum Ratings

Symbol	Parameter	Min[1]	Max[1]	Unit
V_{CC}I/O	I/O supply except for SSTL_2[2]	-0.6	4.0	V
V_{CC}SI/O (DDR)	I/O supply for SSTL_2[2]	-0.6	4.0	V
V_{CC}Core	Core Supply Voltage	-0.6	2.0	V
V_{CC}PLL	PLL supply (digital)	-0.6	2.0	V
V_{CC}APLL	PLL supply (analog)	-0.6	4.0	V
VinI/O	I/O Input Voltage except for SSTL_2	-0.6	V_{cc}I/O+ 0.5	V
VinSI/O	I/O Input Voltage for SSTL_2	-0.6	V_{cc}SI/O+ 0.5	V
T_a Industrial	Ambient Operating Temperature	-40	+85	°C
T_a Commercial	Ambient Operating Temperature	0	+70	°C
T_s	Storage Temperature	-40	+125	°C

Table 19 Absolute Maximum Ratings

1. Functional and tested operating conditions are given in Table 15. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. SSTL_2 I/Os are used to connect to DDR SDRAM.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
C2	BDIRN		G2	MIITXER		L2	SCL		R2	PCICBEN[3]	
C3	COLDRSTN		G3	MIIRXER		L3	GPIO[8]	1	R3	PCIAD[23]	
C4	WEN		G4	MIITXCLK		L4	SDI		R4	PCIAD[21]	
C5	MDATA[3]		G5	V_{cc} I/0		L5	V_{cc} I/0		R5	PCIAD[17]	
C6	MDATA[5]		G6	V_{ss}		L6	V_{ss}		R6	PCIRSTN	
C7	GPIO[6]	1	G7	V_{ss}		L7	V_{ss}		R7	PCICBEN[2]	
C8	MADDR[21]		G8	V_{ss}		L8	V_{cc} CORE		R8	PCITRDYN	
C9	MADDR[18]		G9	V_{ss}		L9	V_{ss}		R9	PCICBEN[1]	
C10	MADDR[14]		G10	V_{ss}		L10	V_{ss}		R10	PCIAD[12]	
C11	JTAG_TMS		G11	V_{ss}		L11	V_{ss}		R11	PCIAD[8]	
C12	V_{cc} APLL		G12	V_{cc} DDR		L12	V_{cc} DDR		R12	PCIAD[5]	
C13	CLK		G13	DDRDM[1]		L13	DDRADDR[9]		R13	PCIAD[3]	
C14	MADDR[4]		G14	DDRDQS[1]		L14	DDRWEN		R14	PCIAD[0]	
C15	MADDR[0]		G15	DDRDATA[10]		L15	DDRCASN		R15	PCIGNTN[2]	
C16	DDRDATA[0]		G16	DDRDATA[11]		L16	DDRADDR[8]		R16	DDRADDR[1]	
D1	MIIRXD[0]		H1	MIIMDIO		M1	GPIO[12]	1	T1	PCIAD[24]	
D2	MIICL		H2	MIIMDC		M2	PCIAD[31]		T2	GPIO[13]	1
D3	MIICRS		H3	GPIO[0]	1	M3	GPIO[11]	1	T3	PCIAD[22]	
D4	MIIRXD[1]		H4	GPIO[1]	1	M4	GPIO[9]	1	T4	PCIAD[19]	
D5	MDATA[7]		H5	V_{cc} CORE		M5	V_{cc} I/0		T5	PCIAD[16]	
D6	MDATA[2]		H6	V_{cc} CORE		M6	V_{cc} I/0		T6	PCICLK	
D7	MDATA[0]		H7	V_{ss}		M7	V_{cc} I/0		T7	PCIGNTN[0]	
D8	MADDR[20]		H8	V_{ss}		M8	V_{cc} CORE		T8	PCIDEVSELN	
D9	MADDR[19]		H9	V_{ss}		M9	V_{cc} CORE		T9	PCIPAR	
D10	MADDR[15]		H10	V_{ss}		M10	V_{cc} I/0		T10	PCIAD[13]	
D11	EXTBCV		H11	V_{ss}		M11	V_{cc} DDR		T11	PCIAD[9]	
D12	JTAG_TRSTN		H12	V_{cc} CORE		M12	V_{cc} DDR		T12	PCIAD[6]	
D13	WAITACKN		H13	DDRDATA[15]		M13	DDRRASN		T13	PCIAD[2]	
D14	DDRDATA[2]		H14	DDRDATA[14]		M14	DDRBA[1]		T14	PCIAD[1]	
D15	DDRDATA[3]		H15	DDRDATA[12]		M15	DDRADDR[6]		T15	PCIGNTN[1]	
D16	DDRDATA[1]		H16	DDRDATA[13]		M16	DDRADDR[7]		T16	PCIGNTN[3]	

Table 20 RC32434 Pinout (Part 2 of 2)

RC32434 Ground Pins

V_{ss}	V_{ss}	V_{ss} PLL
F6	J6	A11, B12
F7	J7	
F8	J8	
F10	J9	
F11	J10	
G6	K7	
G7	K8	
G8	K9	
G9	K10	
G10	K11	
G11	L6	
H7	L7	
H8	L9	
H9	L10	
H10	L11	
H11		

Table 23 RC32434 Ground Pins

RC32434 Signals Listed Alphabetically

The following table lists the RC32434 pins in alphabetical order.

Signal Name	I/O Type	Location	Signal Category
BDIRN	O	C2	Memory and Peripheral Bus
BOEN	O	B1	
CLK	I	C13	System
COLDRSTN	I	C3	
CSN[0]	O	A4	Memory and Peripheral Bus
CSN[1]	O	B4	
CSN[2]	O	A3	
CSN[3]	O	B3	

Table 24 RC32434 Alphabetical Signal List (Part 1 of 7)

Signal Name	I/O Type	Location	Signal Category
DDRDATA[15]	I/O	H13	DDR Bus
DDRDM[0]	O	F15	
DDRDM[1]	O	G13	
DDRDQS[0]	I/O	J16	
DDRDQS[1]	I/O	G14	
DDRRASN	O	M13	
DDRVREF	I	J14	
DDRWEN	O	L14	
EJTAG_TMS	I	J4	JTAG / EJTAG
EXTBCV	I	D11	System
EXTCLK	O	C1	
GPIO[0]	I/O	H3	General Purpose Input/Output
GPIO[1]	I/O	H4	
GPIO[2]	I/O	J3	
GPIO[3]	I/O	J1	
GPIO[4]	I/O	A8	
GPIO[5]	I/O	B8	
GPIO[6]	I/O	C7	
GPIO[7]	I/O	A7	
GPIO[8]	I/O	L3	
GPIO[9]	I/O	M4	
GPIO[10]	I/O	P3	
GPIO[11]	I/O	M3	
GPIO[12]	I/O	M1	
GPIO[13]	I/O	T2	
JTAG_TCK	I	J2	JTAG / EJTAG
JTAG_TDI	I	A12	
JTAG_TDO	O	K1	
JTAG_TMS	I	C11	
JTAG_TRSTN	I	D12	

Table 24 RC32434 Alphabetical Signal List (Part 3 of 7)

Signal Name	I/O Type	Location	Signal Category
MADDR[0]	O	C15	Memory and Peripheral Bus
MADDR[1]	O	B16	
MADDR[2]	O	A16	
MADDR[3]	O	B15	
MADDR[4]	O	C14	
MADDR[5]	O	A15	
MADDR[6]	O	B14	
MADDR[7]	O	A14	
MADDR[8]	O	B13	
MADDR[9]	O	A13	
MADDR[10]	O	A5	
MADDR[11]	O	B5	
MADDR[12]	O	B10	
MADDR[13]	O	A10	
MADDR[14]	O	C10	
MADDR[15]	O	D10	
MADDR[16]	O	A9	
MADDR[17]	O	B9	
MADDR[18]	O	C9	
MADDR[19]	O	D9	
MADDR[20]	O	D8	
MADDR[21]	O	C8	
MDATA[0]	I/O	D7	
MDATA[1]	I/O	B6	
MDATA[2]	I/O	D6	
MDATA[3]	I/O	C5	
MDATA[4]	I/O	B7	
MDATA[5]	I/O	C6	
MDATA[6]	I/O	A6	
MDATA[7]	I/O	D5	

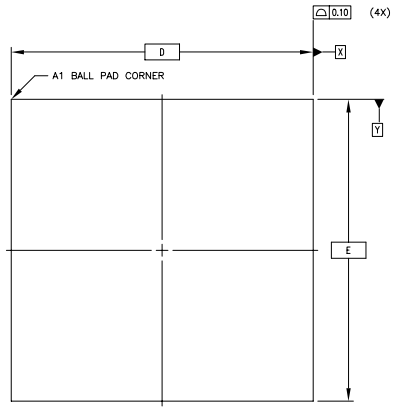
Table 24 RC32434 Alphabetical Signal List (Part 4 of 7)

Signal Name	I/O Type	Location	Signal Category
PCISTOPN	I/O	P8	PCI Bus Interface
PCITRDYN	I/O	R8	
RSTN	I/O	B2	System
RWN	O	A1	Memory and Peripheral Bus
SCK	I/O	K2	Serial Peripheral Interface
SCL	I/O	L2	I^2C
SDA	I/O	L1	
SDI	I/O	L4	Serial Peripheral Interface
SDO	I/O	K4	
Vcc APLL		C12	Power
Vcc Core		E8, E9, F9, H5, H6, H12, J5, J11, J12, L8, M8, M9	
Vcc DDR		E11, E12, F12, G12, K12, L12, M11, M12	
Vcc I/O		E5, E6, E7, E10, F5, G5, K5, K6, L5, M5, M6, M7, M10	
Vcc PLL		B11	
Vss		F6, F7, F8, F10, F11, G6, G7, G8, G9, G10, G11, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, K7, K8, K9, K10, K11, L6, L7, L9, L10, L11	Ground
Vss APLL		B12	
Vss PLL		A11	
WAITACKN	I	D13	Memory and Peripheral Bus
WEN	O	C4	
Reserved		K3, L1, L2	

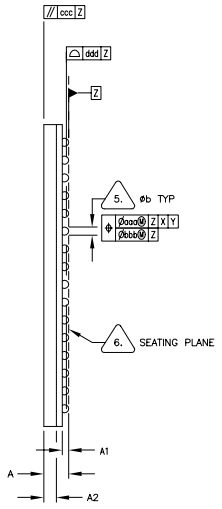
Table 24 RC32434 Alphabetical Signal List (Part 7 of 7)

RC32434 Package Drawing — 256-pin CABGA

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	06/09/00	D.G
	01	JEDEC VARIATION MODIFICATION	07/11/00	D.G
	02	UPDATE MAX. THICKNESS A	10/02/02	



TOP VIEW



SIDE VIEW

SYMBOL	JEDEC VARIATION AAF-1 MIN	NOM	MAX	NOTE
A	1.30	1.40	1.70	
A1	.31	.36	.41	
A2	.65	.70	.75	
D		17.00 BSC		
D1		15.00 BSC		
E		17.00 BSC		
E1		15.00 BSC		
MD		16		3
ME		16		3
N		256		4
e		1.00 BSC		
b	.41	.46	.51	5
aaa	–	–	.15	
bbb	–	–	.08	
ccc	–	–	.10	
ddd	–	–	.12	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS
DECIMAL: XX ±0.10, XXX ±0.05, XXXX ±0.08
ANGULAR: ±1°

APPROVALS	DATE
DRAWN .SX	06/09/00
CHECKED	

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
(408) 727-6116 FAX (408) 492-8074

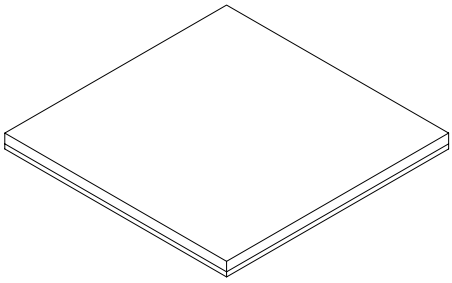
BC256 PACKAGE OUTLINE
17.0 X 17.0 mm BODY CABGA

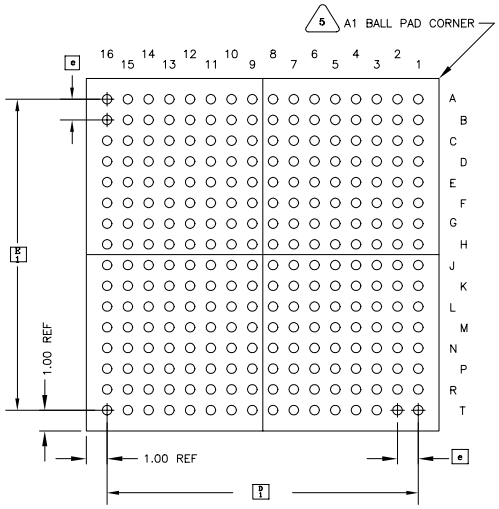
DRAWING No.	SIZE	SCALE	REV
PSC-4093	C	N/A	02

DO NOT SCALE DRAWING — SHEET 1 OF 2

RC32434 Package Drawing — Page Two

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	06/09/00	D.G
	01	JEDEC VARIATION MODIFICATION	07/11/00	D.G
	02	UPDATE MAX. THICKNESS A	10/02/02	





BOTTOM VIEW
256 SOLDER BALLS

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "MD" IS THE MAXIMUM SOLDER BALL MATRIX SIZE IN THE "D" DIRECTION.
   "ME" IS THE MAXIMUM SOLDER BALL MATRIX SIZE IN THE "E" DIRECTION.
4. "N" IS THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.
6. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. "A1" ID CORNER MUST BE IDENTIFIED. IDENTIFICATION MAY BE BY MEANS OF CHAMFER, METALLIZED OR INK MARK, INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY.
8. ALL DIMENSIONS ARE IN MILLIMETERS.
9. THIS DRAWING CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–192 VARIATION AAF–1
   EXCEPTIONS:
   b MIN=0.41 NOM=0.46 MAX=0.51

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS
DECIMAL: X.X ±0.10, X.XX ±0.05, X.XXX ±0.00
ANGULAR: ±1°

APPROVALS	DATE
DRAWN BX	06/09/00
CHECKED	

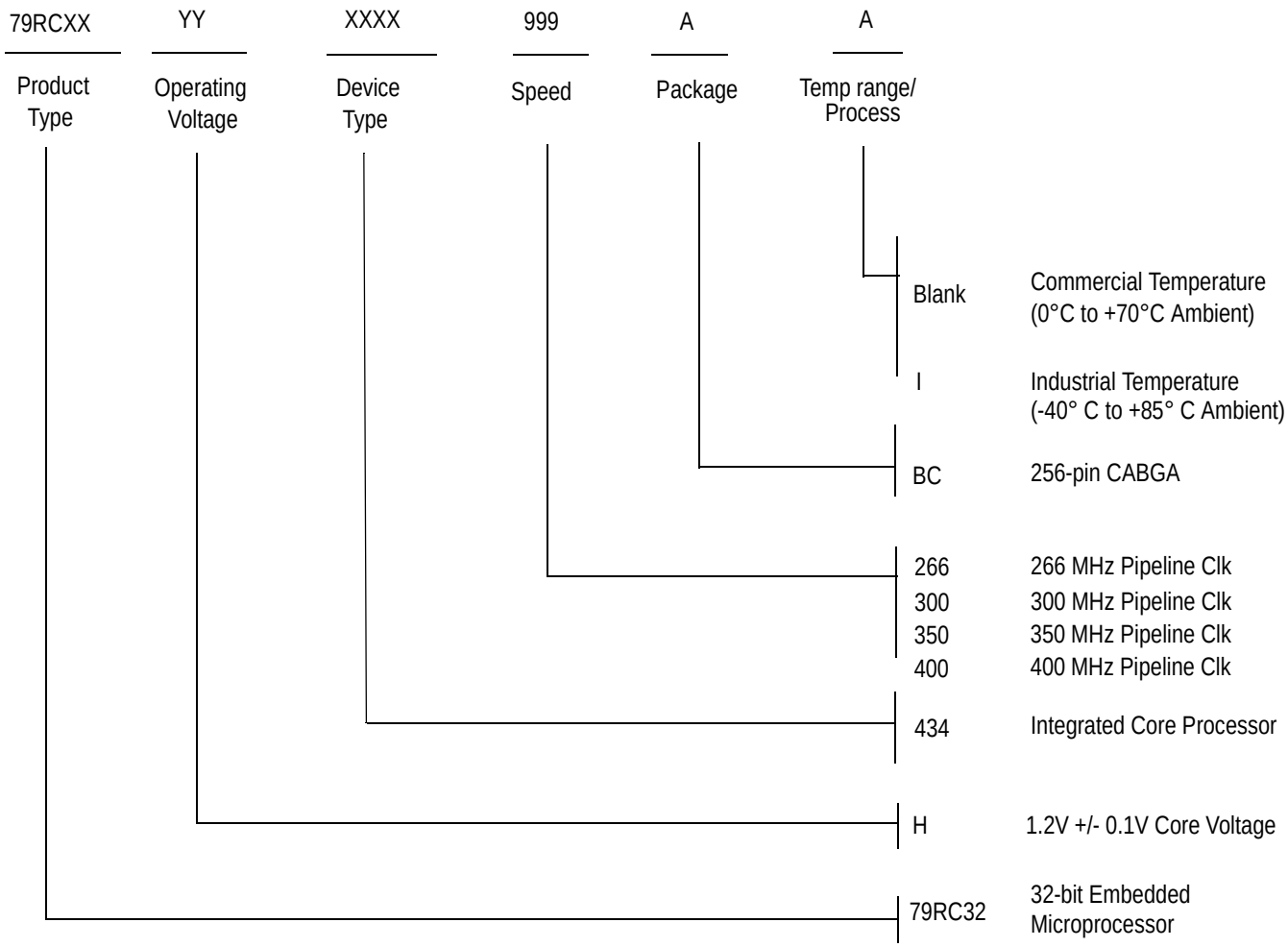
Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
(408) 727–6116 FAX (408) 492–8074

BC256 PACKAGE OUTLINE
17.0 X 17.0 mm BODY CABGA

DRAWING No.	SIZE	SCALE	REV
PSC–4093	C	N/A	02

DO NOT SCALE DRAWING — SHEET 2 OF 2

Ordering Information



Valid Combinations

79RC32H434 - 266BC, 300BC, 350BC, 400BC	256-pin CABGA package, Commercial Temperature
79RC32H434 - 266BCI, 300BCI, 350BCI	256-pin CABGA package, Industrial Temperature

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