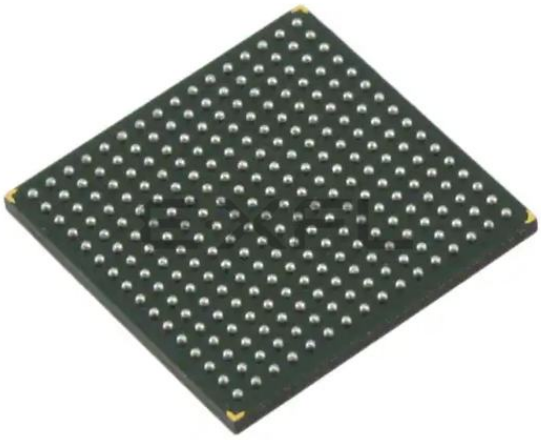
Renesas Electronics America Inc - 79RC32H434-400BCG Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS32
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	256-LBGA
Supplier Device Package	256-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/79rc32h434-400bcg

- **Memory and Peripheral Device Controller**
  - *Provides "glueless" interface to standard SRAM, Flash, ROM, dual-port memory, and peripheral devices*
  - *Demultiplexed address and data buses: 8-bit data bus, 26-bit address bus, 4 chip selects, control for external data bus buffers*

    Automatic byte gathering and scattering
  - *Flexible protocol configuration parameters: programmable number of wait states (0 to 63), programmable postread/post-write delay (0 to 31), supports external wait state generation, supports Intel and Motorola style peripherals*
  - *Write protect capability per chip select*
  - *Programmable bus transaction timer generates warm reset when counter expires*
  - *Supports up to 64 MB of memory per chip select*
- **DMA Controller**
  - *6 DMA channels: two channels for PCI (PCI to Memory and Memory to PCI), two channels for the Ethernet interface, and two channels for memory to memory DMA operations*
  - *Provides flexible descriptor based operation*
  - *Supports unaligned transfers (i.e., source or destination address may be on any byte boundary) with arbitrary byte length*
- **Universal Asynchronous Receiver Transmitter (UART)**
  - *Compatible with the 16550 and 16450 UARTs*
  - *16-byte transmit and receive buffers*
  - *Programmable baud rate generator derived from the system clock*
  - *Fully programmable serial characteristics:*
    - *5, 6, 7, or 8 bit characters*
    - *Even, odd or no parity bit generation and detection*
    - *1, 1-1/2 or 2 stop bit generation*
  - *Line break generation and detection*
  - *False start bit detection*
  - *Internal loopback mode*
- **I^2C-Bus**
  - *Supports standard 100 Kbps mode as well as 400 Kbps fast mode*
  - *Supports 7-bit and 10-bit addressing*
  - *Supports four modes: master transmitter, master receiver, slave transmitter, slave receiver*
- **Additional General Purpose Peripherals**
  - *Interrupt controller*
  - *System integrity functions*
  - *General purpose I/O controller*
  - *Serial peripheral interface (SPI)*
- **Counter/Timers**
  - *Three general purpose 32-bit counter timers*
  - *Timers may be cascaded*
  - *Selectable counter/timer clock source*
- **JTAG Interface**
  - *Compatible with IEEE Std. 1149.1 - 1990*

CPU Execution Core

The 32-bit CPU core is 100% compatible with the MIPS32 instruction set architecture (ISA). Specifically, this device features the 4Kc CPU core developed by MIPS Technologies Inc. (www.mips.com). This core issues a single instruction per cycle, includes a five stage pipeline and is optimized for applications that require integer arithmetic.

The CPU core includes 8 KB instruction and 8 KB data caches. Both caches are 4-way set associative and can be locked on a per line basis, which allows the programmer control over this precious on-chip memory resource. The core also features a memory management unit (MMU). The CPU core also incorporates an enhanced joint test access group (EJTAG) interface that is used to interface to in-circuit emulator tools, providing access to internal registers and enabling the part to be controlled externally, simplifying the system debug process.

The use of this core allows IDT's customers to leverage the broad range of software and development tools available for the MIPS architecture, including operating systems, compilers, and in-circuit emulators.

PCI Interface

The PCI interface on the RC32434 is compatible with version 2.2 of the PCI specification. An on-chip arbiter supports up to six external bus masters, supporting both fixed priority and rotating priority arbitration schemes. The part can support both satellite and host PCI configurations, enabling the RC32434 to act as a slave controller for a PCI add-in card application or as the primary PCI controller in the system. The PCI interface can be operated synchronously or asynchronously to the other I/O interfaces on the RC32434 device.

Ethernet Interface

The RC32434 has one Ethernet Channel supporting 10Mbps and 100Mbps speeds to provide a standard media independent interface (MII or RMII), allowing a wide range of external devices to be connected efficiently.

Double Data Rate Memory Controller

The RC32434 incorporates a high performance double data rate (DDR) memory controller which supports x16 memory configurations up to 256MB. This module provides all of the signals required to interface to discrete memory devices, including a chip select, differential clocking outputs and data strobes.

Memory and I/O Controller

The RC32434 uses a dedicated local memory/IO controller including a de-multiplexed 8-bit data and 26-bit address bus. It includes all of the signals required to interface directly to a maximum of four Intel or Motorola-style external peripherals.

DMA Controller

The DMA controller consists of 6 independent DMA channels, all of which operate in exactly the same manner. The DMA controller off-loads the CPU core from moving data among the on-chip interfaces, external peripherals, and memory. The controller supports scatter/gather DMA with no alignment restrictions, making it appropriate for communications and graphics systems.

UART Interface

The RC32434 contains a serial channel (UART) that is compatible with the industry standard 16550 UART.

I^2C Interface

The standard I2C interface allows the RC32434 to connect to a number of standard external peripherals for a more complete system solution. The RC32434 supports both master and slave operations.

General Purpose I/O Controller

The RC32434 has 14 general purpose input/output pins. Each pin may be used as an active high or active low level interrupt or non-maskable interrupt input, and each signal may be used as a bit input or output port.

System Integrity Functions

The RC32434 contains a programmable watchdog timer that generates a non-maskable interrupt (NMI) when the counter expires and also contains an address space monitor that reports errors in response to accesses to undecoded address regions.

Thermal Considerations

The RC32434 is guaranteed in an ambient temperature range of 0° to +70° C for commercial temperature devices and - 40° to +85° for industrial temperature devices.

Revision History

November 3, 2003: Initial publication. Preliminary Information.

December 15, 2003: Final version. In Table 7, changed maximum value for Tskew in 266MHz category and changed values for Tdo in all speed grades for signals DDRADDR, etc. In Table 8, changed minimum values in all speed grades for all Tdo signals and for Tsu and Tzd in MDATA[7:0]. In Table 16, added reference to Power Considerations document. In Table 17, added 2 rows under PCI and Notes 1 and 2.

January 5, 2004: In Table 19, Pin F6 was changed from Vcc I/O to Vss. In Table 23, pin F6 was deleted from the Vcc I/O row and added to the Vss row.

January 27, 2004: In Table 3, revised description for MADDR[3:0] and changed 4096 cycles to 4000 for MADDR[7]. (Note: MADDR was incorrectly labeled as MDATA in previous data sheet.)

March 29, 2004: Added Standby mode to Table 16, Power Consumption.

April 19, 2004: Added the I^2C feature. In Table 20, pin L1 becomes SDA and pin L2 becomes SCL.

May 25, 2004: In Table 9, signals MIIRXCLK and MIITXCLK, the Min and Max values for Thigh/Tlow_9c were changed to 140 and 260 respectively and the Min and Max values for Thigh/Tlow_9d were changed to 14.0 and 26.0 respectively.

December 8, 2005: In Table 18, corrected error for Capacitance Max value from 8.0 to 10.5.

January 19, 2006: Removed all references to NVRAM.

Signal	Type	Name/Description
DDRCKP	O	**DDR Positive DDR clock.** This signal is the positive clock of the differential DDR clock pair.
DDRCSN	O	**DDR Chip Selects.** This active low signal is used to select DDR device(s) on the DDR bus.
DDRDATA[15:0]	I/O	**DDR Data Bus.** 16-bit DDR data bus is used to transfer data between the RC32434 and the DDR devices. Data is transferred on both edges of the clock.
DDRDM[1:0]	O	**DDR Data Write Enables.** Byte data write enables are used to enable specific byte lanes during DDR writes. DDRDM[0] corresponds to DDRDATA[7:0] DDRDM[1] corresponds to DDRDATA[15:8]
DDRDQS[1:0]	I/O	**DDR Data Strobes.** DDR byte data strobes are used to clock data between DDR devices and the RC32434. These strobes are inputs during DDR reads and outputs during DDR writes. DDRDQS[0] corresponds to DDRDATA[7:0] DDRDQS[1] corresponds to DDRDATA[15:8]
DDRRASN	O	**DDR Row Address Strobe.** The DDR row address strobe is asserted during DDR transactions.
DDRVREF	I	**DDR Voltage Reference.** SSTL_2 DDR voltage reference is generated by an external source.
DDRWEN	O	**DDR Write Enable.** DDR write enable is asserted during DDR write transactions.
PCI Bus		
PCIAD[31:0]	I/O	**PCI Multiplexed Address/Data Bus**. Address is driven by a bus master during initial PCIFRAMEN assertion. Data is then driven by the bus master during writes or by the bus target during reads.
PCICBEN[3:0]	I/O	**PCI Multiplexed Command/Byte Enable Bus**. PCI commands are driven by the bus master during the initial PCIFRAMEN assertion. Byte enable signals are driven by the bus master during subsequent data phase(s).
PCICLK	I	**PCI Clock**. Clock used for all PCI bus transactions.
PCIDEVSELN	I/O	**PCI Device Select**. This signal is driven by a bus target to indicate that the target has decoded the address as one of its own address spaces.
PCIFRAMEN	I/O	**PCI Frame**. Driven by a bus master. Assertion indicates the beginning of a bus transaction. Negation indicates the last data.
PCIGNTN[3:0]	I/O	**PCI Bus Grant**. **In PCI host mode with internal arbiter:** The assertion of these signals indicates to the agent that the internal RC32434 arbiter has granted the agent access to the PCI bus. **In PCI host mode with external arbiter:** PCIGNTN[0]: asserted by an external arbiter to indicate to the RC32434 that access to the PCI bus has been granted. PCIGNTN[3:1]: unused and driven high. **In PCI satellite mode:** PCIGNTN[0]: This signal is asserted by an external arbiter to indicate to the RC32434 that access to the PCI bus has been granted. PCIGNTN[3:1]: unused and driven high.
PCIIRDYN	I/O	**PCI Initiator Ready**. Driven by the bus master to indicate that the current datum can complete.

Table 1 Pin Description (Part 2 of 6)

Signal	Type	Name/Description
GPIO[4]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[22] Alternate function: Memory and peripheral bus address.
GPIO[5]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[23] Alternate function: Memory and peripheral bus address.
GPIO[6]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[24] Alternate function: Memory and peripheral bus address. The value of this pin may be used as a counter timer clock input (see Counter Timer Clock Select Register in Chapter 14, Counter/Timers, of the RC32434 User Manual).
GPIO[7]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[25] Alternate function: Memory and peripheral bus address. The value of this pin may be used as a counter timer clock input (see Counter Timer Clock Select Register in Chapter 14, Counter/Timers, of the RC32434 User Manual).
GPIO[8]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: CPU Alternate function: CPU or DMA debug output pin.
GPIO[9]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIREQN[4] Alternate function: PCI Request 4.
GPIO[10]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIGNTN[4] Alternate function: PCI Grant 4.
GPIO[11]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIREQN[5] Alternate function: PCI Request 5.
GPIO[12]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIGNTN[5] Alternate function: PCI Grant 5.
GPIO[13]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIMUINTN Alternate function: PCI Messaging unit interrupt output.
SPI Interface		
SCK	I/O	**Serial Clock**. This signal is used as the serial clock output. This pin may be used as a bit input/output port.

Table 1 Pin Description (Part 4 of 6)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes[1]
Ethernet Interfaces	MIICL	I	LVTTL	STI	pull-down	
	MIICRS	I	LVTTL	STI	pull-down	
	MIIRXCLK	I	LVTTL	STI	pull-up	
	MIIRXD[3:0]	I	LVTTL	STI	pull-up	
	MIIRXDV	I	LVTTL	STI	pull-down	
	MIIRXER	I	LVTTL	STI	pull-down	
	MIITXCLK	I	LVTTL	STI	pull-up	
	MIITXD[3:0]	O	LVTTL	Low Drive		
	MIITXENP	O	LVTTL	Low Drive		
	MIITXER	O	LVTTL	Low Drive		
	MIIMDC	O	LVTTL	Low Drive		
	MIIMDIO	I/O	LVTTL	Low Drive	pull-up	
EJTAG / JTAG	JTAG_TMS	I	LVTTL	STI	pull-up	
	EJTAG_TMS	I	LVTTL	STI	pull-up	
	JTAG_TRST_N	I	LVTTL	STI	pull-up	
	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDO	O	LVTTL	Low Drive		
	JTAG_TDI	I	LVTTL	STI	pull-up	
System	CLK	I	LVTTL	STI		
	EXTBCV	I	LVTTL	STI	pull-down	
	EXTCLK	O	LVTTL	High Drive		
	COLDRSTN	I	LVTTL	STI		
	RSTN	I/O	LVTTL	Low Drive / STI	pull-up	pull-up on board

Table 2 Pin Characteristics (Part 2 of 2)

1. External pull-up required in most system applications. Some applications may require additional pull-ups not identified in this table.

2. Use a 2.2K pull-up resistor for I2C pins.

Signal	Name/Description
MADDR[11]	**Disable Watchdog Timer**. When this bit is set, the watchdog timer is disabled following a cold reset. 0x0 - Watchdog timer enabled 0x1 - Watchdog timer disabled
MADDR[13:12]	**Reserved**. These pins must be driven low during boot configuration.
MADDR[15:14]	**Reserved**. Must be set to zero.

Table 3 Boot Configuration Encoding (Part 2 of 2)

AC Timing Definitions

Below are examples of the AC timing characteristics used throughout this document.

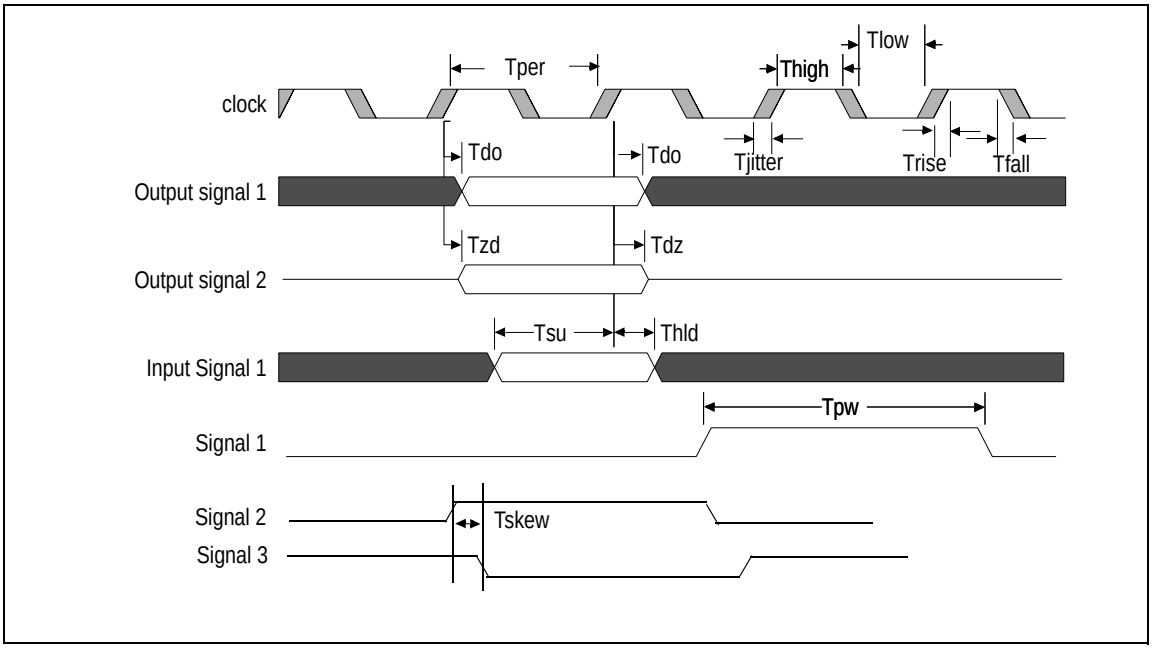
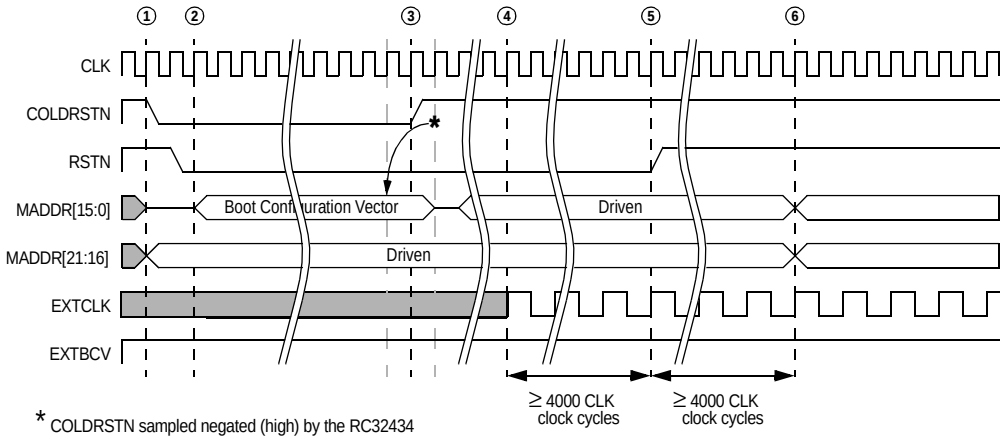


Figure 2 AC Timing Definitions Waveform

Symbol	Definition
Tper	Clock period.
Tlow	Clock low. Amount of time the clock is low in one clock period.
Thigh	Clock high. Amount of time the clock is high in one clock period.
Trise	Rise time. Low to high transition time.
Tfall	Fall time. High to low transition time.
Tjitter	Jitter. Amount of time the reference clock (or signal) edge can vary on either the rising or falling edges.
Tdo	Data out. Amount of time after the reference clock edge that the output will become valid. The minimum time represents the data output hold. The maximum time represents the earliest time the designer can use the data.
Tzd	Z state to data valid. Amount of time after the reference clock edge that the tri-stated output takes to become valid.
Tdz	Data valid to Z state. Amount of time after the reference clock edge that the valid output takes to become tri-stated.
Tsu	Input set-up. Amount of time before the reference clock edge that the input must be valid.
Thld	Input hold. Amount of time after the reference clock edge that the input must remain valid.
Tpw	Pulse width. Amount of time the input or output is active for asynchronous signals.
Tslew	Slew rate. The rise or fall rate for a signal to go from a high to low, or low to high.
X(clock)	Timing value. This notation represents a value of 'X' multiplied by the clock time period of the specified clock. Using 5(CLK) as an example: X = 5 and the oscillator clock (CLK) = 25MHz, then the timing value is 200.
Tskew	Skew. The amount of time two signal edges deviate from one another.

Table 4 AC Timing Definitions



1. EXTBCV is asserted (i.e., pulled-up). COLDRSTN is asserted by external logic. The RC32434 responds by immediately tri-stating the bottom 16-bits of the memory and peripheral address bus (MADDR[15:0]), driving the remaining address bus signals (i.e., MADDR[21:16]), and asserting RSTN. EXTCLK is undefined at this point.
2. External logic drives the boot configuration vector on MADDR[15:0].
3. External logic negates COLDRSTN and tri-states the boot configuration vector on MADDR[15:0]. In response, the RC32434 stops sampling the boot configuration vector and retains the boot configuration vector value seen two clock cycles earlier (i.e., the value on the MADDR[15:0] lines two rising edges of CLK earlier). Within 16 CLK clock cycles after COLDRSTN is sampled negated, the RC32434 begins driving MADDR[15:0].
4. The RC32434 waits for the PLL to stabilize.
5. The RC32434 then begins generating EXTCLK.
6. After at least 4000 CLK clock cycles, the RC32434 tri-states RSTN.
7. At least 4000 CLK clock cycles after negating RSTN, the RC32434 samples RSTN. If RSTN is negated, cold reset has completed and the RC32434 CPU begins executing by taking MIPS reset exception.

Figure 4 COLD Reset Operation with External Boot Configuration Vector AC Timing Waveform

Note: For a diagram showing the COLD Reset Operation with Internal Boot Configuration Vector, see Figure 3.6 in the RC32434 User Reference Manual.

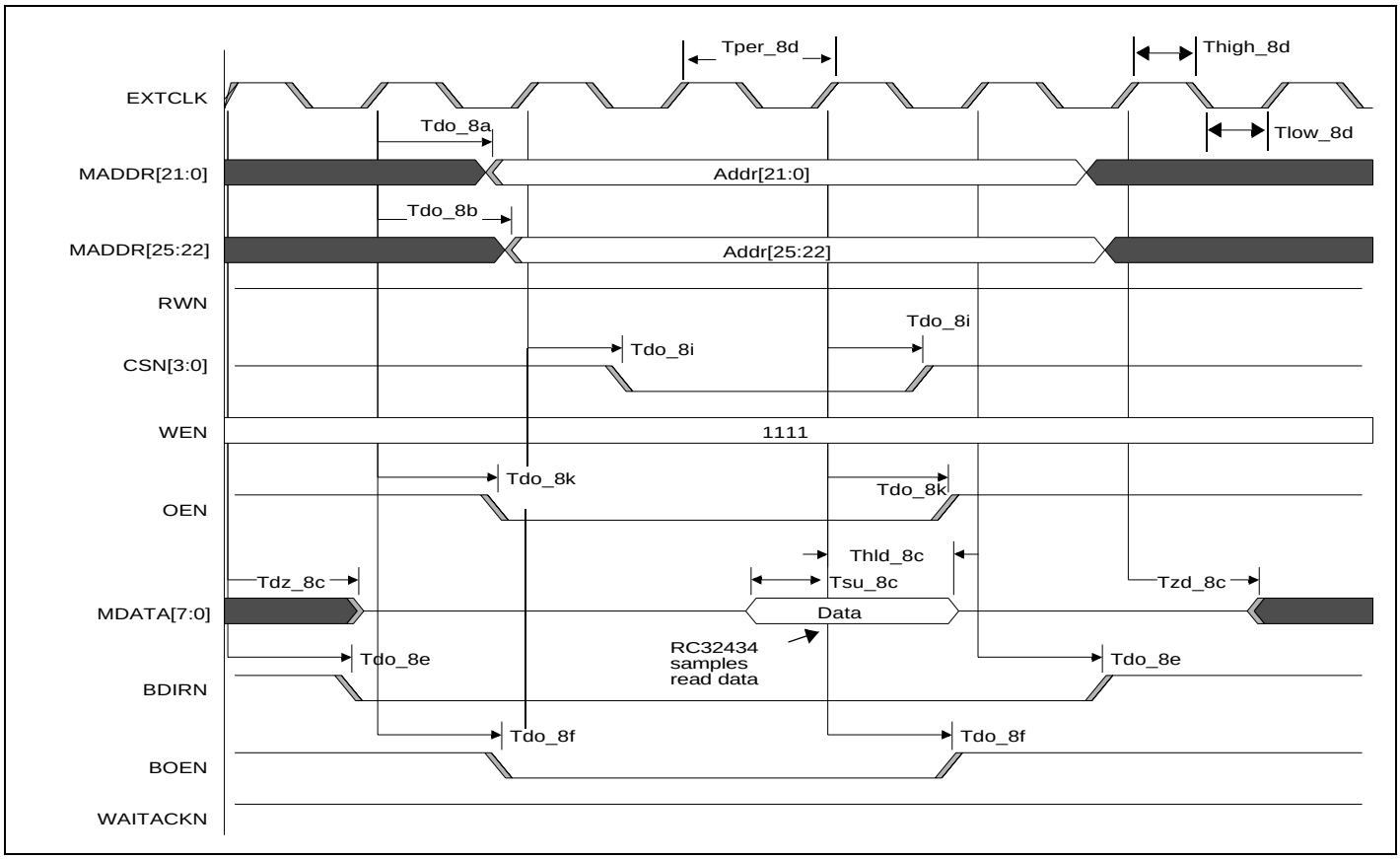


Figure 8 Memory and Peripheral Bus AC Timing Waveform — Read Access

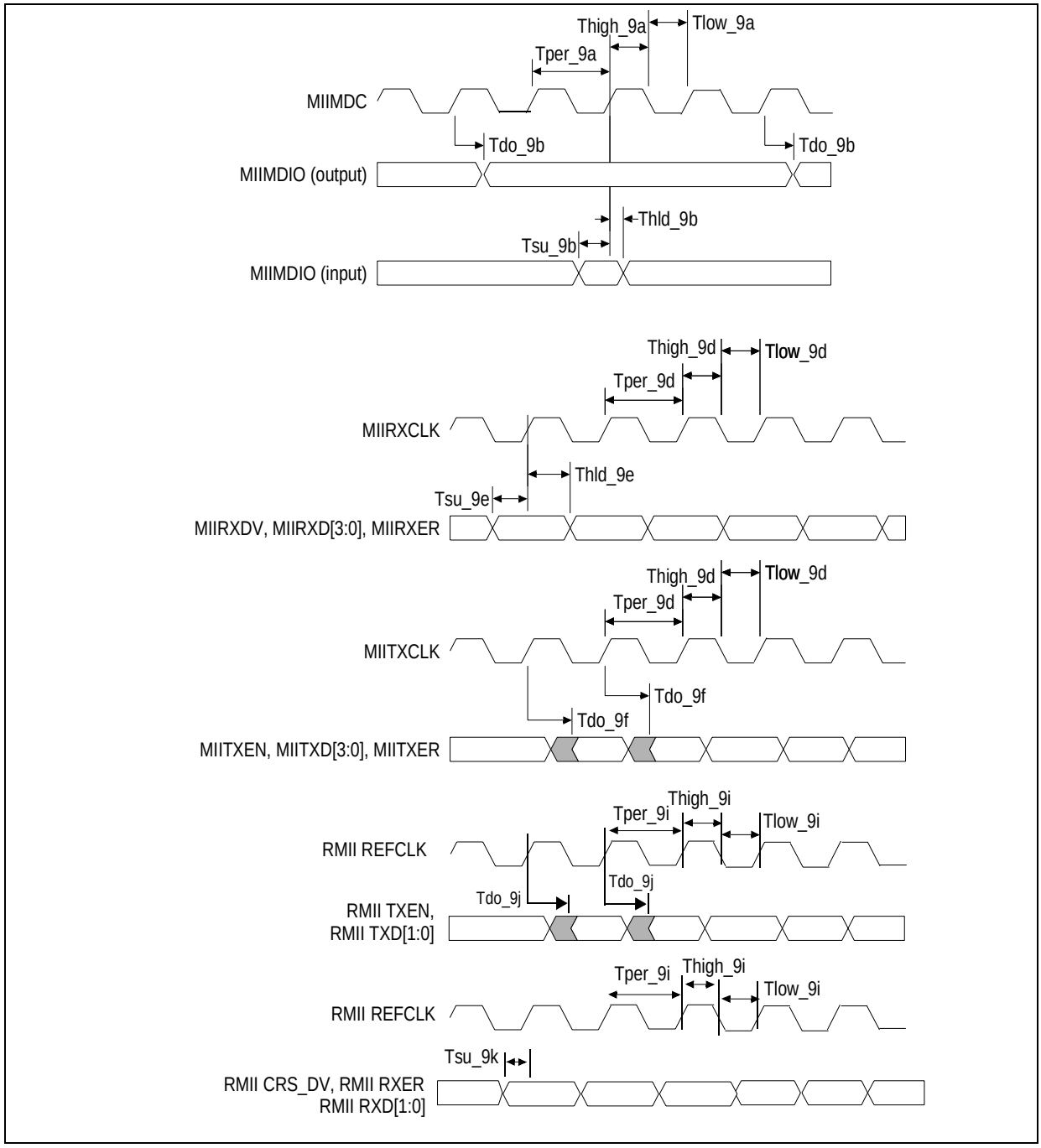


Figure 10 Ethernet AC Timing Waveform

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Start or repeated start condition	Tsu_12c	SDA falling	0.6	—	0.6	—	0.6	—	0.6	—	µs	400 KHz	See Figure 14.
	Thld_12c		0.6	—	0.6	—	0.6	—	0.6	—	µs		
Stop condition	Tsu_12d	SDA rising	0.6	—	0.6	—	0.6	—	0.6	—	µs		
Bus free time between a stop and start condition	Tdelay_12e		1.3	—	1.3	—	1.3	—	1.3	—	µs		

Table 11 I²C AC Timing Characteristics (Part 2 of 2)

1. For more information, see the I²C-Bus specification by Philips Semiconductor.

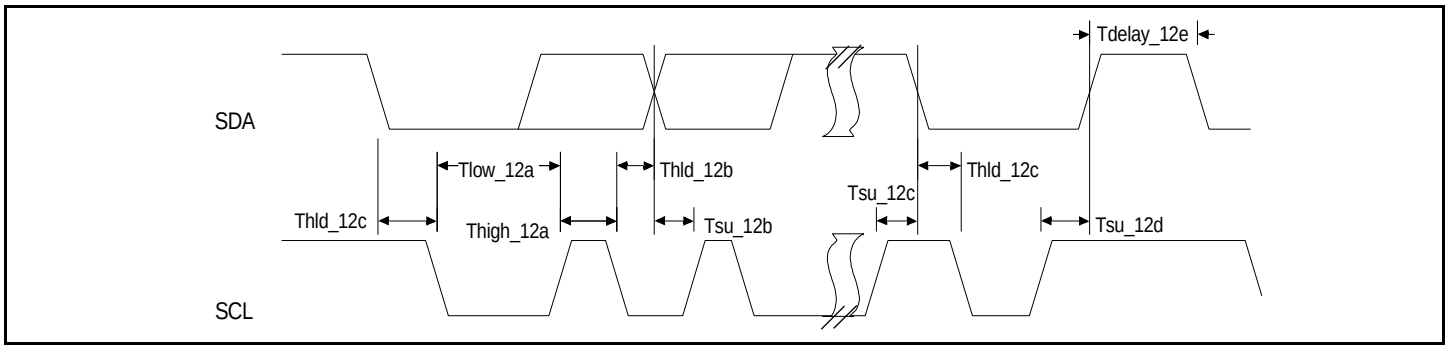


Figure 14 I2C AC Timing Waveform

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
GPIO													
GPIO[13:0]	Tpw_13b[1]	None	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	ns		See Figure 15.

Table 12 GPIO AC Timing Characteristics

1. The values for this symbol were determined by calculation, not by testing.

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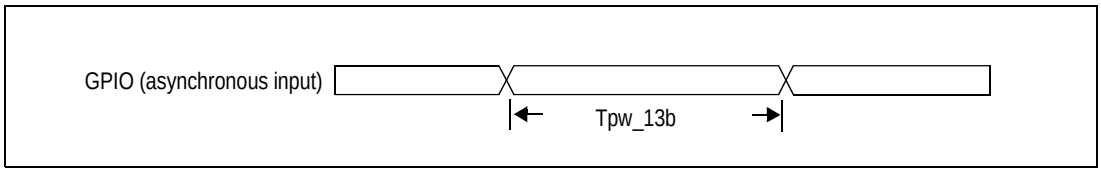


Figure 15 GPIO AC Timing Waveform

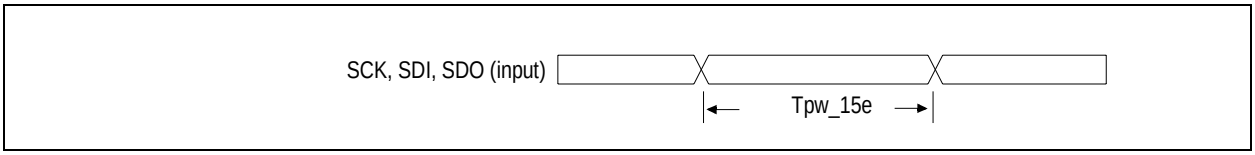


Figure 18 SPI AC Timing Waveform — Bit I/O Mode

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Condi-tions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
EJTAG and JTAG													
JTAG_TCK	Tper_16a	none	25.0	50.0	25.0	50.0	25.0	50.0	25.0	50.0	ns		See Figure 19.
	Thigh_16a, Tlow_16a		10.0	25.0	10.0	25.0	10.0	25.0	10.0	25.0	ns		
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	2.4	—	2.4	—	2.4	—	ns		
	Thld_16b		1.0	—	1.0	—	1.0	—	1.0	—	ns		
JTAG_TDO	Tdo_16c	JTAG_TCK fall-ing	—	11.3	—	11.3	—	11.3	—	11.3	ns		
	Tdz_16c[2]		—	11.3	—	11.3	—	11.3	—	11.3	ns		
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	25.0	—	25.0	—	25.0	—	ns		
EJTAG_TMS[1]	Tsu_16e	JTAG_TCK rising	2.0	—	2.0	—	2.0	—	2.0	—	ns		
	Thld_6e		1.0	—	1.0	—	1.0	—	1.0	—	ns		

Table 14 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that both JTAG_TMS and EJTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when either JTAG_TMS or EJTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

Using the EJTAG Probe

In Figure 20, the pull-up resistors for JTAG_TDO and RST*, the pull-down resistor for JTAG_TRST_N, and the series resistor for JTAG_TDO must be adjusted to the specific design. However, the recommended pull-up/down resistor is 1.0 kΩ because a low value reduces crosstalk on the cable to the connector, allowing higher JTAG_TCK frequencies. A typical value for the series resistor is 33 Ω. Recommended resistor values have ± 5% tolerance.

If a probe is used, the pull-up resistor on JTAG_TDO must ensure that the JTAG_TDO level is high when no probe is connected and the JTAG_TDO output is tri-stated. This requirement allows reliable connection of the probe if it is hooked-up when the power is already on (hot plug). The pull-up resistor value of around 47 kΩ should be sufficient. Optional diodes to protect against overshoot and undershoot voltage can be added on the signals of the chip with EJTAG.

If a probe is used, the RST* signal must have a pull-up resistor because it is controlled by an open-collector (OC) driver in the probe, and thus is actively pulled low only. The pull-up resistor is responsible for the high value when not driven by the probe of 25pF. The input on the target system reset circuit must be able to accept the rise time when the pull-up resistor charges the capacitance to a high logical level. Vcc I/O must connect to a voltage reference that drops rapidly to below 0.5V when the target system loses power, even with a capacitive load of 25pF. The probe can thus detect the lost power condition.

For additional information on EJTAG, refer to Chapter 17 of the RC32434 User Reference Manual.

Phase-Locked Loop (PLL)

The phase-locked loop (PLL) multiplies the external oscillator input (pin CLK) according to the parameter provided by the boot configuration vector to create the processor clock (PCLK). Inherently, PLL circuits are only capable of generating clock frequencies within a limited range.

PLL Filters

It is recommended that the system designer provide a filter network of passive components for the PLL analog and digital power supplies. The PLL circuit power and PLL circuit ground should be isolated from power and ground with a filter circuit such as the one shown in Figure 21. Because the optimum values for the filter components depend upon the application and the system noise environment, these values should be considered as starting points for further experimentation within your specific application.

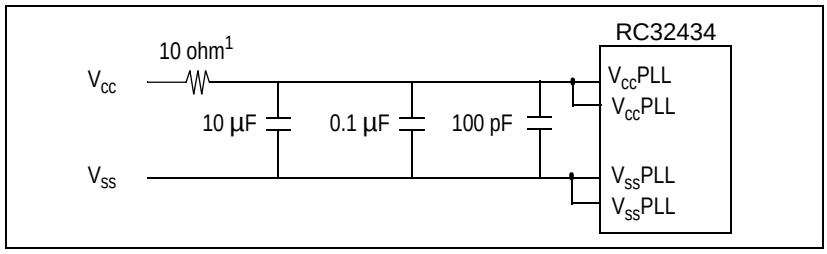


Figure 21 PLL Filter Circuit for Noisy Environments

Power Consumption

Parameter		266MHz		300MHz		350MHz		400MHz		Unit	Conditions
		Typ.	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**		
I_{CC} I/O		215	270	220	275	225	280	230	285	mA	C_L = 35 pF $T_{ambient}$ = 25°C Max. values use the maximum voltages listed in Table 15. Typical values use the typical voltages listed in that table. Note: For additional information, see Power Considerations for IDT Processors on the IDT web site www.idt.com.
I_{CC} SI/O (DDR)		70	85	75	90	85	100	95	110	mA	
I_{CC} Core, I_{CC} PLL	Normal mode	325	510	350	550	400	610	450	670	mA	
	Standby mode[1]	220	—	240	—	260	—	280	—	mA	
Power Dissipation	Normal mode	1.27	1.82	1.36	1.90	1.45	2.02	1.54	2.15	W	
	Standby mode[1]	0.73	—	0.78	—	0.84	—	0.90	—	W	

Table 17 RC32434 Power Consumption

1. The RC32434 enter Standby mode by executing WAIT instructions. Minimal I/O switching is assumed. On-chip logic outside the CPU core continues to function.

Power Curve

The following graph contains a power curve that shows power consumption at various core frequencies.

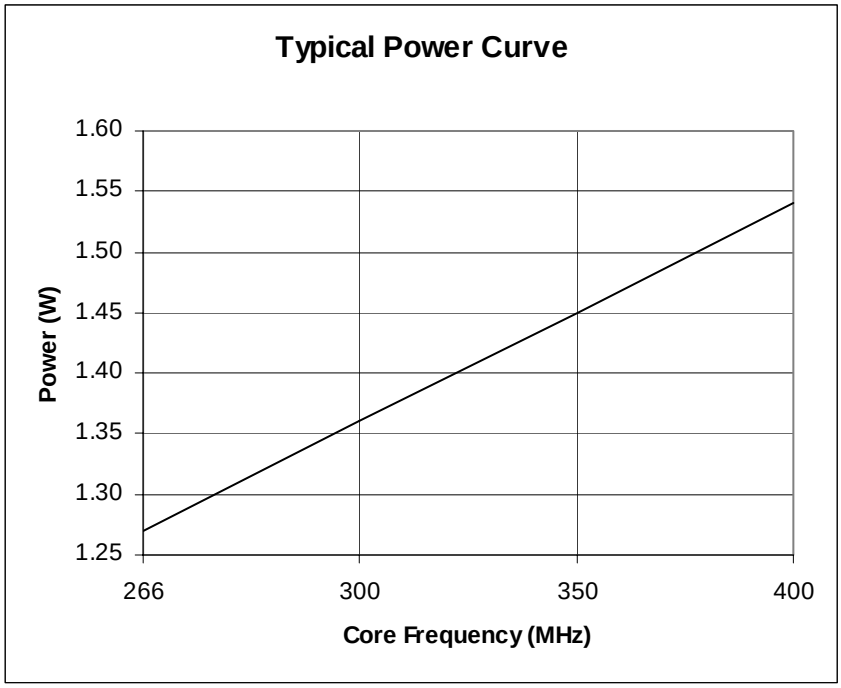


Figure 22 RC32434 Typical Power Usage

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
C2	BDIRN		G2	MIITXER		L2	SCL		R2	PCICBEN[3]	
C3	COLDRSTN		G3	MIIRXER		L3	GPIO[8]	1	R3	PCIAD[23]	
C4	WEN		G4	MIITXCLK		L4	SDI		R4	PCIAD[21]	
C5	MDATA[3]		G5	V_{cc} I/0		L5	V_{cc} I/0		R5	PCIAD[17]	
C6	MDATA[5]		G6	V_{ss}		L6	V_{ss}		R6	PCIRSTN	
C7	GPIO[6]	1	G7	V_{ss}		L7	V_{ss}		R7	PCICBEN[2]	
C8	MADDR[21]		G8	V_{ss}		L8	V_{cc} CORE		R8	PCITRDYN	
C9	MADDR[18]		G9	V_{ss}		L9	V_{ss}		R9	PCICBEN[1]	
C10	MADDR[14]		G10	V_{ss}		L10	V_{ss}		R10	PCIAD[12]	
C11	JTAG_TMS		G11	V_{ss}		L11	V_{ss}		R11	PCIAD[8]	
C12	V_{cc} APLL		G12	V_{cc} DDR		L12	V_{cc} DDR		R12	PCIAD[5]	
C13	CLK		G13	DDRDM[1]		L13	DDRADDR[9]		R13	PCIAD[3]	
C14	MADDR[4]		G14	DDRDQS[1]		L14	DDRWEN		R14	PCIAD[0]	
C15	MADDR[0]		G15	DDRDATA[10]		L15	DDRCASN		R15	PCIGNTN[2]	
C16	DDRDATA[0]		G16	DDRDATA[11]		L16	DDRADDR[8]		R16	DDRADDR[1]	
D1	MIIRXD[0]		H1	MIIMDIO		M1	GPIO[12]	1	T1	PCIAD[24]	
D2	MIICL		H2	MIIMDC		M2	PCIAD[31]		T2	GPIO[13]	1
D3	MIICRS		H3	GPIO[0]	1	M3	GPIO[11]	1	T3	PCIAD[22]	
D4	MIIRXD[1]		H4	GPIO[1]	1	M4	GPIO[9]	1	T4	PCIAD[19]	
D5	MDATA[7]		H5	V_{cc} CORE		M5	V_{cc} I/0		T5	PCIAD[16]	
D6	MDATA[2]		H6	V_{cc} CORE		M6	V_{cc} I/0		T6	PCICLK	
D7	MDATA[0]		H7	V_{ss}		M7	V_{cc} I/0		T7	PCIGNTN[0]	
D8	MADDR[20]		H8	V_{ss}		M8	V_{cc} CORE		T8	PCIDEVSELN	
D9	MADDR[19]		H9	V_{ss}		M9	V_{cc} CORE		T9	PCIPAR	
D10	MADDR[15]		H10	V_{ss}		M10	V_{cc} I/0		T10	PCIAD[13]	
D11	EXTBCV		H11	V_{ss}		M11	V_{cc} DDR		T11	PCIAD[9]	
D12	JTAG_TRSTN		H12	V_{cc} CORE		M12	V_{cc} DDR		T12	PCIAD[6]	
D13	WAITACKN		H13	DDRDATA[15]		M13	DDRRASN		T13	PCIAD[2]	
D14	DDRDATA[2]		H14	DDRDATA[14]		M14	DDRBA[1]		T14	PCIAD[1]	
D15	DDRDATA[3]		H15	DDRDATA[12]		M15	DDRADDR[6]		T15	PCIGNTN[1]	
D16	DDRDATA[1]		H16	DDRDATA[13]		M16	DDRADDR[7]		T16	PCIGNTN[3]	

Table 20 RC32434 Pinout (Part 2 of 2)

RC32434 Alternate Signal Functions

Pin	GPIO	Alternate	Pin	GPIO	Alternate
A7	GPIO[7]	MADDR[25]	J3	GPIO[2]	U0RTSN
A8	GPIO[4]	MADDR[22]	L3	GPIO[8]	CPU
B8	GPIO[5]	MADDR[23]	M1	GPIO[12]	PCIGNTN[5]
C7	GPIO[6]	MADDR[24]	M3	GPIO[11]	PCIREQN[5]
H3	GPIO[0]	U0SOUT	M4	GPIO[9]	PCIREQN[4]
H4	GPIO[1]	U0SINP	P3	GPIO[10]	PCIGNTN[4]
J1	GPIO[3]	U0CTSN	T2	GPIO[13]	PCIMUINTN

Table 21 RC32434 Alternate Signal Functions

RC32434 Power Pins

V_{cc} I/O	V_{cc} DDR	V_{cc} Core	V_{cc} PLL	V_{cc} APLL
E5	E11	E8	B11	C12
E6	E12	E9		
E7	F12	F9		
E10	G12	H5		
F5	K12	H6		
G5	L12	H12		
K5	M11	J5		
K6	M12	J11		
L5		J12		
M5		L8		
M6		M8		
M7		M9		
M10				

Table 22 RC32434 Power Pins

RC32434 Ground Pins

V_{ss}	V_{ss}	V_{ss} PLL
F6	J6	A11, B12
F7	J7	
F8	J8	
F10	J9	
F11	J10	
G6	K7	
G7	K8	
G8	K9	
G9	K10	
G10	K11	
G11	L6	
H7	L7	
H8	L9	
H9	L10	
H10	L11	
H11		

Table 23 RC32434 Ground Pins

RC32434 Signals Listed Alphabetically

The following table lists the RC32434 pins in alphabetical order.

Signal Name	I/O Type	Location	Signal Category
BDIRN	O	C2	Memory and Peripheral Bus
BOEN	O	B1	
CLK	I	C13	System
COLDRSTN	I	C3	
CSN[0]	O	A4	Memory and Peripheral Bus
CSN[1]	O	B4	
CSN[2]	O	A3	
CSN[3]	O	B3	

Table 24 RC32434 Alphabetical Signal List (Part 1 of 7)

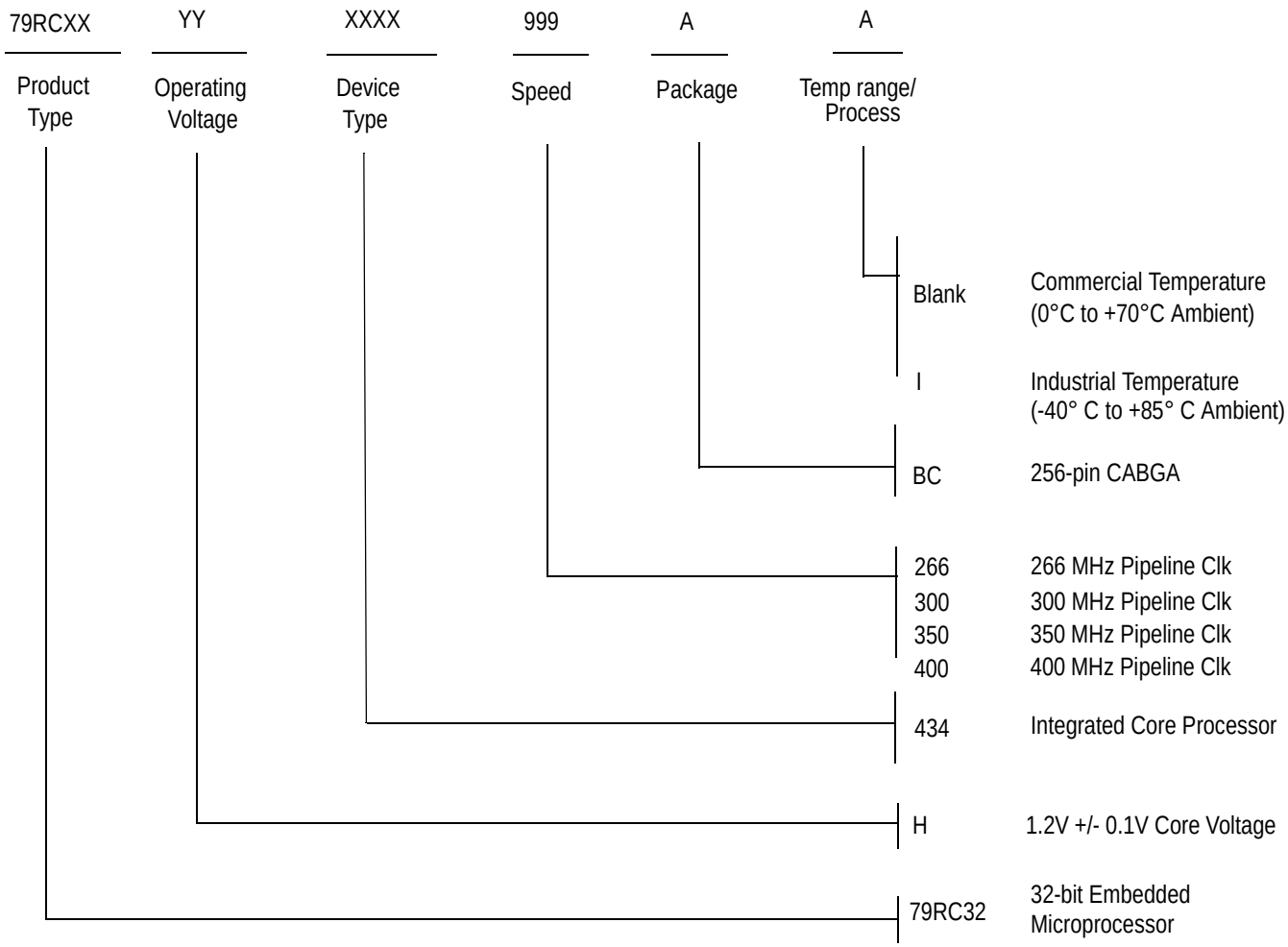
Signal Name	I/O Type	Location	Signal Category
DDRADDR[0]	O	P14	DDR Bus
DDRADDR[1]	O	R16	
DDRADDR[2]	O	P15	
DDRADDR[3]	O	N15	
DDRADDR[4]	O	N14	
DDRADDR[5]	O	N13	
DDRADDR[6]	O	M15	
DDRADDR[7]	O	M16	
DDRADDR[8]	O	L16	
DDRADDR[9]	O	L13	
DDRADDR[10]	O	K15	
DDRADDR[11]	O	K14	
DDRADDR[12]	O	K16	
DDRADDR[13]	O	E15	
DDRBA[0]	O	N16	
DDRBA[1]	O	M14	
DDRCASN	O	L15	
DDRCKE	O	K13	
DDRCKN	O	J13	
DDRCKP	O	J15	
DDRCSN	O	P16	
DDRDATA[0]	I/O	C16	
DDRDATA[1]	I/O	D16	
DDRDATA[2]	I/O	D14	
DDRDATA[3]	I/O	D15	
DDRDATA[4]	I/O	E16	
DDRDATA[5]	I/O	E14	
DDRDATA[6]	I/O	E13	
DDRDATA[7]	I/O	F16	
DDRDATA[8]	I/O	F14	
DDRDATA[9]	I/O	F13	
DDRDATA[10]	I/O	G15	
DDRDATA[11]	I/O	G16	
DDRDATA[12]	I/O	H15	
DDRDATA[13]	I/O	H16	
DDRDATA[14]	I/O	H14	

Table 24 RC32434 Alphabetical Signal List (Part 2 of 7)

Signal Name	I/O Type	Location	Signal Category
PCISTOPN	I/O	P8	PCI Bus Interface
PCITRDYN	I/O	R8	
RSTN	I/O	B2	System
RWN	O	A1	Memory and Peripheral Bus
SCK	I/O	K2	Serial Peripheral Interface
SCL	I/O	L2	I^2C
SDA	I/O	L1	
SDI	I/O	L4	Serial Peripheral Interface
SDO	I/O	K4	
Vcc APLL		C12	Power
Vcc Core		E8, E9, F9, H5, H6, H12, J5, J11, J12, L8, M8, M9	
Vcc DDR		E11, E12, F12, G12, K12, L12, M11, M12	
Vcc I/O		E5, E6, E7, E10, F5, G5, K5, K6, L5, M5, M6, M7, M10	
Vcc PLL		B11	
Vss		F6, F7, F8, F10, F11, G6, G7, G8, G9, G10, G11, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, K7, K8, K9, K10, K11, L6, L7, L9, L10, L11	Ground
Vss APLL		B12	
Vss PLL		A11	
WAITACKN	I	D13	Memory and Peripheral Bus
WEN	O	C4	
Reserved		K3, L1, L2	

Table 24 RC32434 Alphabetical Signal List (Part 7 of 7)

Ordering Information



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79RC32H434 - 266BC, 300BC, 350BC, 400BC	256-pin CABGA package, Commercial Temperature
79RC32H434 - 266BCI, 300BCI, 350BCI	256-pin CABGA package, Industrial Temperature

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