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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.1 ns
Voltage Supply - Internal	1.7V ~ 1.9V
Number of Logic Elements/Blocks	32
Number of Macrocells	512
Number of Gates	12000
Number of I/O	173
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2c512-7pq208c

By mapping a signal to the DataGATE function, lower power can be achieved due to reduction in signal switching.

Another feature that eases voltage translation is I/O banking. Four I/O banks are available on the CoolRunner-II 512 macrocell device that permits easy interfacing to 3.3V, 2.5V, 1.8V, and 1.5V devices.

The CoolRunner-II 512 macrocell CPLD is I/O compatible with various JEDEC I/O standards (see Table 1). This device is also 1.5V I/O compatible with the use of Schmitt-trigger inputs.

RealDigital Design Technology

Xilinx CoolRunner-II CPLDs are fabricated on a 0.18 micron process technology which is derived from leading edge FPGA product development. CoolRunner-II CPLDs employ RealDigital, a design technique that makes use of CMOS technology in both the fabrication and design methodology. RealDigital design technology employs a cascade of CMOS gates to implement sum of products instead of traditional sense amplifier methodology. Due to this technology, Xilinx CoolRunner-II CPLDs achieve both high-performance and low power operation.

Supported I/O Standards

The CoolRunner-II 512 macrocell features LVCMOS, LVTTL, SSTL, and HSTL I/O implementations. See Table 1 for I/O standard voltages. The LVTTL I/O standard is a general purpose EIA/JEDEC standard for 3.3V applications that use an LVTTL input buffer and Push-Pull output buffer. The LVCMOS standard is used in 3.3V, 2.5V, 1.8V applications. Both HSTL and SSTL I/O standards make use of a V_{REF} pin for JEDEC compliance. CoolRunner-II CPLDs are also 1.5V I/O compatible with the use of Schmitt-trigger inputs.

Table 1: **I/O Standards for XC2C512(1)**

IOSTANDARD Attribute	Output V_{CCIO}	Input V_{CCIO}	Input V_{REF}	Board Termination Voltage V_{TT}
LVTTL	3.3	3.3	N/A	N/A
LVCMOS33	3.3	3.3	N/A	N/A
LVCMOS25	2.5	2.5	N/A	N/A
LVCMOS18	1.8	1.8	N/A	N/A
LVCMOS15(2)	1.5	1.5	N/A	N/A
HSTL_1	1.5	1.5	0.75	0.75
SSTL2_1	2.5	2.5	1.25	1.25
SSTL3_1	3.3	3.3	1.5	1.5

(1) For information on Vref pins, see XAPP399.
(2) LVCMOS15 requires Schmitt-trigger inputs.

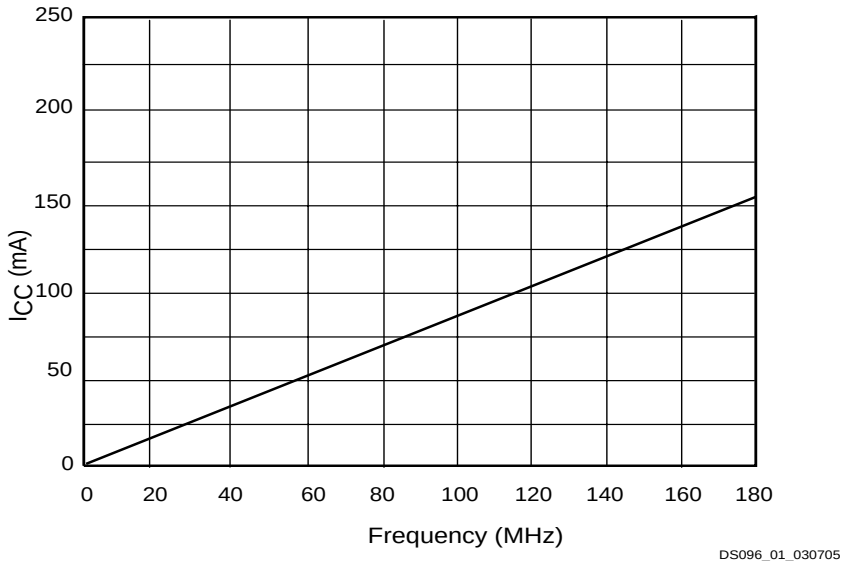


Figure 1: **I_{CC} vs Frequency**

Table 2: **I_{CC} vs Frequency (LVCMOS 1.8V T_A = 25°C)(1)**

	Frequency (MHz)									
	0	20	40	60	80	100	120	140	160	180
Typical I_{CC} (mA)	0.025	17.22	34.37	52.04	69.44	86.85	105.13	122.68	140.23	157.78

Notes:
1. 16-bit up/down, Resetable binary counter (one counter per function block).

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to ground	–0.5 to 2.0	V
V_{CCIO}	Supply voltage for output drivers	–0.5 to 4.0	V
V_{JTAG}(2)	JTAG input voltage limits	-0.5 to 4.0	V
V_{CCAUX}	JTAG input supply voltage	-0.5 to 4.0	V
V_{IN}(1)	Input voltage relative to ground(1)	–0.5 to 4.0	V
V_{TS}(1)	Voltage applied to 3-state output(1)	–0.5 to 4.0	V
T_{STG}(3)	Storage Temperature (ambient)	–65 to +150	°C
T_J	Junction Temperature	+150	°C

Notes:
1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easiest to achieve. During transitions, the device pins may undershoot to –2.0v or overshoot to +4.5V, provided this over or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
2. Valid over commercial temperature range.
3. For soldering guidelines and thermal considerations, see the Device Packaging information on the Xilinx website. For Pb free packages, see XAPP427.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply voltage for internal logic and input buffers	Commercial T_A = 0°C to +70°C	1.7	1.9	V
		Industrial T_A = –40°C to +85°C	1.7	1.9	V
V_{CCIO}	Supply voltage for output drivers @ 3.3V operation		3.0	3.6	V
	Supply voltage for output drivers @ 2.5V operation		2.3	2.7	V
	Supply voltage for output drivers @ 1.8V operation		1.7	1.9	V
	Supply voltage for output drivers @ 1.5V operation		1.4	1.6	V
V_{CCAUX}	JTAG programming		1.7	3.6	V

DC Electrical Characteristics (Over Recommended Operating Conditions)

Symbol	Parameter	Test Conditions	Typical	Max.	Units
I_{CCSB}	Standby current Commercial	V_{CC} = 1.9V, V_{CCIO} = 3.6V	50	240	µA
I_{CCSB}	Standby current Industrial	V_{CC} = 1.9V, V_{CCIO} = 3.6V	150	400	µA
I_{CC} (1)	Dynamic current	f = 1 MHz	-	1	mA
		f = 50 MHz	-	55	mA
C_{JTAG}	JTAG input capacitance	f = 1 MHz	-	10	pF
C_{CLK}	Global clock input capacitance	f = 1 MHz	-	12	pF
C_{IO}	I/O capacitance	f = 1 MHz	-	10	pF
I_{IL}(2)	Input leakage current	V_{IN} = 0V or V_{CCIO} to 3.9V	-	+/–1	µA
I_{IH}(2)	I/O High-Z leakage	V_{IN} = 0V or V_{CCIO} to 3.9V	-	+/–1	µA

Notes:
1. 16-bit up/down, Resetable binary counter (one counter per function block) tested at V_{CC}= V_{CCIO} = 1.9V.
2. See Quality and Reliability section of the CoolRunner-II family data sheet.

LVCMOS 3.3V and LVTTL 3.3V DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage	-	3.0	3.6	V
V_{IH}	High level input voltage	-	2	3.9	V
V_{IL}	Low level input voltage	-	–0.3	0.8	V
V_{OH}	High level output voltage	I_{OH} = –8 mA, V_{CCIO} = 3V	V_{CCIO} – 0.4V	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 3V	V_{CCIO} – 0.2V	-	V
V_{OL}	Low level output voltage	I_{OL} = 8 mA, V_{CCIO} = 3V	-	0.4	V
		I_{OL} = 0.1 mA, V_{CCIO} = 3V	-	0.2	V

LVCMOS 2.5V DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage	-	2.3	2.7	V
V_{IH}	High level input voltage	-	1.7	V_{CCIO} + 0.3(1))	V
V_{IL}	Low level input voltage	-	–0.3	0.7	V
V_{OH}	High level output voltage	I_{OH} = –8 mA, V_{CCIO} = 2.3V	V_{CCIO} – 0.4V	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 2.3V	V_{CCIO} – 0.2V	-	V
V_{OL}	Low level output voltage	I_{OL} = 8 mA, V_{CCIO} = 2.3V	-	0.4	V
		I_{OL} = 0.1mA, V_{CCIO} = 2.3V	-	0.2	V

(1) The V_{IH} Max value represents the JEDEC specification for LVCMOS25. The CoolRunner-II input buffer can tolerate up to 3.9V without physical damage.

LVCMOS 1.8V DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage	-	1.7	1.9	V
V_{IH}	High level input voltage	-	0.65 x V_{CCIO}	V_{CCIO} + 0.3(1)	V
V_{IL}	Low level input voltage	-	–0.3	0.35 x V_{CCIO}	V
V_{OH}	High level output voltage	I_{OH} = –8 mA, V_{CCIO} = 1.7V	V_{CCIO} – 0.45	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 1.7V	V_{CCIO} – 0.2	-	V
V_{OL}	Low level output voltage	I_{OL} = 8 mA, V_{CCIO} = 1.7V	-	0.45	V
		I_{OL} = 0.1 mA, V_{CCIO} = 1.7V	-	0.2	V

(1) The V_{IH} Max value represents the JEDEC specification for LVCMOS18. The CoolRunner-II input buffer can tolerate up to 3.9V without physical damage.

LVCMOS 1.5V DC Voltage Specifications(1)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage	-	1.4	1.6	V
V_{IH}	High level input voltage	-	0.5 x V_{CCIO}	0.8 x V_{CCIO}	V
V_{IL}	Low level input voltage	-	0.2 x V_{CCIO}	0.5 x V_{CCIO}	V

HSTL1 DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Units
V_{CCIO}	Input source voltage		1.4	1.5	1.6	V
V_{REF}(1)	Input reference voltage		0.68	0.75	0.90	V
V_{TT}(2)	Termination voltage		-	V_{CCIO} x 0.5	-	V
V_{IH}	High level input voltage		V_{REF} + 0.1	-	1.9	V
V_{IL}	Low level input voltage		–0.3	-	V_{REF} – 0.1	V
V_{OH}	High level output voltage	I_{OH} = –8 mA, V_{CCIO} = 1.7V	V_{CCIO} – 0.4	-	-	V
V_{OL}	Low level output voltage	I_{OL} = 8 mA, V_{CCIO} = 1.7V	-	-	0.4	V

Notes:
1. V_{REF} should track the variations in V_{CCIO}, also peak-to-peak AC noise on V_{REF} may not exceed ±2% V_{REF}
2. V_{TT} of transmitting device must track V_{REF} of receiving devices

AC Electrical Characteristics Over Recommended Operating Conditions

Symbol	Parameter	-7		-10		Units
		Min.	Max.	Min.	Max.	
T_{PD1}	Propagation delay (single p-term)	-	7.1	-	9.2	ns
T_{PD2}	Propagation delay (OR array)	-	7.5	-	10.0	ns
T_{SUD}	Direct input register set-up time	3.4	-	4.0	-	ns
T_{SU1}	Setup time fast (single p-term)	2.6	-	3.1	-	ns
T_{SU2}	Setup time (OR array)	3.0	-	3.9	-	ns
T_H	Direct input register hold time	0	-	0	-	ns
T_H	P-term hold time	0	-	0	-	ns
T_{CO}	Clock to output	-	5.8	-	7.9	ns
F_{TOGGLE}(1)	Internal toggle rate	-	250	-	166	MHz
$F_{SYSTEM1}$(2)	Maximum system frequency	-	179	-	128	MHz
$F_{SYSTEM2}$(2)	Maximum system frequency	-	167	-	116	MHz
F_{EXT1}(3)	Maximum external frequency	-	119	-	91	MHz
F_{EXT2}(3)	Maximum external frequency	-	114	-	85	MHz
T_{PSUD}	Direct input register p-term clock setup time	2.1	-	2.8	-	ns
T_{PSU1}	P-term clock setup time (single p-term)	1.1	-	1.7	-	ns
T_{PSU2}	P-term clock setup time (OR array)	1.5	-	2.5	-	ns
T_{PHD}	Direct input register p-term clock hold time	0.1	-	0.4	-	ns
T_{PH}	P-term clock hold	1.3	-	1.7	-	ns
T_{PCO}	P-term clock to output	-	7.3	-	9.3	ns
T_{OE}/T_{OD}	Global OE to output enable/disable	-	6.5	-	9.2	ns
T_{POE}/T_{POD}	P-term OE to output enable/disable	-	7.5	-	10.2	ns
T_{MOE}/T_{MOD}	Macrocell driven OE to output enable/disable	-	8.6	-	12.5	ns
T_{PAO}	P-term set/reset to output valid	-	7.6	-	11.6	ns
T_{AO}	Global set/reset to output valid	-	7.5	-	11.5	ns
T_{SUEC}	Register clock enable setup time	2.8	-	3.2	-	ns
T_{HEC}	Register clock enable hold time	0	-	0	-	ns
T_{CW}	Global clock pulse width High or Low	2.0	-	3.0	-	ns
T_{PCW}	P-term pulse width High or Low	7.5	-	10.0	-	ns
T_{APRPW}	Asynchronous preset/reset pulse width (High or Low)	7.5	-	10.0	-	ns
T_{DGSU}	Set-up before DataGATE latch assertion	0.0	-	0.0	-	ns
T_{DGH}	Hold to DataGATE latch assertion	4.0	-	6.0	-	ns
T_{DGR}	DataGATE recovery to new data	-	9.3	-	11.0	ns
T_{DGW}	DataGATE low pulse width	3.0	-	5.0	-	ns
T_{CDRSU}	CDRST setup time before falling edge GCLK2	1.7	-	2.5	-	ns
T_{CDRH}	Hold time CDRST after falling edge GCLK2	0	-	0	-	ns
T_{CONFIG}(4)	Configuration time	-	400	-	400	µs

Notes:

1. F_{TOGGLE} is the maximum clock frequency to which a T-Flip Flop can reliably toggle (see the CoolRunner-II family data sheet for more information).
2. $F_{SYSTEM1}$ ($1/T_{CYCLE}$) is the internal operating frequency for a device fully populated with 16-bit Resetable binary counter through one p-term per macrocell while $F_{SYSTEM2}$ is through the OR array.
3. $F_{EXT1}(1/T_{SU1}+T_{CO})$ is the maximum external frequency using one p-term while F_{EXT2} is through the OR array
4. Typical configuration current during T_{CONFIG} is approximately 15mA

Internal Timing Parameters(1)

Symbol	Parameter(1)	-7		-10		Units
		Min.	Max.	Min.	Max.	
Buffer Delays						
T_{IN}	Input buffer delay	-	3.1	-	3.8	ns
T_{DIN}	Direct data register input delay	-	4.4	-	5.5	ns
T_{GCK}	Global Clock buffer delay	-	2.4	-	3.3	ns
T_{GSR}	Global set/reset buffer delay	-	3.8	-	4.6	ns
T_{GTS}	Global 3-state buffer delay	-	2.9	-	3.7	ns
T_{OUT}	Output buffer delay	-	3.0	-	3.9	ns
T_{EN}	Output buffer enable/disable delay	-	3.6	-	5.5	ns
P-term Delays						
T_{CT}	Control term delay	-	0.8	-	0.9	ns
T_{LOGI1}	Single P-term delay adder	-	0.5	-	0.8	ns
T_{LOGI2}	Multiple P-term delay adder	-	0.4	-	0.8	ns
Macrocell Delay						
T_{PDI}	Input to output valid	-	0.5	-	0.7	ns
T_{SUI}	Setup before clock	1.4	-	1.8	-	ns
T_{HI}	Hold after clock	0	-	0	-	ns
T_{ECSU}	Enable clock setup time	1.3	-	1.8	-	ns
T_{ECHO}	Enable clock hold time	0	-	0	-	ns
T_{COI}	Clock to output valid	-	0.4	-	0.7	ns
T_{AOI}	Set/reset to output valid	-	0.7	-	3.0	ns
T_{CDBL}	Clock doubler delay	-	0	-	0	ns
Feedback Delays						
T_{F}	Feedback delay	-	3.3	-	4.5	ns
T_{OEM}	Macrocell to global OE delay	-	2.2	-	3.0	ns
I/O Standard Time Adder Delays 1.5V CMOS						
T_{HYS15}	Hysteresis input adder	-	3.0	-	4.0	ns
T_{OUT15}	Output adder	-	0.8	-	1.0	ns
T_{SLEW15}	Output slew rate adder	-	3.0	-	4.0	ns
I/O Standard Time Adder Delays 1.8V CMOS						
T_{HYS18}	Hysteresis input adder	-	2.0	-	3.0	ns
T_{OUT18}	Output adder	-	0	-	0	ns
T_{SLEW18}	Output slew rate adder	-	2.5	-	4.0	ns

Internal Timing Parameters(1) *(Continued)*

Symbol	Parameter(1)	-7		-10		Units
		Min.	Max.	Min.	Max.	
I/O Standard Time Adder Delays 2.5V CMOS						
T_{IN25}	Standard input adder	-	0.6	-	1.0	ns
T_{HYS25}	Hysteresis input adder	-	1.5	-	3.0	ns
T_{OUT25}	Output adder	-	0.8	-	2.0	ns
T_{SLEW25}	Output slew rate adder	-	3.0	-	4.0	ns
I/O Standard Time Adder Delays 3.3V CMOS/TTL						
T_{IN33}	Standard input adder	-	0.5	-	2.0	ns
T_{HYS33}	Hysteresis input adder	-	1.2	-	3.0	ns
T_{OUT33}	Output adder	-	1.2	-	3.0	ns
T_{SLEW33}	Output slew rate adder	-	3.0	-	4.0	ns
I/O Standard Time Adder Delays HSTL, SSTL						
SSTL2-1	Input adder to T_{IN}, T_{DIN}, T_{GCK}, T_{GSR},T_{GTS}	-	0.4	-	1.0	ns
	Output adder to T_{OUT}	-	-0.5	-	0.0	ns
SSTL3-1	Input adder to T_{IN}, T_{DIN}, T_{GCK}, T_{GSR},T_{GTS}	-	0.6	-	1.0	ns
	Output adder to T_{OUT}	-	0.0	-	0.0	ns
HSTL-1	Input adder to T_{IN}, T_{DIN}, T_{GCK}, T_{GSR},T_{GTS}	-	0.8	-	1.0	ns
	Output adder to T_{OUT}	-	0.0	-	0.0	ns

Notes:
1. 1.5 ns input pin signal rise/fall.

Switching Characteristics

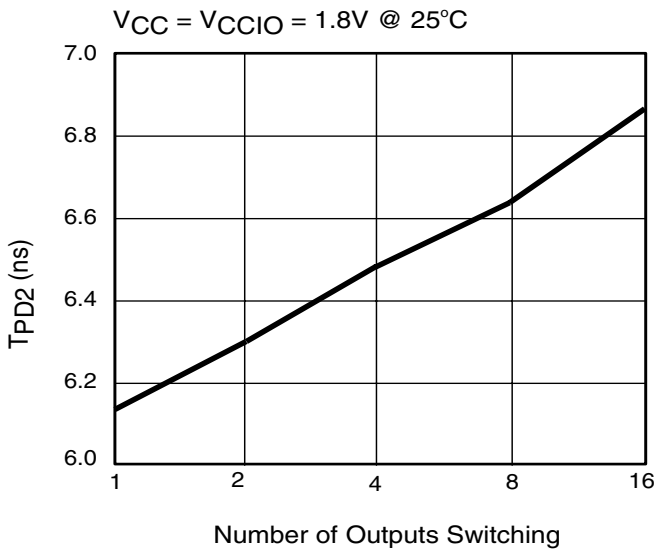
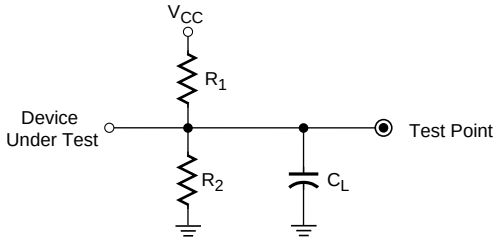


Figure 2: **Derating Curve for T_{PD}**

AC Test Circuit



Output Type	R_1	R_2	C_L
LVTTL33	268Ω	235Ω	35 pF
LVCMOS33	275Ω	275Ω	35 pF
LVCMOS25	188Ω	188Ω	35pF
LVCMOS18	112.5Ω	112.5Ω	35pF
LVCMOS15	150Ω	150Ω	35pF

C_L includes test fixtures and probe capacitance.
1.5 nsec maximum rise/fall times on inputs.

DS_ACT_08_14_02

Figure 3: **Load Circuit**

Typical I/O Output Curves

The I/V curve illustrates the nominal amount of current that an I/O can source/sink at different voltage levels.

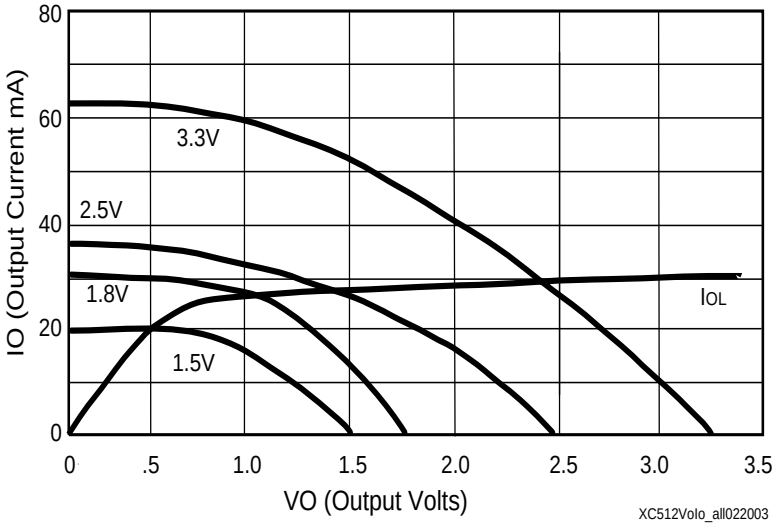


Figure 4: **Typical I/V Curves for XC2C512**

Pin Descriptions

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
1(GTS0)	1	7	D4	C1	2
1	2	6	B2	C2	2
1(GTS3)	3	5	E3	B1	2
1	4	4	C3	B2	2
1	5	-	-	-	-
1	6	-	-	-	-
1	7	-	-	-	-
1	8	-	-	-	-
1	9	-	-	-	-
1	10	-	-	-	-
1	11	-	-	-	-
1	12	-	-	-	-
1(GTS2)	13	3	D3	D3	2
1	14	2	B3	C3	2
1	15	208	B4	A1	2
1(GSR)	16	206	C4	A2	2
2	1	-	A1	D2	2
2	2	8	-	D1	2
2	3	-	D2	F4	2
2	4	-	-	F3	2
2	5	-	-	-	-
2	6	-	-	-	-
2	7	-	-	-	-
2	8	-	-	-	-
2	9	-	-	-	-
2	10	-	-	-	-
2	11	-	-	-	-
2	12	-	-	-	-
2	13	-	C2	E2	2
2(GTS1)	14	9	E5	E1	2
2	15	10	B1	F2	2
2	16	12	E4	G4	2

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
3	1	205	-	B3	2
3	2	-	A2	C4	2
3	3	203	-	B4	2
3	4	-	C5	C5	2
3	5	202	A3	B5	2
3	6	-	-	-	-
3	7	-	-	-	-
3	8	-	-	-	-
3	9	-	-	-	-
3	10	-	-	-	-
3	11	-	-	-	-
3	12	-	-	-	-
3	13	201	E7	A3	2
3	14	-	A4	A4	2
3	15	200	C6	D6	2
3	16	199	B5	A5	2
4	1	-	C1	G3	2
4	2	14	E2	G2	2
4	3	-	F2	G1	2
4	4	15	E6	H4	2
4	5	-	-	-	-
4	6	-	-	-	-
4	7	-	-	-	-
4	8	-	-	-	-
4	9	-	-	-	-
4	10	-	-	-	-
4	11	-	-	-	-
4	12	-	-	-	-
4	13	-	F3	H3	2
4	14	16	D1	H2	2
4	15	17	G4	H1	2
4	16	18	E1	J4	2

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
5	1	198	D6	C6	2
5	2	197	A5	B6	2
5	3	196	E8	A6	2
5	4	195	B6	D7	2
5	5	194	C7	C7	2
5	6	-	-	-	-
5	7	-	-	-	-
5	8	-	-	-	-
5	9	-	-	-	-
5	10	-	-	-	-
5	11	-	-	-	-
5	12	-	-	-	-
5	13	193	-	B7	2
5	14	-	A6	A7	2
5	15	192	D7	D8	2
5	16	-	B7	C8	2
6	1	19	G3	J3	2
6	2	20	G2	J2	2
6	3	21	-	J1	2
6	4	-	F5	K4	2
6	5	-	-	-	-
6	6	-	-	-	-
6	7	-	-	-	-
6	8	-	-	-	-
6	9	-	-	-	-
6	10	-	-	-	-
6	11	-	-	-	-
6	12	-	-	-	-
6	13	-	-	K3	2
6	14	-	F1	K2	2
6	15	-	-	K1	2
6	16	-	G5	L1	2

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
7	1	191	-	B8	2
7	2	-	E9	A8	2
7	3	189	A7	D9	2
7	4	188	D8	C9	2
7	5	187	B8	B9	2
7	6	-	-	-	-
7	7	-	-	-	-
7	8	-	-	-	-
7	9	-	-	-	-
7	10	-	-	-	-
7	11	-	-	-	-
7	12	-	-	-	-
7	13	186	C8	A9	2
7	14	185	A8	D10	2
7	15	184	E11	C10	2
7	16	183	E10	B10	2
8	1	-	H2	L4	2
8	2	22	-	L3	2
8	3	23	H4	L2	2
8	4	-	-	M1	2
8	5	-	-	-	-
8	6	-	-	-	-
8	7	-	-	-	-
8	8	-	-	-	-
8	9	-	-	-	-
8	10	-	-	-	-
8	11	-	-	-	-
8	12	-	-	-	-
8	13	-	G1	M2	2
8	14	25	H3	M3	2
8	15	-	H1	M4	2
8	16	-	H5	N1	2

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
9	1	-	-	AA2	1
9	2	50	N3	AB1	1
9	3	49	-	AA1	1
9	4	48	-	W4	1
9	5	-	-	-	-
9	6	-	-	-	-
9	7	-	-	-	-
9	8	-	-	-	-
9	9	-	-	-	-
9	10	-	-	-	-
9	11	-	-	-	-
9	12	-	-	-	-
9	13	-	R1	Y3	1
9	14	47	N4	Y2	1
9	15	-	N2	W3	1
9(GCK1)	16	46	M3	Y1	1
10(CDRST)	1	51	P2	AB2	1
10	2	54	P4	Y4	1
10(GCK2)	3	55	P5	AB3	1
10	4	56	R2	AA4	1
10	5	-	-	-	-
10	6	-	-	-	-
10	7	-	-	-	-
10	8	-	-	-	-
10	9	-	-	-	-
10	10	-	-	-	-
10	11	-	-	-	-
10	12	-	-	-	-
10	13	57	T1	Y5	1
10(DGE)	14	58	T2	AA5	1
10	15	-	-	AB4	1
10	16	-	N5	W6	1

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
11	1	45	P1	W2	1
11	2	-	M4	W1	1
11(GCK0)	3	44	M2	V3	1
11	4	43	L3	U4	1
11	5	-	-	-	-
11	6	-	-	-	-
11	7	-	-	-	-
11	8	-	-	-	-
11	9	-	-	-	-
11	10	-	-	-	-
11	11	-	-	-	-
11	12	-	-	-	-
11	13	41	N1	V2	1
11	14	40	L4	V1	1
11	15	39	M1	U3	1
11	16	38	L5	U2	1
12	1	60	R4	AB5	1
12	2	61	M5	Y6	1
12	3	62	R5	AA6	1
12	4	63	R6	AB6	1
12	5	64	-	W7	1
12	6	-	-	-	-
12	7	-	-	-	-
12	8	-	-	-	-
12	9	-	-	-	-
12	10	-	-	-	-
12	11	-	-	-	-
12	12	-	-	-	-
12	13	65	N6	Y7	1
12	14	66	-	AA7	1
12	15	67	R3	AB7	1
12	16	-	-	W8	1

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
13	1	37	-	U1	1
13	2	-	K4	T4	1
13	3	36	L2	T3	1
13	4	35	-	T2	1
13	5	-	-	-	-
13	6	-	-	-	-
13	7	-	-	-	-
13	8	-	-	-	-
13	9	-	-	-	-
13	10	-	-	-	-
13	11	-	-	-	-
13	12	-	-	-	-
13	13	-	K3	T1	1
13	14	34	L1	R4	1
13	15	32	K5	R3	1
13	16	-	K2	R2	1
14	1	-	M6	Y8	1
14	2	-	-	AA8	1
14	3	69	T3	AB8	1
14	4	70	P6	W9	1
14	5	71	T4	Y9	1
14	6	-	-	-	-
14	7	-	-	-	-
14	8	-	-	-	-
14	9	-	-	-	-
14	10	-	-	-	-
14	11	-	-	-	-
14	12	-	-	-	-
14	13	72	P7	AA9	1
14	14	-	-	AB9	1
14	15	73	T5	W10	1
14	16	-	-	Y10	1

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
15	1	31	J4	R1	1
15	2	-	K1	P4	1
15	3	30	J3	P3	1
15	4	29	J2	P2	1
15	5	-	-	-	-
15	6	-	-	-	-
15	7	-	-	-	-
15	8	-	-	-	-
15	9	-	-	-	-
15	10	-	-	-	-
15	11	-	-	-	-
15	12	-	-	-	-
15	13	28	J5	P1	1
15	14	27	J1	N4	1
15	15	-	-	N3	1
15	16	-	-	N2	1
16	1	74	N7	AA10	1
16	2	-	-	AB10	1
16	3	75	R7	AB11	1
16	4	76	M7	W11	1
16	5	77	T6	AA11	1
16	6	-	-	-	-
16	7	-	-	-	-
16	8	-	-	-	-
16	9	-	-	-	-
16	10	-	-	-	-
16	11	-	-	-	-
16	12	-	-	-	-
16	13	-	-	Y11	1
16	14	78	-	AB12	1
16	15	-	-	AA12	1
16	16	-	-	Y12	1

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
17	1	161	A16	A21	4
17	2	162	B13	B20	4
17	3	163	-	C19	4
17	4	164	-	B19	4
17	5	165	B14	C18	4
17	6	-	-	-	-
17	7	-	-	-	-
17	8	-	-	-	-
17	9	-	-	-	-
17	10	-	-	-	-
17	11	-	-	-	-
17	12	-	-	-	-
17	13	166	C13	B18	4
17	14	167	A15	A19	4
17	15	168	C12	D17	4
17	16	169	B12	A18	4
18	1	160	B15	A22	4
18	2	-	C14	B21	4
18	3	-	G11	B22	4
18	4	159	B16	C20	4
18	5	-	-	-	-
18	6	-	-	-	-
18	7	-	-	-	-
18	8	-	-	-	-
18	9	-	-	-	-
18	10	-	-	-	-
18	11	-	-	-	-
18	12	-	-	-	-
18	13	-	-	C21	4
18	14	-	D14	D19	4
18	15	158	-	D20	4
18	16	-	C15	C22	4

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
19	1	170	D13	C17	4
19	2	171	A14	B17	4
19	3	173	E13	A17	4
19	4	-	A13	D16	4
19	5	-	C11	C16	4
19	6	-	-	-	-
19	7	-	-	-	-
19	8	-	-	-	-
19	9	-	-	-	-
19	10	-	-	-	-
19	11	-	-	-	-
19	12	-	-	-	-
19	13	-	A12	B16	4
19	14	-	B11	A16	4
19	15	-	D11	D15	4
19	16	-	A11	C15	4
20	1	-	G12	D21	4
20	2	-	D15	D22	4
20	3	155	E14	E20	4
20	4	154	C16	F19	4
20	5	-	-	-	-
20	6	-	-	-	-
20	7	-	-	-	-
20	8	-	-	-	-
20	9	-	-	-	-
20	10	-	-	-	-
20	11	-	-	-	-
20	12	-	-	-	-
20	13	153	F14	E21	4
20	14	152	D16	E22	4
20	15	151	F13	F20	4
20	16	150	E15	F21	4

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
21	1	-	D10	B15	4
21	2	174	B10	A15	4
21	3	175	E12	D14	4
21	4	-	F12	B14	4
21	5	178	-	A14	4
21	6	-	-	-	-
21	7	-	-	-	-
21	8	-	-	-	-
21	9	-	-	-	-
21	10	-	-	-	-
21	11	-	-	-	-
21	12	-	-	-	-
21	13	-	-	D13	4
21	14	-	-	C13	4
21	15	-	-	B13	4
21	16	-	-	A13	4
22	1	149	G13	F22	4
22	2	148	F15	G19	4
22	3	147	G14	G20	4
22	4	146	E16	G21	4
22	5	-	-	-	-
22	6	-	-	-	-
22	7	-	-	-	-
22	8	-	-	-	-
22	9	-	-	-	-
22	10	-	-	-	-
22	11	-	-	-	-
22	12	-	-	-	-
22	13	145	H12	G22	4
22	14	144	F16	H19	4
22	15	143	H16	H20	4
22	16	142	-	H21	4

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
23	1	179	B9	A12	4
23	2	180	-	D12	4
23	3	-	C9	B12	4
23	4	182	-	C12	4
23	5	-	C10	A11	4
23	6	-	-	-	-
23	7	-	-	-	-
23	8	-	-	-	-
23	9	-	-	-	-
23	10	-	-	-	-
23	11	-	-	-	-
23	12	-	-	-	-
23	13	-	-	B11	4
23	14	-	A9	C11	4
23	15	-	-	D11	4
23	16	-	D9	A10	4
24	1	140	G15	H22	4
24	2	139	H13	J19	4
24	3	138	G16	J20	4
24	4	137	H14	J21	4
24	5	-	-	-	-
24	6	-	-	-	-
24	7	-	-	-	-
24	8	-	-	-	-
24	9	-	-	-	-
24	10	-	-	-	-
24	11	-	-	-	-
24	12	-	-	-	-
24	13	136	H15	J22	4
24	14	135	J12	K19	4
24	15	134	K12	K20	4
24	16	-	J16	K21	4

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
25	1	110	R16	W22	3
25	2	111	N15	V20	3
25	3	112	M15	V21	3
25	4	113	M13	U19	3
25	5	-	-	-	-
25	6	-	-	-	-
25	7	-	-	-	-
25	8	-	-	-	-
25	9	-	-	-	-
25	10	-	-	-	-
25	11	-	-	-	-
25	12	-	-	-	-
25	13	114	P16	V22	3
25	14	115	N16	U20	3
25	15	116	L14	U21	3
25	16	117	M14	U22	3
26	1	109	N14	Y22	3
26	2	108	T16	W21	3
26	3	107	R15	W20	3
26	4	106	P15	Y21	3
26	5	-	P14	Y20	3
26	6	-	-	-	-
26	7	-	-	-	-
26	8	-	-	-	-
26	9	-	-	-	-
26	10	-	-	-	-
26	11	-	-	-	-
26	12	-	-	-	-
26	13	103	P13	AA22	3
26	14	102	R13	AB22	3
26	15	101	N13	AA21	3
26	16	100	R14	AB21	3

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
27	1	118	L15	T19	3
27	2	-	L13	T20	3
27	3	119	M12	T21	3
27	4	120	M16	T22	3
27	5	-	-	-	-
27	6	-	-	-	-
27	7	-	-	-	-
27	8	-	-	-	-
27	9	-	-	-	-
27	10	-	-	-	-
27	11	-	-	-	-
27	12	-	-	-	-
27	13	-	K14	R19	3
27	14	-	-	R20	3
27	15	121	-	R21	3
27	16	-	-	R22	3
28	1	99	T15	W19	3
28	2	97	R12	AA20	3
28	3	95	T14	Y18	3
28	4	-	N11	AA19	3
28	5	-	P11	W17	3
28	6	-	-	-	-
28	7	-	-	-	-
28	8	-	-	-	-
28	9	-	-	-	-
28	10	-	-	-	-
28	11	-	-	-	-
28	12	-	-	-	-
28	13	-	M11	Y17	3
28	14	-	T13	AA18	3
28	15	-	N10	AB18	3
28	16	-	-	AA17	3

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
29	1	-	L16	P19	3
29	2	-	-	P20	3
29	3	122	-	P21	3
29	4	123	-	P22	3
29	5	-	-	-	-
29	6	-	-	-	-
29	7	-	-	-	-
29	8	-	-	-	-
29	9	-	-	-	-
29	10	-	-	-	-
29	11	-	-	-	-
29	12	-	-	-	-
29	13	-	-	N19	3
29	14	125	K15	N21	3
29	15	-	L12	N22	3
29	16	-	-	M22	3
30	1	-	-	AB17	3
30	2	91	T12	W16	3
30	3	90	P10	Y16	3
30	4	89	T11	AA16	3
30	5	-	R10	AB16	3
30	6	-	-	-	-
30	7	-	-	-	-
30	8	-	-	-	-
30	9	-	-	-	-
30	10	-	-	-	-
30	11	-	-	-	-
30	12	-	-	-	-
30	13	88	M10	W15	3
30	14	87	T10	Y15	3
30	15	-	M9	AA15	3
30	16	86	R9	AB15	3

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
31	1	126	K16	M19	3
31	2	-	-	M20	3
31	3	127	-	M21	3
31	4	128	J14	L22	3
31	5	-	-	-	-
31	6	-	-	-	-
31	7	-	-	-	-
31	8	-	-	-	-
31	9	-	-	-	-
31	10	-	-	-	-
31	11	-	-	-	-
31	12	-	-	-	-
31	13	-	-	L21	3
31	14	-	J15	L20	3
31	15	-	-	L19	3
31	16	131	J13	K22	3
32	1	85	P9	W14	3
32	2	84	N9	Y14	3
32	3	-	T9	AA14	3
32	4	83	M8	AB14	3
32	5	-	T8	W13	3
32	6	-	-	-	-
32	7	-	-	-	-
32	8	-	-	-	-
32	9	-	-	-	-
32	10	-	-	-	-
32	11	-	-	-	-
32	12	-	-	-	-
32	13	82	P8	Y13	3
32	14	80	R8	AA13	3
32	15	-	T7	AB13	3
32	16	-	N8	W12	3

Notes:

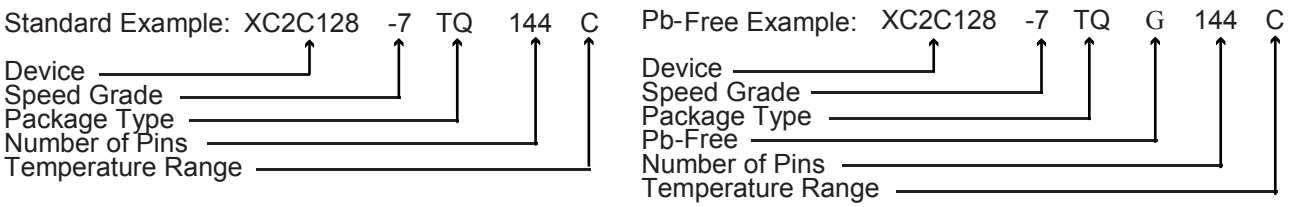
1. GTS = global output enable, GSR = global reset/set, GCK = global clock, CDRST = clock divide reset, DGE = DataGATE enable.
2. GCK, GSR, and GTS pins can also be used for general purpose I/O.

Ordering Information

Part Number	Pin/Ball Spacing	θ_{JA} (C/Watt)	θ_{JC} (C/Watt)	Package Type	Package Body Dimensions	I/O	Commercial (C) Industrial (I)[1]
XC2C512-7PQ208C	0.5mm	35.1	7.2	Plastic Quad Flat Pack	28mm x 28mm	173	C
XC2C512-10PQ208C	0.5mm	35.1	7.2	Plastic Quad Flat Pack	28mm x 28mm	173	C
XC2C512-7FT256C	1.0mm	32.2	4.9	Fine Pitch Thin BGA	17mm x 17mm	212	C
XC2C512-7FT256I	1.0mm	32.2	4.9	Fine Pitch Thin BGA	17mm x 17mm	212	I
XC2C512-10FT256C	1.0mm	32.2	4.9	Fine Pitch Thin BGA	17mm x 17mm	212	C
XC2C512-7FG324C	1.0mm	39.1	5.0	Fine Pitch BGA	23mm x 23mm	270	C
XC2C512-10FG324C	1.0mm	39.1	5.0	Fine Pitch BGA	23mm x 23mm	270	C
XC2C512-7PQG208C	0.5mm	35.1	7.2	Plastic Quad Flat Pack; Pb-free	28mm x 28mm	173	C
XC2C512-10PQG208C	0.5mm	35.1	7.2	Plastic Quad Flat Pack; Pb-free	28mm x 28mm	173	C
XC2C512-7FTG256C	1.0mm	32.2	4.9	Fine Pitch Thin BGA; Pb-free	17mm x 17mm	212	C
XC2C512-7FTG256I	1.0mm	32.2	4.9	Fine Pitch Thin BGA; Pb-free	17mm x 17mm	212	I
XC2C512-10FTG256C	1.0mm	32.2	4.9	Fine Pitch Thin BGA; Pb-free	17mm x 17mm	212	C
XC2C512-7FGG324C	1.0mm	39.1	5.0	Fine Pitch BGA; Pb-free	23mm x 23mm	270	C
XC2C512-10FGG324C	1.0mm	39.1	5.0	Fine Pitch BGA; Pb-free	23mm x 23mm	270	C
XC2C512-10PQ208I	0.5mm	35.1	7.2	Plastic Quad Flat Pack	28mm x 28mm	173	I
XC2C512-10FT256I	1.0mm	32.2	4.9	Fine Pitch Thin BGA	17mm x 17mm	212	I
XC2C512-10FG324I	1.0mm	39.1	5.0	Fine Pitch BGA	23mm x 23mm	270	I
XC2C512-10PQG208I	0.5mm	35.1	7.2	Plastic Quad Flat Pack; Pb-free	28mm x 28mm	173	I
XC2C512-10FTG256I	1.0mm	32.2	4.9	Fine Pitch Thin BGA; Pb-free	17mm x 17mm	212	I
XC2C512-10FGG324I	1.0mm	39.1	5.0	Fine Pitch BGA; Pb-free	23mm x 23mm	270	I

Notes:

1. C = Commercial (T_A = 0°C to +70° C); I = Industrial (T_A = –40°C to +85°C)..



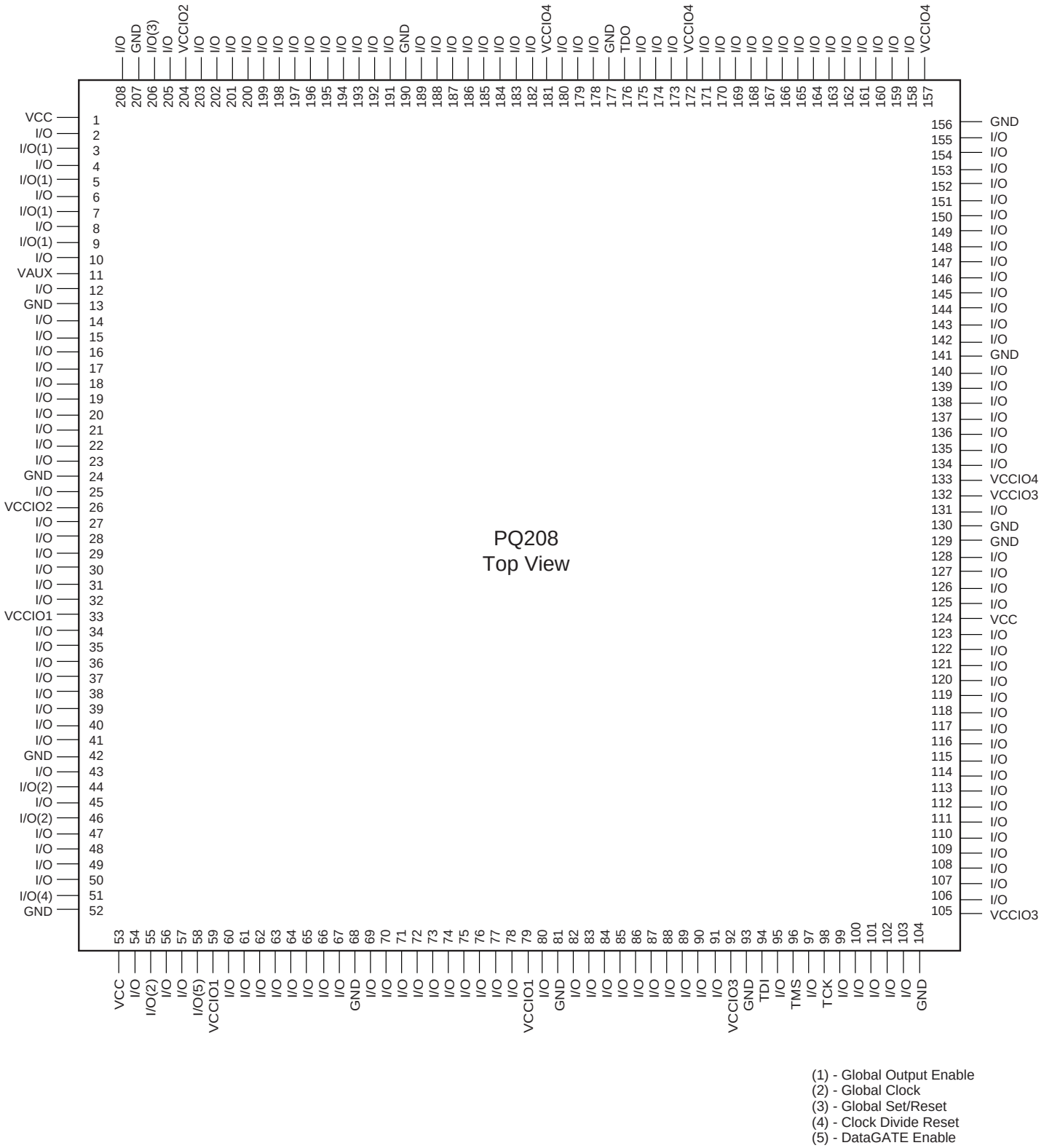


Figure 6: **PQ208 Plastic Quad Flat Pack**

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O	I/O	I/O	I/O	I/O	I/O	TDO	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	A
B	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	B
C	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O(3)	I/O	I/O	I/O	C
D	I/O	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O	I/O	I/O	VCC	I/O(1)	I/O(1)	I/O	I/O	D
E	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O(1)	I/O	I/O(1)	I/O	I/O	E
F	I/O	I/O	I/O	I/O	I/O	GND	VCCIO4	VCCIO4	VCCIO2	VCCIO2	GND	I/O	VAUX	I/O	I/O	I/O	F
G	I/O	I/O	I/O	I/O	I/O	I/O	GND	GND	GND	GND	VCCIO2	I/O	I/O	I/O	I/O	I/O	G
H	I/O	I/O	I/O	I/O	I/O	VCCIO4	GND	GND	GND	GND	VCCIO2	I/O	I/O	I/O	I/O	I/O	H
J	I/O	I/O	I/O	I/O	I/O	VCCIO3	GND	GND	GND	GND	VCCIO1	I/O	I/O	I/O	I/O	I/O	J
K	I/O	I/O	I/O	VCC	I/O	VCCIO3	GND	GND	GND	GND	VCCIO1	I/O	I/O	I/O	I/O	I/O	K
L	I/O	I/O	I/O	I/O	I/O	GND	VCCIO3	VCCIO3	VCCIO1	VCCIO1	GND	I/O	I/O	I/O	I/O	I/O	L
M	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O(2)	I/O(2)	I/O	M
N	I/O	I/O	I/O	I/O	TMS	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	N
P	I/O	I/O	I/O	I/O	TCK	I/O	I/O	I/O	I/O	I/O	I/O	I/O(2)	I/O	VCC	I/O(4)	I/O	P
R	I/O	I/O	I/O	I/O	I/O	TDI	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	R
T	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O(5)	I/O	T

FT256 Bottom View

(1) - Global Output Enable
(2) - Global Clock
(3) - Global Set/Reset
(4) - Clock Divide Reset
(5) - DataGATE Enable

Figure 7: **FT256 Fine Pitch Thin BGA**

Warranty Disclaimer

THESE PRODUCTS ARE SUBJECT TO THE TERMS OF THE XILINX LIMITED WARRANTY WHICH CAN BE VIEWED AT http://www.xilinx.com/warranty.htm. THIS LIMITED WARRANTY DOES NOT EXTEND TO ANY USE OF THE PRODUCTS IN AN APPLICATION OR ENVIRONMENT THAT IS NOT WITHIN THE SPECIFICATIONS STATED ON THE THEN-CURRENT XILINX DATA SHEET FOR THE PRODUCTS. PRODUCTS ARE NOT DESIGNED TO BE FAIL-SAFE AND ARE NOT WARRANTED FOR USE IN APPLICATIONS THAT POSE A RISK OF PHYSICAL HARM OR LOSS OF LIFE. USE OF PRODUCTS IN SUCH APPLICATIONS IS FULLY AT THE RISK OF CUSTOMER SUBJECT TO APPLICABLE LAWS AND REGULATIONS.

Additional Information

Additional information is available for the following CoolRunner-II topics:

- XAPP784: Bulletproof CPLD Design Practices
- XAPP375: Timing Model
- XAPP376: Logic Engine
- XAPP378: Advanced Features
- XAPP382: I/O Characteristics
- XAPP389: Powering CoolRunner-II
- XAPP399: Assigning VREF Pins

To access these and all application notes with their associated reference designs, click the following link and scroll down the page until you find the document you want:

CoolRunner-II Data Sheets and Application Notes

Device Packages

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
7/19/02	1.0	Initial Xilinx release.
3/15/03	2.0	Added characterization data.
11/25/03	2.1	Fixed two typos.
1/26/04	2.2	Updated Tsol; added links to Data Sheets and Application Notes.
8/03/04	2.3	Pb-free documentation
10/01/04	2.4	Add Asynchronous Preset/Reset Pulse Width specification to AC Electrical Characteristics.
01/30/05	2.5	Change to I_{CCSB} MAX for Commercial and Industrial.
03/07/05	2.6	Removed -6 speed grade. Modified Table 1, IOSTANDARDs.
03/20/06	3.0	Change to Product Specification. Add warranty Disclaimer. Add note to Pin Descriptions that GCK, GSR, and GTS pins can also be used for general purpose I/O.
02/15/07	3.1	Corrections to timing parameters t_{DIN}, t_{SUD}, t_{PSUD}, t_{PHD}, t_{PH}, t_{SLEW18}, t_{IN} (HSTL), t_{OUT}(SSTL3), and t_{Tin} (SSTL3) for -6 speed grade. Corrections to t_{DIN}, t_{SUD}, t_{CO}, t_{PSUD}, t_{PHD}, and t_{PH} for the -7 speed grade. Values now match the software. There were no changes to silicon or characterization. Added XC2C512-7FT256I and XC2C512-7FTG236I packages. Change to V_{IH} specification for 2.5V and 1.8V LVCMOS.
03/08/07	3.2	Fixed typo in note for V_{IL} for LVCMOS18; removed note for V_{IL} for LVCMOS33.