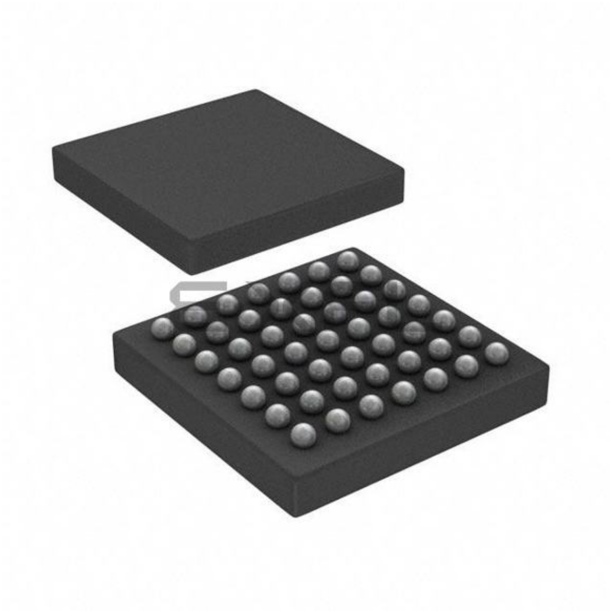

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	49-UFBGA, WLCSP
Supplier Device Package	49-WLCSP (3.29x3.26)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l072cby6tr

Figure 1. STM32L072xx block diagram

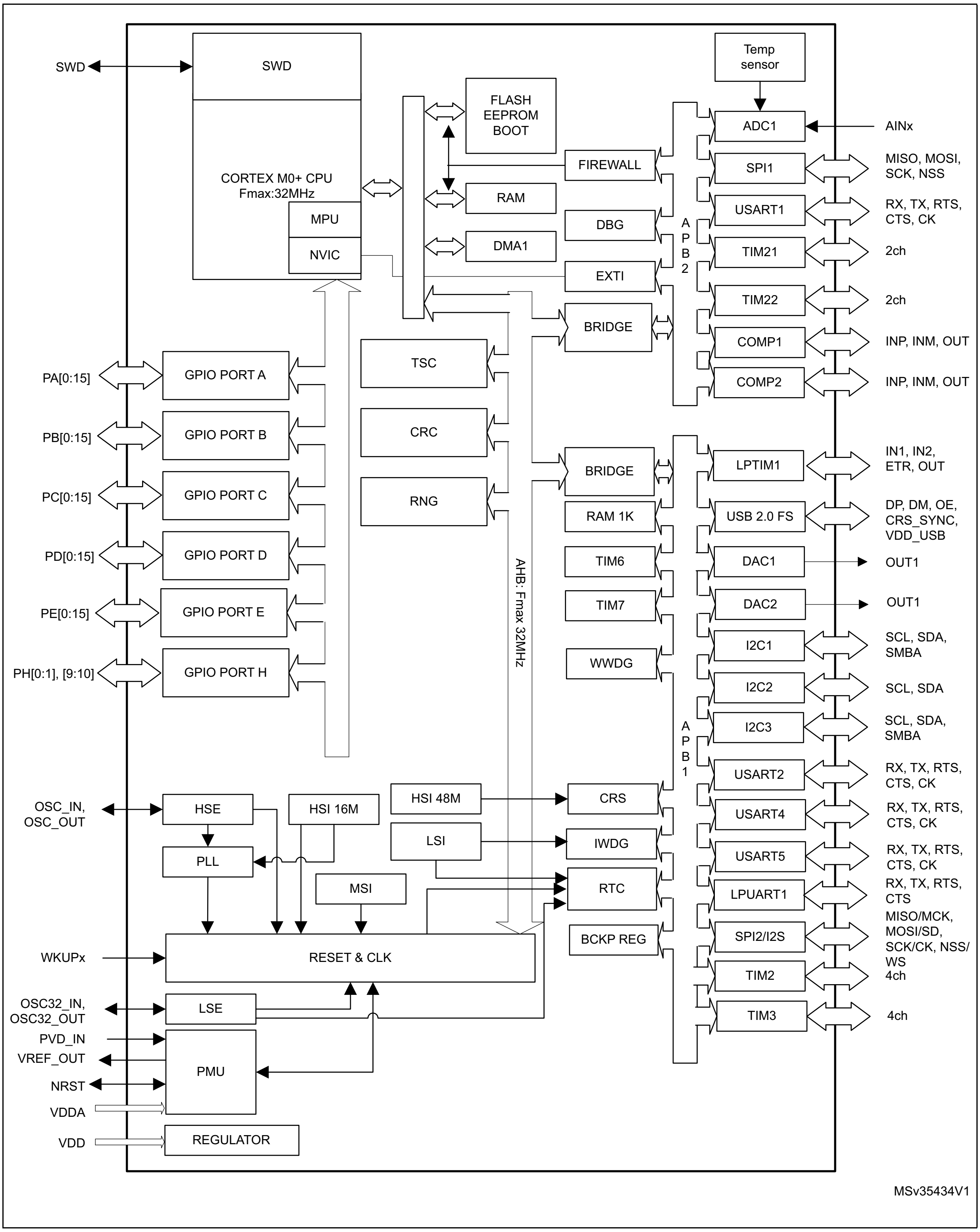


Table 5. Functionalities depending on the working mode (from Run/active down to standby) (1)(2)

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
CPU	Y	--	Y	--	--		--	
Flash memory	O	O	O	O	--		--	
RAM	Y	Y	Y	Y	Y		--	
Backup registers	Y	Y	Y	Y	Y		Y	
EEPROM	O	O	O	O	--		--	
Brown-out reset (BOR)	O	O	O	O	O	O	O	O
DMA	O	O	O	O	--		--	
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	-	
Power-on/down reset (POR/PDR)	Y	Y	Y	Y	Y	Y	Y	Y
High Speed Internal (HSI)	O	O	--	--	(3)		--	
High Speed External (HSE)	O	O	O	O	--		--	
Low Speed Internal (LSI)	O	O	O	O	O		O	
Low Speed External (LSE)	O	O	O	O	O		O	
Multi-Speed Internal (MSI)	O	O	Y	Y	--		--	
Inter-Connect Controller	Y	Y	Y	Y	Y		--	
RTC	O	O	O	O	O	O	O	
RTC Tamper	O	O	O	O	O	O	O	O
Auto WakeUp (AWU)	O	O	O	O	O	O	O	O
USB	O	O	--	--	--	O	--	
USART	O	O	O	O	O(4)	O	--	
LPUART	O	O	O	O	O(4)	O	--	
SPI	O	O	O	O	--		--	
I2C	O	O	O	O	O(5)	O	--	
ADC	O	O	--	--	--		--	
DAC	O	O	O	O	O		--	

3.4 Reset and supply management

3.4.1 Power supply schemes

- V_{DD} = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supplies for ADC reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{DD_USB} = 1.65 to 3.6V: external power supply for USB transceiver, USB_DM (PA11) and USB_DP (PA12). To guarantee a correct voltage level for USB communication V_{DD_USB} must be above 3.0V. If USB is not used this pin must be tied to V_{DD}.

3.4.2 Power supply supervisor

The devices have an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

Two versions are available:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the VDD min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The devices feature an embedded programmable voltage detector (PVD) that monitors the $V_{DD/VDDA}$ power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when $V_{DD/VDDA}$ drops below the V_{PVD} threshold and/or when $V_{DD/VDDA}$ is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

Figure 2. Clock tree

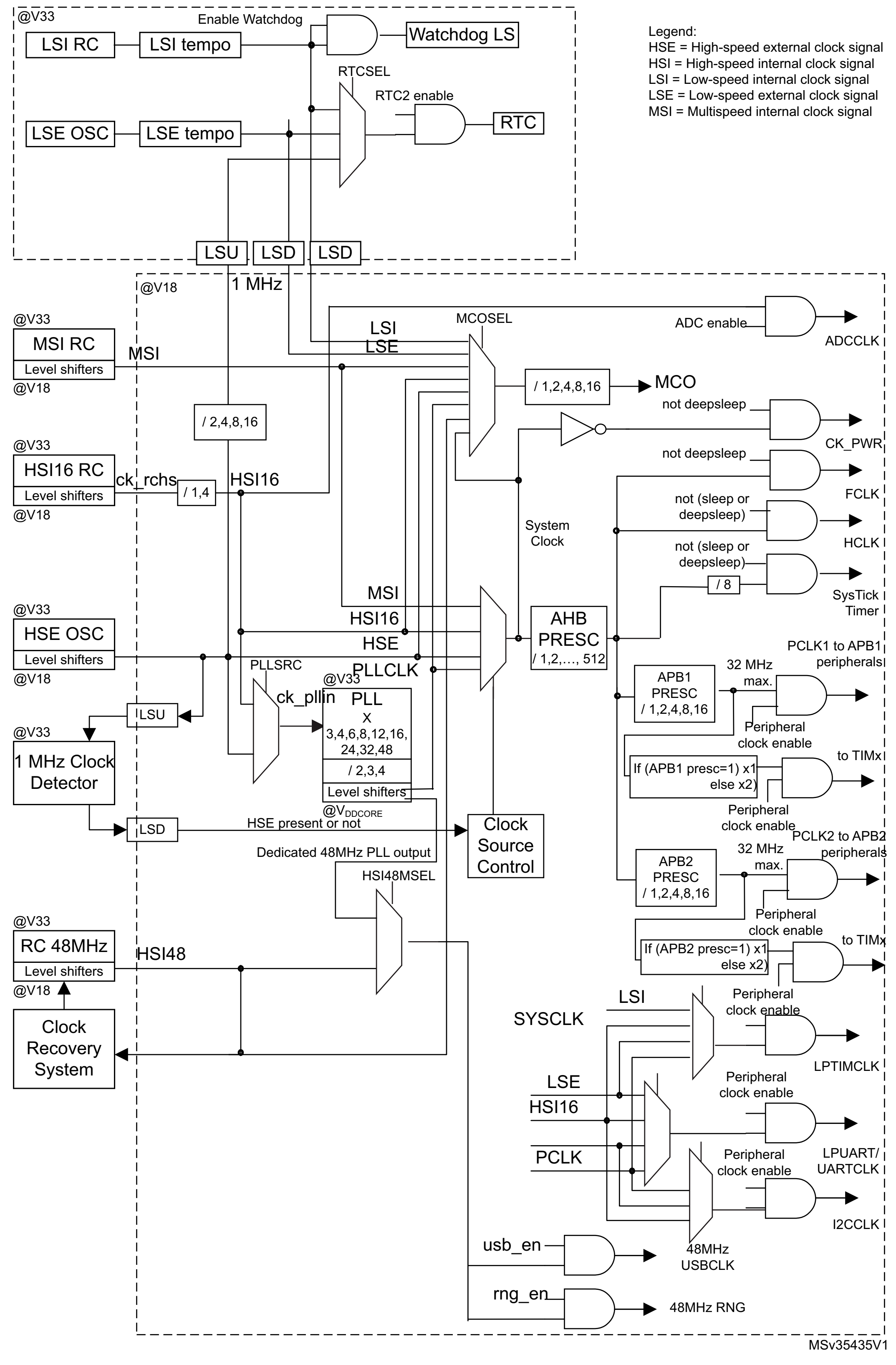


Table 16. STM32L072xxx pin definition (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32(1)	LQFP48	LQFP64	UFBGA64/TFBGA64	WLCSP49	LQFP100	UFBG100						
12	12	16	22	G4	G5	31	L4	PA6	I/O	FT	-	SPI1_MISO, TIM3_CH1, TSC_G2_IO3, LPUART1_CTS, TIM22_CH1, EVENTOUT, COMP1_OUT	ADC_IN6
13	13	17	23	H4	F4	32	M4	PA7	I/O	FT	-	SPI1_MOSI, TIM3_CH2, TSC_G2_IO4, TIM22_CH2, EVENTOUT, COMP2_OUT	ADC_IN7
-	-	-	24	H5	-	33	K5	PC4	I/O	FT	-	EVENTOUT, LPUART1_TX	ADC_IN14
-	-	-	25	H6	-	34	L5	PC5	I/O	FT	-	LPUART1_RX, TSC_G3_IO1	ADC_IN15
14	14	18	26	F5	G4	35	M5	PB0	I/O	FT	-	EVENTOUT, TIM3_CH3, TSC_G3_IO2	ADC_IN8, VREF_OUT
15	15	19	27	G5	D3	36	M6	PB1	I/O	FT	-	TIM3_CH4, TSC_G3_IO3, LPUART1_RTS	ADC_IN9, VREF_OUT
-	-	20	28	G6	E3	37	L6	PB2	I/O	FT	-	LPTIM1_OUT, TSC_G3_IO4, I2C3_SMBA	-
-	-	-	-	-	-	38	M7	PE7	I/O	FT	-	USART5_CK/USART5_RTS_DE	-
-	-	-	-	-	-	39	L7	PE8	I/O	FT	-	USART4_TX	-
-	-	-	-	-	-	40	M8	PE9	I/O	FT	-	TIM2_CH1, TIM2_ETR, USART4_RX	-
-	-	-	-	-	-	41	L8	PE10	I/O	FT	-	TIM2_CH2, USART5_TX	-
-	-	-	-	-	-	42	M9	PE11	I/O	FT	-	TIM2_CH3, USART5_RX	-
-	-	-	-	-	-	43	L9	PE12	I/O	FT	-	TIM2_CH4, SPI1_NSS	-
-	-	-	-	-	-	44	M10	PE13	I/O	FT	-	SPI1_SCK	-
-	-	-	-	-	-	45	M11	PE14	I/O	FT	-	SPI1_MISO	-

Table 16. STM32L072xxx pin definition (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32(1)	LQFP48	LQFP64	UFBGA64/TFBGA64	WLCSP49	LQFP100	UFBG100						
-	24	36	48	E6	A1	75	G11	VDD_USB	S		-	-	-
24	25	37	49	A7	B2	76	A10	PA14	I/O	FT	-	SWCLK, USART2_TX, LPUART1_TX	-
25	-	38	50	A6	A2	77	A9	PA15	I/O	FT	-	SPI1_NSS, TIM2_ETR, EVENTOUT, USART2_RX, TIM2_CH1, USART4_RTS_DE	-
-	-	-	51	B7	-	78	B11	PC10	I/O	FT	-	LPUART1_TX, USART4_TX	-
-	-	-	52	B6	-	79	C10	PC11	I/O	FT	-	LPUART1_RX, USART4_RX	-
-	-	-	53	C5	-	80	B10	PC12	I/O	FT	-	USART5_TX, USART4_CK	-
-	-	-	-	-	-	81	C9	PD0	I/O	FT	-	TIM21_CH1, SPI2_NSS/I2S2_WS	-
-	-	-	-	-	-	82	B9	PD1	I/O	FT	-	SPI2_SCK/I2S2_CK	-
-	-	-	54	B5	-	83	C8	PD2	I/O	FT	-	LPUART1_RTS_DE, TIM3_ETR, USART5_RX	-
-	-	-	-	-	-	84	B8	PD3	I/O	FT	-	USART2_CTS, SPI2_MISO/I2S2_MCK	-
-	-	-	-	-	-	85	B7	PD4	I/O	FT	-	USART2_RTS_DE, SPI2_MOSI/I2S2_SD	-
-	-	-	-	-	-	86	A6	PD5	I/O	FT	-	USART2_TX	-
-	-	-	-	-	-	87	B6	PD6	I/O	FT	-	USART2_RX	-
-	-	-	-	-	-	88	A5	PD7	I/O	FT	-	USART2_CK, TIM21_CH2	-
26	-	39	55	A5	A3	89	A8	PB3	I/O	FT	-	SPI1_SCK, TIM2_CH2, TSC_G5I_O1, EVENTOUT, USART1__RTS_DE, USART5_TX	COMP2_INM

Table 24. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}[2]	Total current into sum of all V_{DD} power lines (source)[1]	105	mA
ΣI_{VSS}[2]	Total current out of sum of all V_{SS} ground lines (sink)[1]	105	
ΣI_{VDD_USB}	Total current into V_{DD_USB} power lines (source)	25	
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin (source)[1]	100	
$I_{VSS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)[1]	100	
I_{IO}	Output current sunk by any I/O and control pin except FTf pins	16	
	Output current sunk by FTf pins	22	
	Output current sourced by any I/O and control pin	-16	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins except PA11 and PA12[2]	90	
	Total output current sunk by PA11 and PA12	25	
	Total output current sourced by sum of all IOs and control pins[2]	-90	
$I_{INJ(PIN)}$	Injected current on FT, FFf, RST and B pins	-5/+0[3]	
	Injected current on TC pin	± 5[4]	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)[5]	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive current injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 23* for maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 23: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 25. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 26. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	32	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	32	
f_{PCLK2}	Internal APB2 clock frequency	-	0	32	
V_{DD}	Standard operating voltage	BOR detector disabled	1.65	3.6	V
		BOR detector enabled, at power on	1.8	3.6	
		BOR detector disabled, after power on	1.65	3.6	
V_{DDA}	Analog operating voltage (DAC not used)	Must be the same voltage as V_{DD}(1)	1.65	3.6	V
V_{DDA}	Analog operating voltage (all features)	Must be the same voltage as V_{DD}(1)	1.8	3.6	V
V_{DD_USB}	Standard operating voltage, USB domain(2)	USB peripheral used	3.0	3.6	V
		USB peripheral not used	1.65	3.6	
V_{IN}	Input voltage on FT, FTf and RST pins(3)	$2.0\ V \leq V_{DD} \leq 3.6\ V$	-0.3	5.5	V
		$1.65\ V \leq V_{DD} \leq 2.0\ V$	-0.3	5.2	
	Input voltage on BOOT0 pin	-	0	5.5	
	Input voltage on TC pin	-	-0.3	V_{DD}+0.3	

Table 29. Embedded internal reference voltage(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LPBUF}(4)	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V_{REFINT_DIV1}(4)	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}(4)	1/2 reference voltage	-	49	50	51	
V_{REFINT_DIV3}(4)	3/4 reference voltage	-	74	75	76	

1. Refer to *Table 41: Peripheral current consumption in Stop and Standby mode* for the value of the internal reference current consumption (I_{REFINT}).
2. Guaranteed by test in production.
3. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.
4. Guaranteed by design.
5. Shortest sampling time can be determined in the application by multiple iterations.
6. To guarantee less than 1% VREF_OUT deviation.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 15: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code if not specified otherwise.

The current consumption values are derived from the tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 26: General operating conditions* unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time and prefetch is adjusted depending on fHCLK frequency and voltage range to provide the best CPU performance unless otherwise specified.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{APB}$
- When PLL is on, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used)
- The HSE user clock applied to OSCI_IN input follows the characteristic specified in *Table 43: High-speed external user clock characteristics*
- For maximum current consumption $V_{DD} = V_{DDA} = 3.6$ V is applied to all supply pins
- For typical current consumption $V_{DD} = V_{DDA} = 3.0$ V is applied to all supply pins if not specified otherwise

The parameters given in *Table 51*, *Table 26* and *Table 27* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 26*.

Figure 20. I_{DD} vs V_{DD}, at T_A= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks off

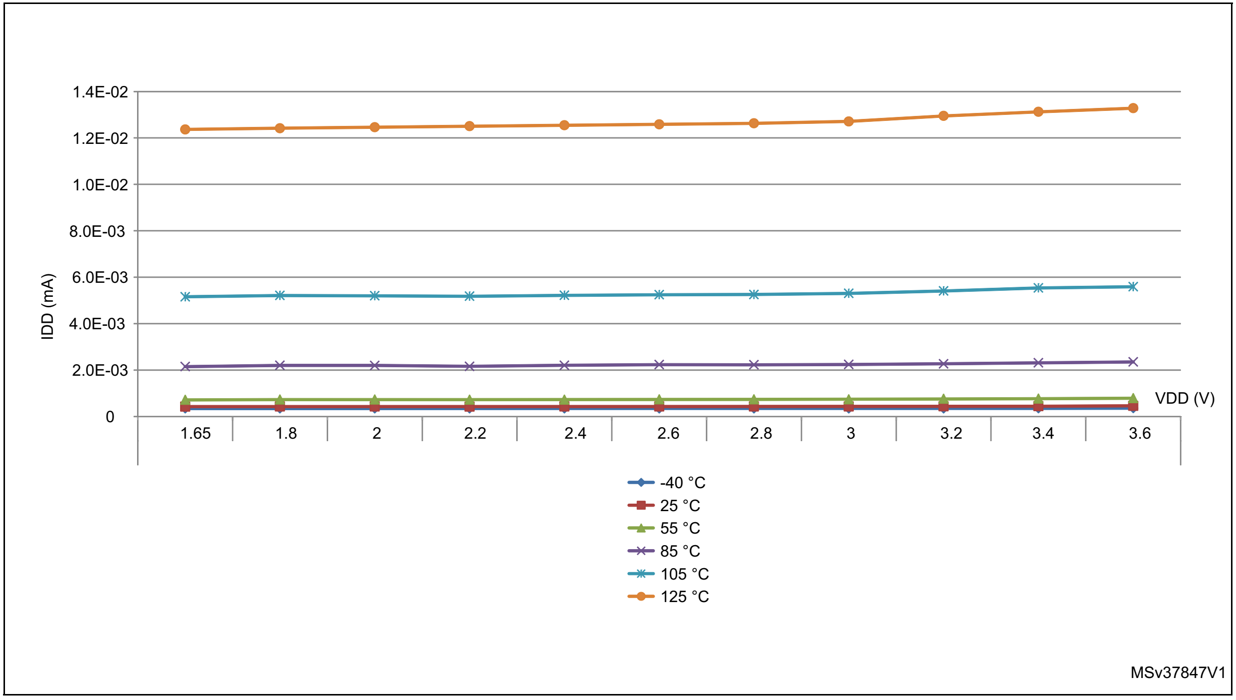


Table 38. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions		Typ	Max[1]	Unit
I_{DD} (Standby)	Supply current in Standby mode	Independent watchdog and LSI enabled	T_A = − 40 to 25°C	0,855	1,70	µA
			T_A = 55 °C	-	2,90	
			T_A= 85 °C	-	3,30	
			T_A = 105 °C	-	4,10	
			T_A = 125 °C	-	8,50	
		Independent watchdog and LSI off	T_A = − 40 to 25°C	0,29	0,60	
			T_A = 55 °C	0,32	1,20	
			T_A = 85 °C	0,5	2,30	
			T_A = 105 °C	0,94	3,00	
			T_A = 125 °C	2,6	7,00	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified

Low-speed external user clock generated from an external source

The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 26*.

Table 44. Low-speed external user clock characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time		465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production

Figure 22. Low-speed external clock source AC timing diagram

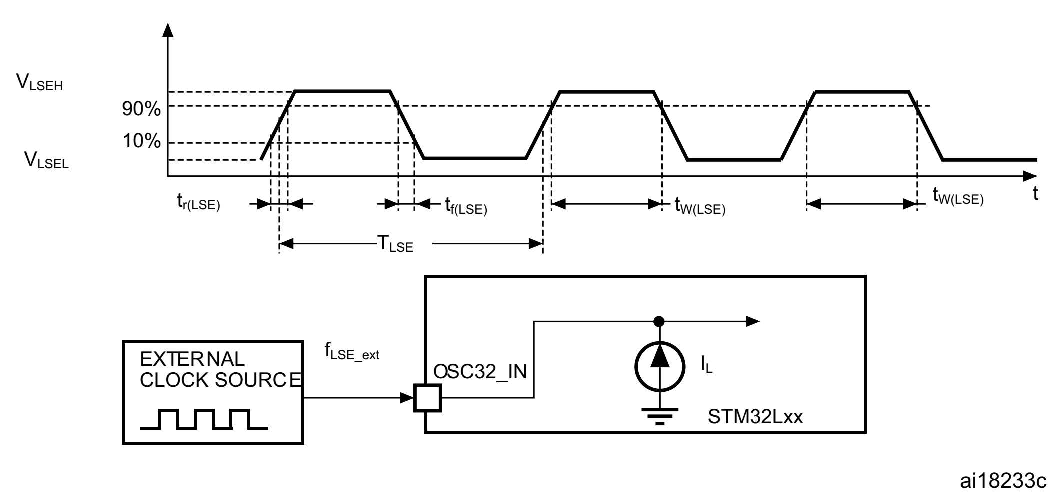


Table 50. MSI oscillator characteristics (continued)

Symbol	Parameter	Condition	Typ	Max	Unit
$t_{STAB(MSI)}$[2]	MSI oscillator stabilization time	MSI range 0	-	40	µs
		MSI range 1	-	20	
		MSI range 2	-	10	
		MSI range 3	-	4	
		MSI range 4	-	2.5	
		MSI range 5	-	2	
		MSI range 6, Voltage range 1 and 2	-	2	
		MSI range 3, Voltage range 3	-	3	
$f_{OVER(MSI)}$	MSI oscillator frequency overshoot	Any range to range 5	-	4	MHz
		Any range to range 6	-	6	

1. This is a deviation for an individual part, once the initial frequency has been measured.
2. Guaranteed by characterization results.

6.3.8 PLL characteristics

The parameters given in *Table 51* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 26*.

Table 51. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max[1]	
f_{PLL_IN}	PLL input clock[2]	2	-	24	MHz
	PLL input clock duty cycle	45	-	55	%
f_{PLL_OUT}	PLL output clock	2	-	32	MHz
t_{LOCK}	PLL input = 16 MHz PLL VCO = 96 MHz	-	115	160	µs
Jitter	Cycle-to-cycle jitter	-		± 600	ps
$I_{DDA}(PLL)$	Current consumption on V_{DDA}	-	220	450	µA
$I_{DD}(PLL)$	Current consumption on V_{DD}	-	120	150	

1. Guaranteed by characterization results.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

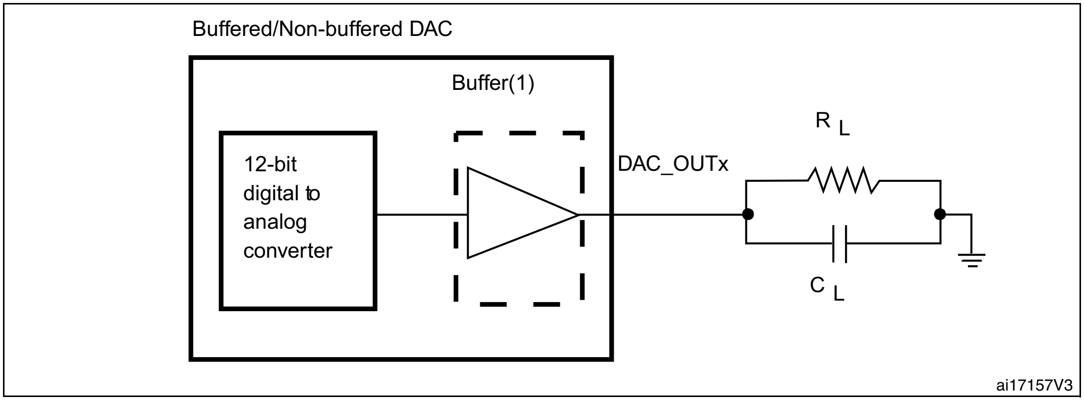
Table 64. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{ADC}(3)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(3)(5)	Calibration time	f_{ADC} = 16 MHz	5.2			µs
		-	83			$1/f_{ADC}$
$W_{LATENCY}$(6)	ADC_DR register write latency	ADC clock = HSI16	1.5 ADC cycles + 2 f_{PCLK} cycles	-	1.5 ADC cycles + 3 f_{PCLK} cycles	-
		ADC clock = PCLK/2	-	4.5	-	f_{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f_{PCLK} cycle
t_{latr}(3)	Trigger conversion latency	$f_{ADC} = f_{PCLK}/2$ = 16 MHz	0.266			µs
		$f_{ADC} = f_{PCLK}/2$	8.5			$1/f_{PCLK}$
		$f_{ADC} = f_{PCLK}/4$ = 8 MHz	0.516			µs
		$f_{ADC} = f_{PCLK}/4$	16.5			$1/f_{PCLK}$
		$f_{ADC} = f_{HSI16}$ = 16 MHz	0.252	-	0.260	µs
$Jitter_{ADC}$	ADC jitter on trigger conversion	$f_{ADC} = f_{HSI16}$	-	1	-	$1/f_{HSI16}$
t_S(3)	Sampling time	f_{ADC} = 16 MHz	0.093	-	10.03	µs
		-	1.5	-	160.5	$1/f_{ADC}$
t_{UP_LDO}(3)(5)	Internal LDO power-up time	-	-	-	10	µs
t_{STAB}(3)(5)	ADC stabilization time	-	14			$1/f_{ADC}$
t_{ConV}(3)	Total conversion time (including sampling time)	f_{ADC} = 16 MHz, 12-bit resolution	0.875	-	10.81	µs
		12-bit resolution	14 to 173 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. V_{DDA} minimum value can be decreased in specific temperature conditions. Refer to *Table 65: RAIN max for fADC = 16 MHz*.
2. A current consumption proportional to the APB clock frequency has to be added (see *Table 40: Peripheral current consumption in Run or Sleep mode*).
3. Guaranteed by design.
4. Standard channels have an extra protection resistance which depends on supply voltage. Refer to *Table 65: RAIN max for fADC = 16 MHz*.
5. This parameter only includes the ADC timing. It does not take into account register access latency.
6. This parameter specifies the latency to transfer the conversion result into the ADC_DR register. EOC bit is set to indicate the conversion is complete and has the same latency.

6. Difference between the value measured at Code (0x800) and the ideal value = $V_{REF+}/2$.
7. Difference between the value measured at Code (0x001) and the ideal value.
8. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is off, and from code giving 0.2 V and (V_{DDA} – 0.2) V when buffer is on.
9. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

Figure 34. 12-bit buffered/non-buffered DAC



6.3.17 Temperature sensor characteristics

Table 68. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3 V	0x1FF8 007A - 0x1FF8 007B
TS_CAL2	TS ADC raw data acquired at temperature of 130 °C, V_{DDA}= 3 V	0x1FF8 007E - 0x1FF8 007F

Table 69. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	1.48	1.61	1.75	mV/°C
V_{130}	Voltage at 130°C ±5°C(2)	640	670	700	mV
$I_{DDA(TEMP)}$(3)	Current consumption	-	3.4	6	µA
t_{START}(3)	Startup time	-	-	10	µs
T_{S_temp}(4)(3)	ADC sampling time when reading the temperature	10	-	-	

1. Guaranteed by characterization results.
2. Measured at V_{DD} = 3 V ±10 mV. V130 ADC conversion result is stored in the TS_CAL2 byte.
3. Guaranteed by design.
4. Shortest sampling time can be determined in the application by multiple iterations.

Table 77. SPI characteristics in voltage Range 3 (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	2	MHz
		Slave mode			$2^{(2)}$	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	1.5	-	-	
$t_{su(SI)}$		Slave mode	6	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	13.5	-	-	
$t_{h(SI)}$		Slave mode	16	-	-	
$t_{a(SO}$	Data output access time	Slave mode	30	-	70	
$t_{dis(SO)}$	Data output disable time	Slave mode	40	-	80	
$t_{v(SO)}$	Data output valid time	Slave mode	-	30	70	
$t_{v(MO)}$		Master mode	-	7	9	
$t_{h(SO)}$	Data output hold time	Slave mode	25	-	-	
$t_{h(MO)}$		Master mode	8	-	-	

1. Guaranteed by characterization results.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

Figure 35. SPI timing diagram - slave mode and CPHA = 0

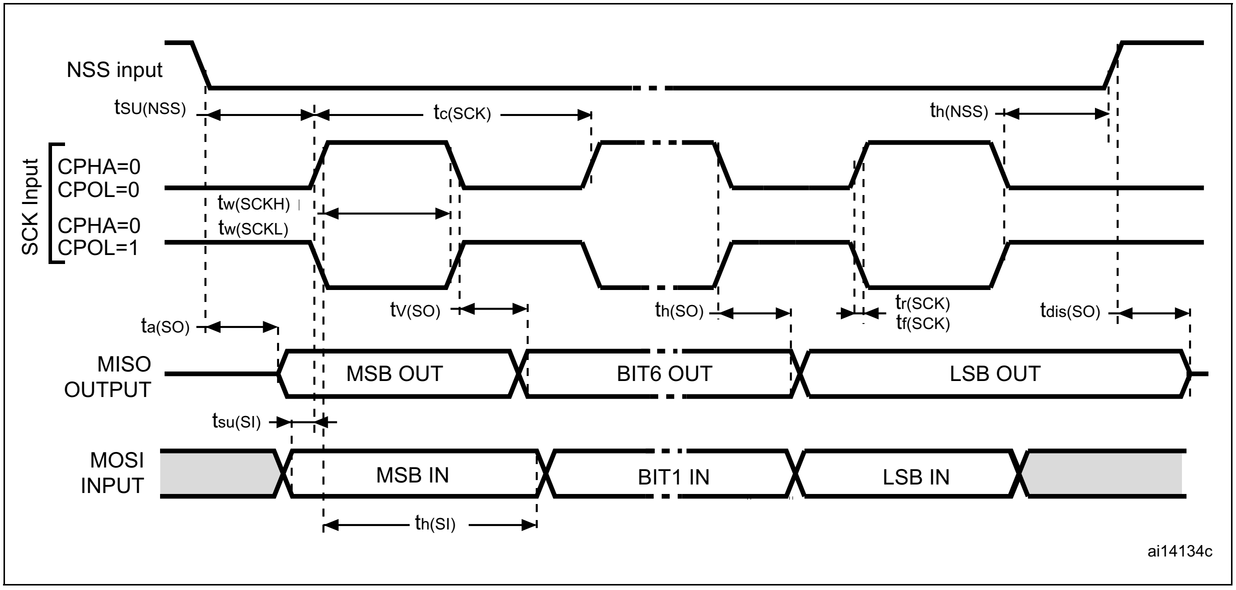
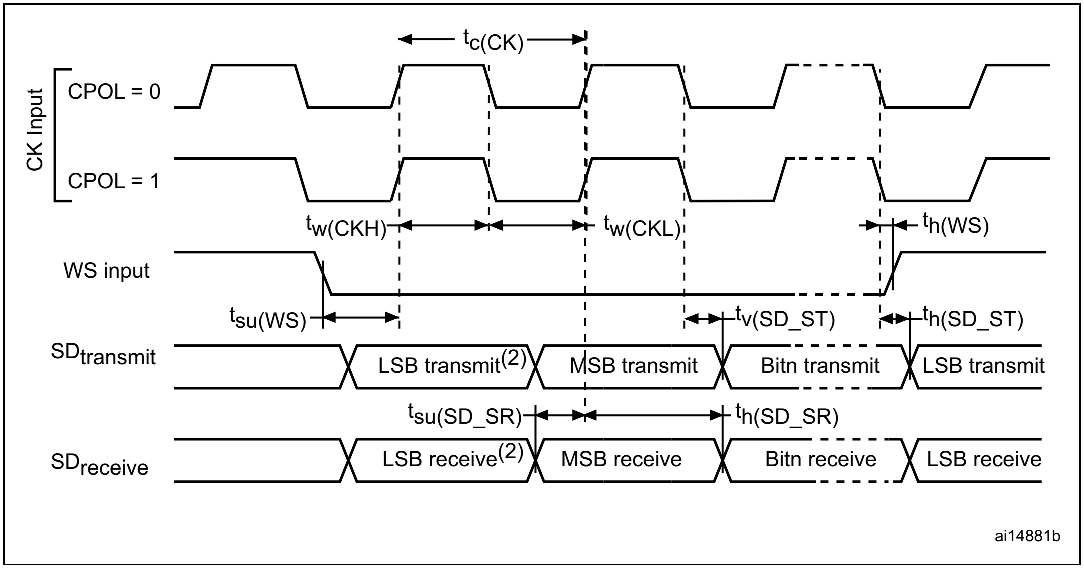
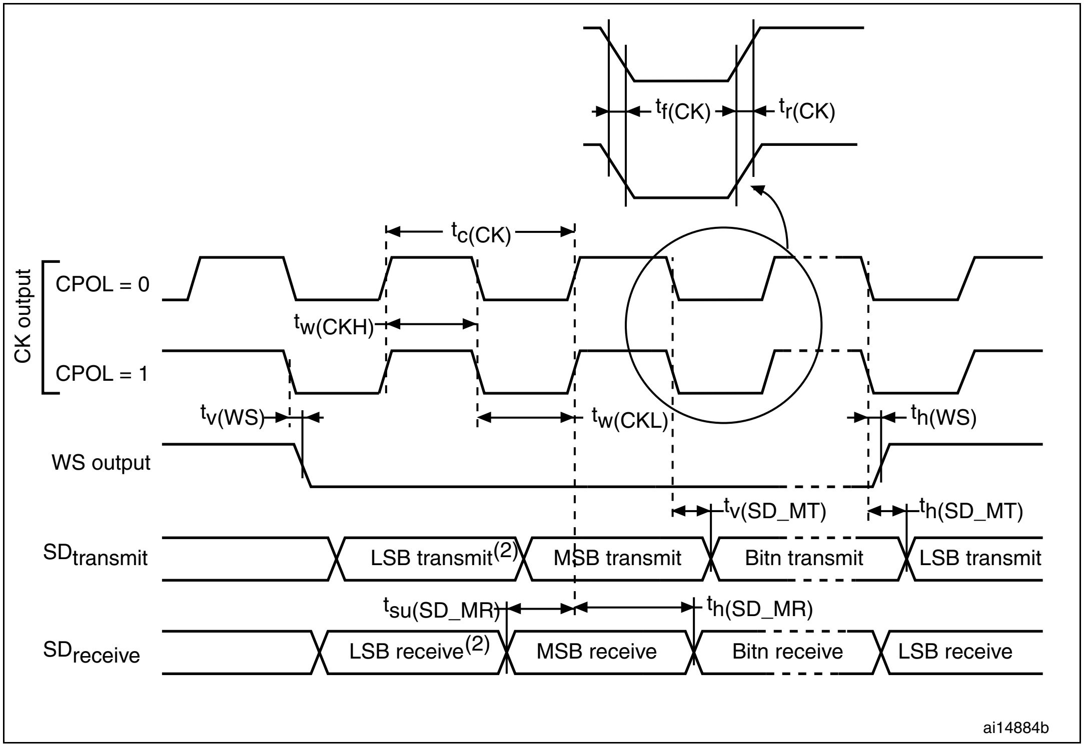


Figure 38. I^{2}S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at CMOS levels: 0.3 × V_{DD} and 0.7 × V_{DD}.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 39. I^{2}S master timing diagram (Philips protocol)(1)



1. Guaranteed by characterization results.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 40. USB timings: definition of data signal rise and fall time

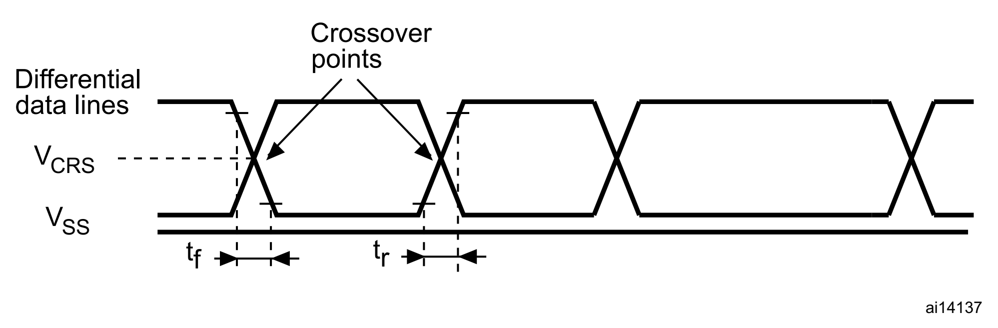


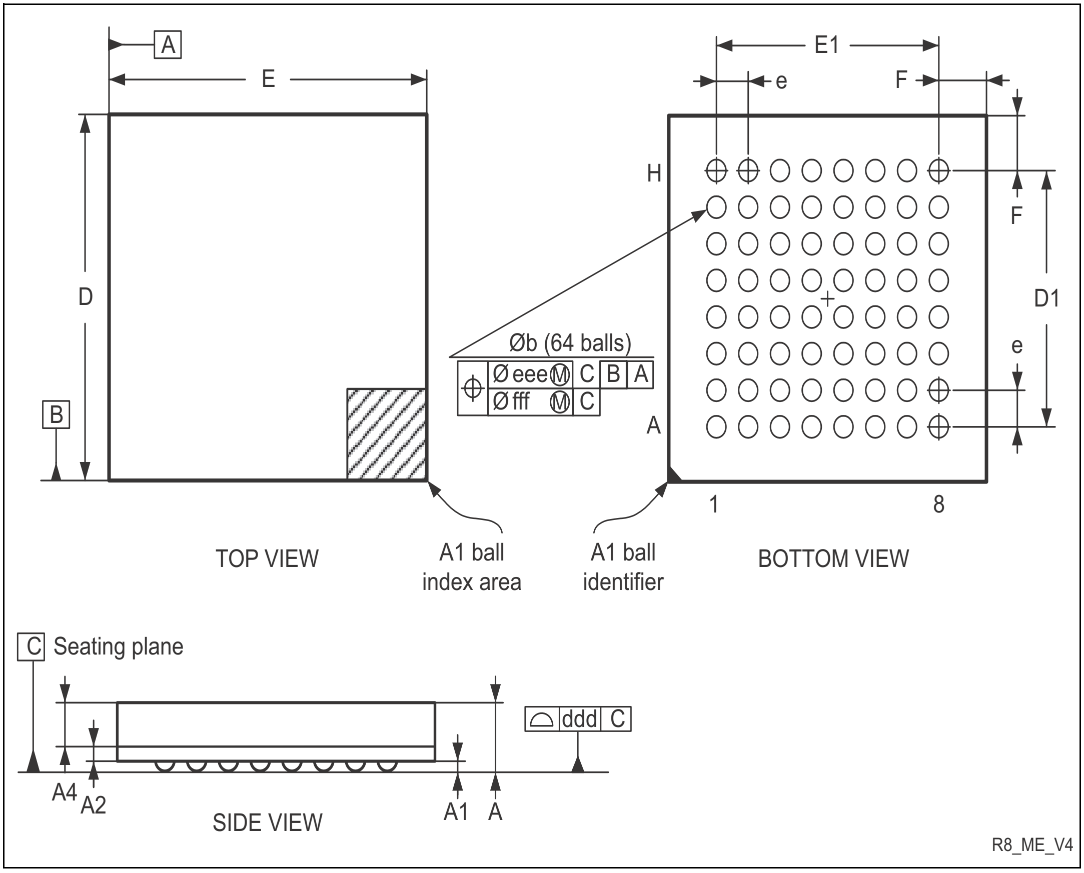
Table 81. USB: full speed electrical characteristics

Driver characteristics[1]					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time[2]	C_L = 50 pF	4	20	ns
t_f	Fall Time[2]	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

7.5 TFBGA64 package information

Figure 51. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch thin profile fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 88. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.150	-	-	0.0059	-	-
A2	-	0.200	-	-	0.0079	-
A4	-	-	0.600	-	-	0.0236
b	0.250	0.300	0.350	0.0098	0.0118	0.0138
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	-	3.500	-	-	0.1378	-
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	-	3.500	-	-	0.1378	-

Table 92. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.