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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l072kzt6

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

• Startup clock

After reset, the microcontroller restarts by default with an internal 2.1 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.

• Clock security system (CSS)

This feature can be enabled by software. If an HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.

Another clock security system can be enabled, in case of failure of the LSE it provides an interrupt or wakeup event which is generated if enabled.

Clock-out capability (MCO: microcontroller clock output)

It outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.



3.8 Memories

The STM32L072xx devices have the following features:

- 20 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
 - 64, 128 or 192 Kbytes of embedded Flash program memory
 - 6 Kbytes of data EEPROM
 - Information block containing 32 user and factory options bytes plus 8 Kbytes of system memory

Flash program and data EEPROM are divided into two banks. This allows writing in one bank while running code or reading data from the other bank.

The user options bytes are used to write-protect or read-out protect the memory (with 4 Kbyte granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no protection
- Level 1: memory readout protected.

The Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected

 Level 2: chip readout protected, debug features (Cortex-M0+ serial wire) and boot in RAM selection disabled (debugline fuse)

The firewall protects parts of code/data from access by the rest of the code that is executed outside of the protected area. The granularity of the protected code segment or the non-volatile data segment is 256 bytes (Flash memory or EEPROM) against 64 bytes for the volatile data segment (RAM).

The whole non-volatile memory embeds the error correction code (ECC) feature.

3.9 Boot modes

At startup, BOOT0 pin and nBOOT1 option bit are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using USB (PA11, PA12), USART1(PA9, PA10) or USART2(PA2, PA3). See STM32[™] microcontroller system memory boot mode AN2606 for details.



3.16.4 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit downcounter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches '0'.

3.16.5 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

3.16.6 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.17 Communication interfaces

3.17.1 I²C bus

Up to three I²C interfaces (I2C1 and I2C3) can operate in multimaster or slave modes.

Each I²C interface can support Standard mode (Sm, up to 100 kbit/s), Fast mode (Fm, up to 400 kbit/s) and Fast Mode Plus (Fm+, up to 1 Mbit/s) with 20 mA output drive on some I/Os.

7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask) are also supported as well as programmable analog and digital noise filters.

	Analog filter	Digital filter		
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks		
Benefits	Available in Stop mode	 Extra filtering capability vs. standard requirements. Stable length 		
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.		

Table 11. Comparison of I2C analog and digital filters

In addition, I2C1 and I2C3 provide hardware support for SMBus 2.0 and PMBus 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1/I2C3 also have a clock domain





1. The above figure shows the package top view.

2. I/O pin supplied by VDD_USB.



1. The above figure shows the package top view.

2. I/O pin supplied by VDD_USB.



			Pin n	umb	er								
LQFP32	UFQFPN32 ⁽¹⁾	LQFP48	LQFP64	UFBGA64/TFBGA64	WLCSP49	LQFP100	UFBG100	Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
-	-	2	2	A2	B7	7	C1	PC13	I/O	FT	-	-	RTC_TAMP1/RTC_TS/ RTC_OUT/WKUP2
2	1	3	3	A1	C6	8	D1	PC14- OSC32_IN (PC14)	I/O	FT	-	-	OSC32_IN
3	2	4	4	B1	C7	9	E1	PC15- OSC32_OUT (PC15)	I/O	тс	-	-	OSC32_OUT
-	-	-	-	-	-	10	F2	PH9	I/O	FT	-	-	-
-	-	-	-	-	-	11	G2	PH10	I/O	FT	-	-	-
-	-	5	5	C1	D6	12	F1	PH0-OSC_IN (PH0)	I/O	тс	-	USB_CRS_SYNC	OSC_IN
-	-	6	6	D1	D7	13	G1	PH1- OSC_OUT (PH1)	I/O	тс	-	-	OSC_OUT
4	3	7	7	E1	D5	14	H2	NRST	I/O		1	-	-
-	-	-	8	E3	C5	15	H1	PC0	I/O	FTf	-	LPTIM1_IN1, EVENTOUT, TSC_G7_IO1, LPUART1_RX, I2C3_SCL	ADC_IN10
-	-	-	9	E2	C4	16	J2	PC1	I/O	FTf	-	LPTIM1_OUT, EVENTOUT, TSC_G7_IO2, LPUART1_TX, I2C3_SDA	ADC_IN11
-	-	-	10	F2	E7	17	J3	PC2	I/O	FTf	-	LPTIM1_IN2, SPI2_MISO/I2S2_MCK, TSC_G7_IO3	ADC_IN12
-	-	-	11	-	-	18	К2	PC3	I/O	FT	-	LPTIM1_ETR, SPI2_MOSI/I2S2_SD, TSC_G7_I04	ADC_IN13
-	4	8	12	F1	-	19	J1	VSSA	S		-	-	-



		I	Pin n	umb	er								
LQFP32	UFQFPN32 ⁽¹⁾	LQFP48	LQFP64	UFBGA64/TFBGA64	WLCSP49	LQFP100	UFBG100	Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
-	-	-	-	-	-	60	H12	PD13	I/O	FT	-	-	-
-	-	-	-	-	-	61	H11	PD14	I/O	FT	-	-	-
-	-	-	-	-	-	62	H10	PD15	I/O	FT	-	USB_CRS_SYNC	-
-	-	-	37	F6	-	63	E12	PC6	I/O	FT	-	TIM22_CH1, TIM3_CH1, TSC_G8_IO1	-
-	-	-	38	E7	-	64	E11	PC7	I/O	FT	-	TIM22_CH2, TIM3_CH2, TSC_G8_IO2	-
-	-	-	39	E8	-	65	E10	PC8	I/O	FT	-	TIM22_ETR, TIM3_CH3, TSC_G8_IO3	-
-	-	-	40	D8	-	66	D12	PC9	I/O	FTf	-	TIM21_ETR, USB_OE/TIM3_CH4, TSC_G8_IO4, I2C3_SDA	-
18	18	29	41	D7	D1	67	D11	PA8	I/O	FTf	-	MCO, USB_CRS_SYNC, EVENTOUT, USART1_CK, I2C3_SCL	-
19	19	30	42	C7	E2	68	D10	PA9	I/O	FTf	-	MCO, TSC_G4_IO1, USART1_TX, I2C1_SCL, I2C3_SMBA	-
20	20	31	43	C6	C1	69	C12	PA10	I/O	FTf	-	TSC_G4_IO2, USART1_RX, I2C1_SDA	-
21	21	32	44	C8	D2	70	B12	PA11	I/O	FT	(3)	SPI1_MISO, EVENTOUT, TSC_G4_IO3, USART1_CTS, COMP1_OUT	USB_DM
22	22	33	45	B8	B1	71	A12	PA12	I/O	FT	(3)	SPI1_MOSI, EVENTOUT, TSC_G4_IO4, USART1_RTS_DE, COMP2_OUT	USB_DP
23	23	34	46	A8	C2	72	A11	PA13	I/O	FT	-	SWDIO, USB_OE, LPUART1_RX	-
_	-	-	-	-	-	73	C11	VDD	S		-	-	-
-	-	35	47	D5	-	74	F11	VSS	S		-	-	-

Table To. STWSZLU/ZXXX pin deminition (continued)



					Table 21.	Alternate fur	nctions port E			
			AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
	Port		SPI1/SPI2/I2S2/ USART1/2/ LPUART1/USB/ LPTIM1/TSC/ TIM2/21/22/ EVENTOUT/ SYS_AF	SPI1/SPI2/I2S2/I2C1 /TIM2/21	SPI1/SPI2/I2S2/ LPUART1/ USART5/USB/ LPTIM1/TIM2/3 /EVENTOUT/ SYS_AF	I2C1/TSC/ EVENTOUT	I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT	SPI2/I2S2 /I2C2/ USART1/ TIM2/21/22	I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/ EVENTOUT	I2C3/LPUART1/ COMP1/2/TIM3
Docl		PE0	-		EVENTOUT	-	-	-	-	-
		PE1	-		EVENTOUT	-	-	-	-	-
		PE2	-		TIM3_ETR	-	-	-	-	-
		PE3	TIM22_CH1		TIM3_CH1	-	-	-	-	-
		PE4	TIM22_CH2	-	TIM3_CH2	-	-	-	-	-
		PE5	TIM21_CH1	-	TIM3_CH3	-	-	-	-	-
D02		PE6	TIM21_CH2	-	TIM3_CH4	-	-	-	-	-
27100 Re ¹	Port E	PE7	-		-	-	-	-	USART5_CK/U SART5_RTS_D E	-
3		PE8	-		-	-	-	-	USART4_TX	-
		PE9	TIM2_CH1		TIM2_ETR	-	-	-	USART4_RX	-
		PE10	TIM2_CH2		-	-	-	-	USART5_TX	-
		PE11	TIM2_CH3	-	-	-	-	-	USART5_RX	-
		PE12	TIM2_CH4	-	SPI1_NSS	-	-	-	-	-
		PE13	-		SPI1_SCK	-	-	-	-	-
		PE14	-		SPI1_MISO	-	-	-	-	-
		PE15	-		SPI1_MOSI	-	-	-	-	-

55/147

STM32L072xx

Pin descriptions

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 23: Voltage characteristics*, *Table 24: Current characteristics*, and *Table 25: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Symbol	Definition	Min	Мах	Unit
$V_{DD} - V_{SS}$	External main supply voltage (including V _{DDA} , V _{DD_USB} , V _{DD}) ⁽¹⁾	-0.3	4.0	
	Input voltage on FT and FTf pins	$V_{SS} - 0.3$	V _{DD} +4.0	
V(2)	Input voltage on TC pins	$V_{SS} - 0.3$	4.0	V
VIN' /	Input voltage on BOOT0	V _{SS}	$V_{DD} + 4.0$	
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	
$ \Delta V_{DD} $	Variations between different V_{DDx} power pins	-	50	
V _{DDA} -V _{DDx}	Variations between any V_{DDx} and V_{DDA} power $\mbox{pins}^{(3)}$	-	300	mV
$ \Delta V_{SS} $	Variations between all different ground pins including $V_{\text{REF}\text{-}}$ pin	-	50	
$V_{REF+} - V_{DDA}$	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	V
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	see Section 6.3.11		

Table 23	. Voltage	characteristics
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1. All main power ($V_{DD}, V_{DD}, U_{SB}, V_{DDA}$) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

2. V_{IN} maximum must always be respected. Refer to *Table 24* for maximum allowed injected current values.

 It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and device operation. V_{DD_USB} is independent from V_{DD} and V_{DDA}: its value does not need to respect this rule.



6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in *Table 26*.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
		BOR detector enabled	0	-	∞	
t _{VDD} ⁽¹⁾	V _{DD} rise time rate	BOR detector disabled	0	-	1000	
		BOR detector enabled	20	-	×	μs/v
	V _{DD} fail time rate	BOR detector disabled	0	-	1000	
T (1)	Deast temperization	V _{DD} rising, BOR enabled	-	2	3.3	
RSTTEMPO	Resertemponzation	V _{DD} rising, BOR disabled ⁽²⁾	0.4	0.7	1.6	ms
VDOD/DDD	Power on/power down reset	Falling edge	1	1.5	1.65	
VPOR/PDR	threshold	Rising edge	1.3	1.5	1.65	
V	Drown out react threshold 0	Falling edge	1.67	1.7	1.74	
VBOR0	Brown-out reset threshold 0	Rising edge	1.69	1.76	1.8	
Veee	Drown out react threshold 1	Falling edge	1.87	1.93	1.97	
VBOR1	Rising edge		1.96	2.03	2.07	
V _{BOR2}	Brown out reset threshold 2	Falling edge	2.22	2.30	2.35	
	Rising edge		2.31	2.41	2.44	
Vnona	Brown out reset threshold 3	Falling edge	2.45	2.55	2.6	
VBOR3		Rising edge	2.54	2.66	2.7	
V	Prown out report throshold 4	Falling edge	2.68	2.8	2.85	
VBOR4		Rising edge	2.78	2.9	2.95	V
V	Programmable voltage detector	Falling edge	1.8	1.85	1.88	
V PVD0	threshold 0	Rising edge	1.88	1.94	1.99	
V	D\/D threehold 1	Falling edge	1.98	2.04	2.09	
VPVD1		Rising edge	2.08	2.14	2.18	
V	D\/D threehold 2	Falling edge	2.20	2.24	2.28	
VPVD2		Rising edge	2.28	2.34	2.38	
V	D\/D throshold 3	Falling edge	2.39	2.44	2.48	
♥ PVD3		Rising edge	2.47	2.54	2.58	
V	D\/D throshold 4	Falling edge	2.57	2.64	2.69	
YPVD4		Rising edge	2.68	2.74	2.79	
V	D\/D threshold 5	Falling edge	2.77	2.83	2.88	
V PVD5		Rising edge	2.87	2.94	2.99]

Table 27. Embedded reset and	power control block	characteristics
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Symbol	parameter	System frequency	Current consumption during wakeup	Unit
		HSI	1	
	Supply current during Wakeup from Stop mode	HSI/4	0,7	mA
I _{DD} (Wakeup from Stop)		MSI clock = 4,2 MHz	0,7	
		MSI clock = 1,05 MHz	0,4	
		MSI clock = 65 KHz	0,1	
I _{DD} (Reset)	Reset pin pulled down	-	0,21	
I _{DD} (Power-up)	BOR on	-	0,23	
I _{DD} (Wakeup from	With Fast wakeup set	MSI clock = 2,1 MHz	0,5	
StandBy)	With Fast wakeup disabled	MSI clock = 2,1 MHz	0,12	

Table 39. Average current consumption during Wakeup



Symbol	Parinharal	Typical consum	Unit	
Symbol	Feripiteral	V _{DD} =1.8 V V _{DD} =3.0 V		
I _{DD(PVD / BOR)}	-	0.7	1.2	
I _{REFINT}	-	-	1.7	
-	LSE Low drive ⁽²⁾	0.11	0,13	
-	LSI	0.27	0.31	
-	IWDG	0.2	0.3	
-	LPTIM1, Input 100 Hz	0.01	0,01	μΑ
-	LPTIM1, Input 1 MHz	11	12	
-	LPUART1	-	0,5	
-	RTC	0.16	0,3	

Table 41. Peripheral current consumption in §	Stop and Standby mode ⁽¹
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1. LPTIM, LPUART peripherals can operate in Stop mode but not in Standby mode.

2. LSE Low drive consumption is the difference between an external clock on OSC32_IN and a quartz between OSC32_IN and OSC32_OUT.-

6.3.5 Wakeup time from low-power mode

The wakeup times given in the following table are measured with the MSI or HSI16 RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is either the MSI oscillator in the range configured before entering Stop mode, the HSI16 or HSI16/4.
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 26*.

Symbol	Parameter	Conditions	Тур	Max	Unit
t _{WUSLEEP}	Wakeup from Sleep mode	f _{HCLK} = 32 MHz	7	8	
	Wakeup from Low-power sleep mode,	f _{HCLK} = 262 kHz Flash memory enabled	7	8	Number of clock
WUSLEEP_ LP	f _{HCLK} = 262 kHz	f _{HCLK} = 262 kHz Flash memory switched OFF	9	10	cycles

Table 42	I ow-nower	mode	wakeun	timinas
1 a Die 42.	LOW-DOWEI	moue	waneup	unnigs



Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 46*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Conditions ⁽²⁾	Min ⁽²⁾	Тур	Max	Unit
f _{LSE}	LSE oscillator frequency		-	32.768	-	kHz
	Maximum critical crystal transconductance	LSEDRV[1:0]=00 lower driving capability	-	-	0.5	
6		LSEDRV[1:0]= 01 medium low driving capability	-	-	0.75	
Gm		LSEDRV[1:0] = 10 medium high driving capability	-	-	1.7	μΑνν
		LSEDRV[1:0]=11 higher driving capability	-	-	2.7	
t _{SU(LSE)} ⁽³⁾	Startup time	V _{DD} is stabilized	-	2	-	S

	Table 46. L	SE oscillator	characteristics ⁽¹⁾
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1. Guaranteed by design.

2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".

3. Guaranteed by characterization results. t_{SU(LSE)} is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer. To increase speed, address a lower-drive quartz with a high- driver mode.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website <u>www.st.com</u>.





Note:

An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.



6.3.7 Internal clock source characteristics

The parameters given in *Table 47* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 26*.

High-speed internal 16 MHz (HSI16) RC oscillator

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{HSI16}	Frequency	V _{DD} = 3.0 V	-	16	-	MHz
TRIM ⁽¹⁾⁽²⁾	HSI16 user-	Trimming code is not a multiple of 16	-	±0.4	0.7	%
	trimmed resolution	Trimming code is a multiple of 16	-	-	± 1.5	%
		V _{DDA} = 3.0 V, T _A = 25 °C	-1 ⁽³⁾	-	1 ⁽³⁾	%
ACC _{HSI16}	Accuracy of the factory-calibrated HSI16 oscillator	V_{DDA} = 3.0 V, T_A = 0 to 55 °C	-1.5	-	1.5	%
		V_{DDA} = 3.0 V, T_A = -10 to 70 °C	-2	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 85 °C	-2.5	-	2	%
		V _{DDA} = 3.0 V, T _A = -10 to 105 °C	-4	-	2	%
		V _{DDA} = 1.65 V to 3.6 V T _A = − 40 to 125 °C	-5.45	-	3.25	%
t _{SU(HSI16)} ⁽²⁾	HSI16 oscillator startup time	-	-	3.7	6	μs
I _{DD(HSI16)} ⁽²⁾	HSI16 oscillator power consumption	-	-	100	140	μA

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).

2. Guaranteed by characterization results.

3. Guaranteed by test in production.



Figure 25. HSI16 minimum and maximum value versus temperature

DocID027100 Rev 3



6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts \times (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Symbol	Ratings	Conditions	Class	Maximum value ⁽¹⁾	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	$T_A = +25 \degree C$, conforming to ANSI/JEDEC JS-001	2	2000	V
V _{ESD(CDM)}	Electrostatic discharge voltage (charge device model)	$T_A = +25 \degree C$, conforming to ANSI/ESD STM5.3.1.	C4	500	v

Table 57. ESD absolute maximum ratings

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 58. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = +125$ °C conforming to JESD78A	II level A



6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of $-5 \mu A/+0 \mu A$ range), or other functional failure (for example reset occurrence oscillator frequency deviation).

The test results are given in the Table 59.

		Functional s		
Symbol	Description	Negative injection	Positive injection	Unit
	Injected current on BOOT0	-0	NA	
Symbol	Injected current on PA0, PA4, PA5, PC15, PH0 and PH1	-5	0	mA
	Injected current on any other FT, FTf pins	-5 ⁽¹⁾	NA	
	Injected current on any other pins	-5 ⁽¹⁾	+5	

Table 59. I/O current injection susceptibility

1. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.



Symbol	Parameter	Conditions	Min	Тур	Max	Unit
ET	Total unadjusted error		-	2	5	
EO	Offset error		-	1	2.5	
EG	Gain error		-	1	2	LSB
EL	Integral linearity error	1.65 V < V _{REF+} <v<sub>DDA < 3.6 V, range 1/2/3</v<sub>	-	1.5	3	
ED	Differential linearity error		-	1	2	
ENOB	Effective number of bits		10.0	11.0	-	bits
SINAD	Signal-to-noise distortion		62	69	-	
SNR	Signal-to-noise ratio		61	69	-	dB
THD	Total harmonic distortion		-	-85	-65	

Table 66. ADC accuracy⁽¹⁾⁽²⁾⁽³⁾ (continued)

1. ADC DC accuracy values are measured after internal calibration.

 ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in Section 6.3.12 does not affect the ADC accuracy.

3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.

4. This number is obtained by the test board without additional noise, resulting in non-optimized value for oversampling mode.



Figure 30. ADC accuracy characteristics



Symbol	millimeters			inches ⁽¹⁾		
	Min	Тур	Мах	Min	Тур	Мах
А	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3 ⁽²⁾	-	0.025	-	-	0.0010	-
b ⁽³⁾	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	3.259	3.294	3.329	0.1283	0.1297	0.1311
E	3.223	3.258	3.293	0.1269	0.1283	0.1296
е	-	0.400	-	-	0.0157	-
e1	-	2.400	-	-	0.0945	-
e2	-	2.400	-	-	0.0945	-
F	-	0.447	-	-	0.0176	-
G	-	0.429	-	-	0.0169	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ССС	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

Table 90. WLCSP49 - 49-pin, 3.294 x 3.258 mm, 0.4 mm pitch wafer level chip scalepackage mechanical data

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. Back side coating

3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 55. WLCSP49 - 49-pin, 3.294 x 3.258 mm, 0.4 mm pitch wafer level chip scale recommended footprint





7.9 UFQFPN32 package information





^{1.} Drawing is not to scale.



7.10 Thermal characteristics

The maximum chip-junction temperature, $T_{\rm J}$ max, in degrees Celsius, may be calculated using the following equation:

 $T_J \max = T_A \max + (P_D \max \times \Theta_{JA})$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and P_{I/O} max (P_D max = P_{INT} max + P_{I/O}max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

P_{I/O} max represents the maximum power dissipation on output pins where:

 $\mathsf{P}_{\mathsf{I}/\mathsf{O}} \max = \Sigma (\mathsf{V}_{\mathsf{OL}} \times \mathsf{I}_{\mathsf{OL}}) + \Sigma ((\mathsf{V}_{\mathsf{DD}} - \mathsf{V}_{\mathsf{OH}}) \times \mathsf{I}_{\mathsf{OH}}),$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Symbol	Parameter	Value	Unit
Θ _{JA}	Thermal resistance junction-ambient UFQFPN32 - 5 x 5 mm / 0.5 mm pitch	36	
	Thermal resistance junction-ambient LQFP32 - 7 x 7 mm / 0.8 mm pitch	60	
	Thermal resistance junction-ambient LQFP48 - 7 x 7 mm / 0.5 mm pitch	54	
	Thermal resistance junction-ambient WLCSP49 - 0.4 mm pitch	48	
	Thermal resistance junction-ambient TFBGA64 - 5 x 5 mm / 0.5 mm pitch	64	°C/W
	Thermal resistance junction-ambient UFBGA64 - 5 x 5 mm / 0.5 mm pitch	65	
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	41	
	Thermal resistance junction-ambient UFBGA100 - 7 x 7 mm / 0.5 mm pitch	57	

Table 95. Thermal characteristics



Date	Revision	Changes
22-Mar-2016	3	Updated number of SPIs on cover page and in <i>Table 2: Ultra-low-power STM32L072xx device features and peripheral counts.</i> Changed minimum comparator supply voltage to 1.65 V on cover page. Added minimum DAC supply voltage on cover page. Added number of fast and standard channels in <i>Section 3.11:</i> <i>Analog-to-digital converter (ADC).</i> Updated <i>Section 3.17.2: Universal synchronous/asynchronous</i> <i>receiver transmitter (USART)</i> and <i>Section 3.17.4: Serial</i> <i>peripheral interface (SPI)/Inter-integrated sound (I2S)</i> to mention the fact that USARTs with synchronous mode feature can be used as SPI master interfaces. Added baudrate allowing to wake up the MCU from Stop mode in <i>Section 3.17.2: Universal synchronous/asynchronous receiver</i> <i>transmitter (USART)</i> and <i>Section 3.17.3: Low-power universal</i> <i>asynchronous receiver transmitter (LPUART).</i> <i>Section 6.3.15: 12-bit ADC characteristics:</i> – <i>Table 64: ADC characteristics:</i> Distinction made between V _{DDA} for fast and standard channels; added note 1. Added note 4. related to R _{ADC} . Updated f _{TRIG} . Updated f _{TRIG} . Updated f ₂ and t _{CONV} . – Updated <i>Table 65: RAIN max for fADC = 16 MHz</i> for f _{ADC} <i>=</i> 16 MHz and distinction made between fast and standard channels. Updated R _Q and added Note 2. in <i>Table 67: DAC characteristics:</i> Added <i>Table 74: USART/LPUART characteristics.</i>

Table 97. Document revision history

