



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l072rbt3

3 Functional overview

3.1 Low-power modes

The ultra-low-power STM32L072xx support dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 (V_{DD} range limited to 1.71-3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full V_{DD} range), with a maximum CPU frequency of 16 MHz
- Range 3 (full V_{DD} range), with a maximum CPU frequency limited to 4.2 MHz

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

- **Low-power run mode**

This mode is achieved with the multispeed internal (MSI) RC oscillator set to the low-speed clock (max 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In Low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

- **Low-power sleep mode**

This mode is achieved by entering Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

When wakeup is triggered by an event or an interrupt, the system reverts to the Run mode with the regulator on.

Stop mode with RTC

The Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSE crystal and HSI RC oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

The device can be woken up from Stop mode by any of the EXTI line, in 3.5 μ s, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on), it can be the RTC alarm/tamper/timestamp/wakeup events, the USB/USART/I2C/LPUART/LPTIMER wakeup events.

- **Stop mode without RTC**

The Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are disabled.

Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 3.5 μ s, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB/USART/I2C/LPUART/LPTIMER wakeup events.

- **Standby mode with RTC**

The Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSE crystal and HSI RC oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

The device exits Standby mode in 60 μ s when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby mode without RTC**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

The device exits Standby mode in 60 μ s when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.

3.4 Reset and supply management

3.4.1 Power supply schemes

- $V_{DD} = 1.65$ to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA} , $V_{DDA} = 1.65$ to 3.6 V: external analog power supplies for ADC reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.
- $V_{DD_USB} = 1.65$ to 3.6 V: external power supply for USB transceiver, USB_DM (PA11) and USB_DP (PA12). To guarantee a correct voltage level for USB communication V_{DD_USB} must be above 3.0 V. If USB is not used this pin must be tied to V_{DD} .

3.4.2 Power supply supervisor

The devices have an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

Two versions are available:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the V_{DD} min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for any external reset circuit.

Note: *The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.*

The devices feature an embedded programmable voltage detector (PVD) that monitors the $V_{DD/VDDA}$ power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when $V_{DD/VDDA}$ drops below the V_{PVD} threshold and/or when $V_{DD/VDDA}$ is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.10 Direct memory access (DMA)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I²C, USART, LPUART, general-purpose timers, DAC, and ADC.

3.11 Analog-to-digital converter (ADC)

A native 12-bit, extended to 16-bit through hardware oversampling, analog-to-digital converter is embedded into STM32L072xx device. It has up to 16 external channels and 3 internal channels (temperature sensor, voltage reference). Three channels, PA0, PA4 and PA5, are fast channels, while the others are standard channels.

The ADC performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of 1.14 MSPS even with a low CPU speed. The ADC consumption is low at all frequencies (~25 μ A at 10 kSPS, ~240 μ A at 1MSPS). An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.

The ADC can be served by the DMA controller. It can operate from a supply voltage down to 1.65 V.

The ADC features a hardware oversampler up to 256 samples, this improves the resolution to 16 bits (see AN2668).

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers.

3.12 Temperature sensor

The temperature sensor (T_{SENSE}) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 7. Temperature sensor calibration values

Calibration value name	Description	Memory address
TSENSE_CAL1	TS ADC raw data acquired at temperature of 30 °C, $V_{DDA} = 3\text{ V}$	0x1FF8 007A - 0x1FF8 007B
TSENSE_CAL2	TS ADC raw data acquired at temperature of 130 °C $V_{DDA} = 3\text{ V}$	0x1FF8 007E - 0x1FF8 007F

3.12.1 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the V_{DD} value (when no external voltage, V_{REF+} , is available for ADC). The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 8. Internal voltage reference measured values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25 °C $V_{DDA} = 3\text{ V}$	0x1FF8 0078 - 0x1FF8 0079

3.13 Digital-to-analog converter (DAC)

Two 12-bit buffered DACs can be used to convert digital signal into analog voltage signal output. An optional amplifier can be used to reduce the output signal impedance.

This digital Interface supports the following features:

- One data holding register (for each channel)
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channels with independent or simultaneous conversions
- DMA capability (including the underrun interrupt)
- External triggers for conversion
- Input reference voltage V_{REF+}

Six DAC trigger inputs are used in the STM32L072xx. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.14 Ultra-low-power comparators and reference voltage

The STM32L072xx embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with ultra low consumption
- One comparator with rail-to-rail inputs, fast or slow mode.
- The threshold can be one of the following:
 - DAC output
 - External I/O pins
 - Internal reference voltage (V_{REFINT})
 - submultiple of Internal reference voltage (1/4, 1/2, 3/4) for the rail to rail comparator.

Both comparators can wake up the devices from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 μ A typical).

3.15 Touch sensing controller (TSC)

The STM32L072xx provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 24 capacitive sensing channels distributed over 8 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (such as glass, plastic). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage, this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library, which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

independent from the CPU clock, allowing the I2C1/I2C3 to wake up the MCU from Stop mode on address match.

Each I2C interface can be served by the DMA controller.

Refer to [Table 12](#) for an overview of I2C interface features.

Table 12. STM32L072xx I²C implementation

I2C features ⁽¹⁾	I2C1	I2C2	I2C3
7-bit addressing mode	X	X	X
10-bit addressing mode	X	X	X
Standard mode (up to 100 kbit/s)	X	X	X
Fast mode (up to 400 kbit/s)	X	X	X
Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X ⁽²⁾	X
Independent clock	X	-	X
SMBus	X	-	X
Wakeup from STOP	X	-	X

1. X = supported.

2. See [Table 16: STM32L072xxx pin definition on page 43](#) for the list of I/Os that feature Fast Mode Plus capability

3.17.2 Universal synchronous/asynchronous receiver transmitter (USART)

The four USART interfaces (USART1, USART2, USART4 and USART5) are able to communicate at speeds of up to 4 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1 and USART2 also support SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock, allowing to wake up the MCU from Stop mode using baudrates up to 42 Kbaud.

All USART interfaces can be served by the DMA controller.

[Table 13](#) for the supported modes and features of USART interfaces.

Table 13. USART implementation

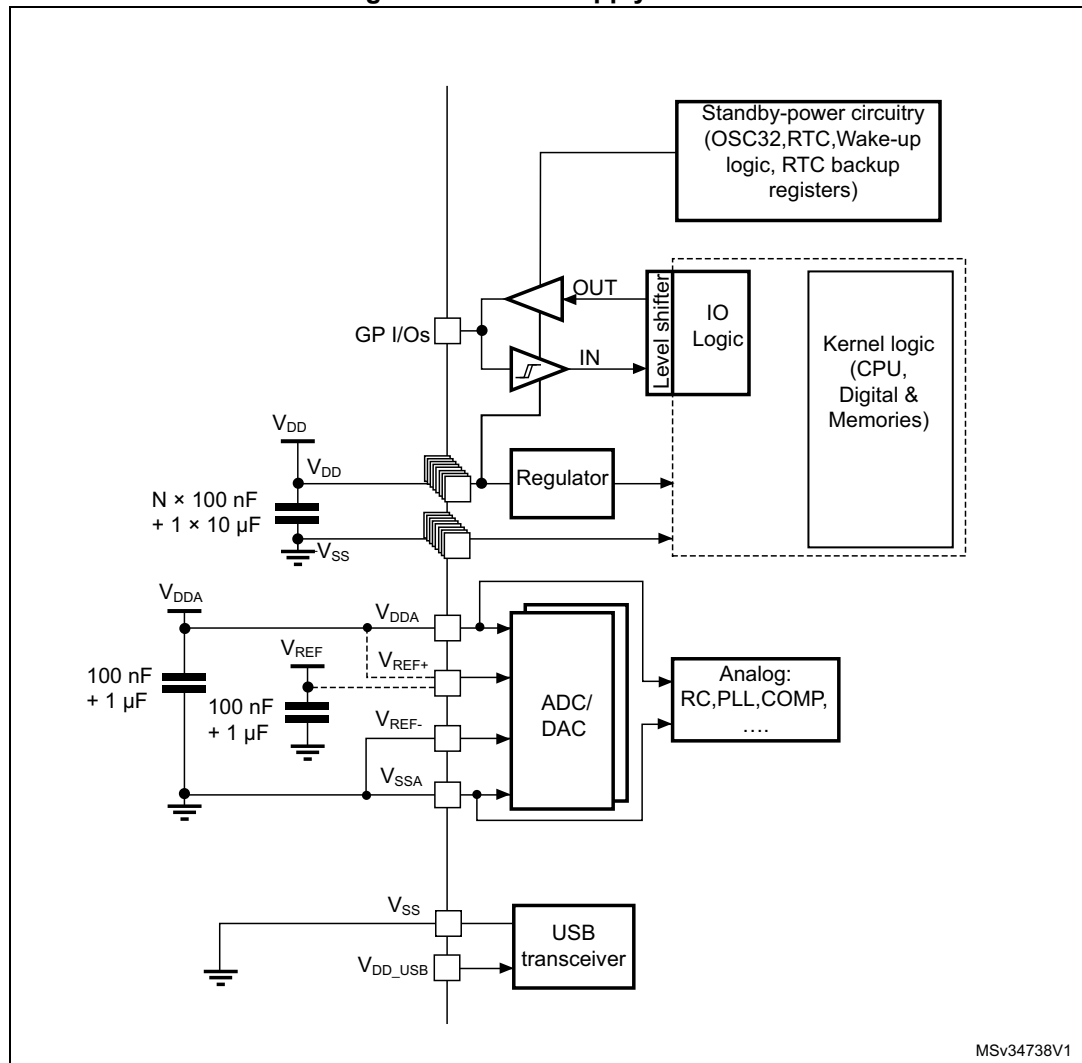
USART modes/features ⁽¹⁾	USART1 and USART2	USART4 and USART5
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode ⁽²⁾	X	X
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	-

Table 21. Alternate functions port E

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/SPI2/I2S2/ USART1/2/ LPUART1/USB/ LPTIM1/TSC/ TIM2/21/22/ EVENTOUT/ SYS_AF	SPI1/SPI2/I2S2/I2C1 /TIM2/21	SPI1/SPI2/I2S2/ LPUART1/ USART5/USB/ LPTIM1/TIM2/3 /EVENTOUT/ SYS_AF	I2C1/TSC/ EVENTOUT	I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT	SPI2/I2S2 /I2C2/ USART1/ TIM2/21/22	I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/ EVENTOUT	I2C3/LPUART1/ COMP1/2/TIM3
Port E	PE0	-		EVENTOUT	-	-	-	-	-
	PE1	-		EVENTOUT	-	-	-	-	-
	PE2	-		TIM3_ETR	-	-	-	-	-
	PE3	TIM22_CH1		TIM3_CH1	-	-	-	-	-
	PE4	TIM22_CH2	-	TIM3_CH2	-	-	-	-	-
	PE5	TIM21_CH1	-	TIM3_CH3	-	-	-	-	-
	PE6	TIM21_CH2	-	TIM3_CH4	-	-	-	-	-
	PE7	-		-	-	-	-	USART5_CK/U SART5_RTS_D E	-
	PE8	-		-	-	-	-	USART4_TX	-
	PE9	TIM2_CH1		TIM2_ETR	-	-	-	USART4_RX	-
	PE10	TIM2_CH2		-	-	-	-	USART5_TX	-
	PE11	TIM2_CH3	-	-	-	-	-	USART5_RX	-
	PE12	TIM2_CH4	-	SPI1_NSS	-	-	-	-	-
	PE13	-		SPI1_SCK	-	-	-	-	-
	PE14	-		SPI1_MISO	-	-	-	-	-
	PE15	-		SPI1_MOSI	-	-	-	-	-

6.1.6 Power supply scheme

Figure 14. Power supply scheme



6.1.7 Current consumption measurement

Figure 15. Current consumption measurement scheme

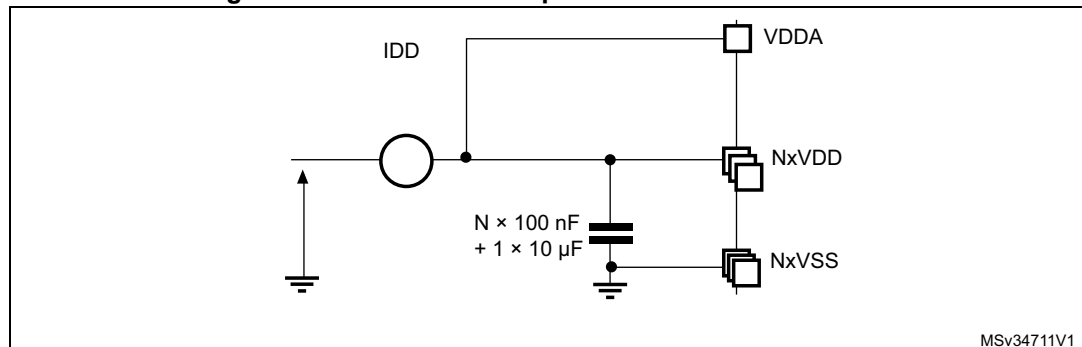


Table 30. Current consumption in Run mode, code with data processing running from Flash memory

Symbol	Parameter	Condition		f _{HCLK} (MHz)	Typ	Max ⁽¹⁾	Unit
I _{DD} (Run from Flash memory)	Supply current in Run mode code executed from Flash memory	f _{HSE} = f _{HCLK} up to 16MHz included, f _{HSE} = f _{HCLK} /2 above 16 MHz (PLL ON) ⁽²⁾	Range3, Vcore=1.2 V VOS[1:0]=11	1	190	250	μA
				2	345	380	
				4	650	670	
			Range2, Vcore=1.5 V VOS[1:0]=10	4	0,8	0,86	mA
				8	1,55	1,7	
				16	2,95	3,1	
			Range1, Vcore=1.8 V VOS[1:0]=01	8	1,9	2,1	
				16	3,55	3,8	
				32	6,65	7,2	
		MSI clock source	Range3, Vcore=1.2 V VOS[1:0]=11	0,065	39	130	μA
				0,524	115	210	
				4,2	700	770	
		HSI clock source (16MHz)	Range2, Vcore=1.5 V VOS[1:0]=10	16	2,9	3,2	mA
			Range1, Vcore=1.8 V VOS[1:0]=01	32	7,15	7,4	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 31. Current consumption in Run mode vs code type, code with data processing running from Flash memory

Symbol	Parameter	Conditions			f _{HCLK}	Typ	Unit
I _{DD} (Run from Flash memory)	Supply current in Run mode, code executed from Flash memory	f _{HSE} = f _{HCLK} up to 16 MHz included, f _{HSE} = f _{HCLK} /2 above 16 MHz (PLL on) ⁽¹⁾	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	Dhrystone	4 MHz	650	μA
				CoreMark		655	
				Fibonacci		485	
				while(1)		385	
				while(1), 1WS, prefetch off		375	
			Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	Dhrystone	32 MHz	6,65	mA
				CoreMark		6,9	
				Fibonacci		6,75	
				while(1)		5,8	
				while(1), prefetch off		5,5	

1. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Figure 20. I_{DD} vs V_{DD} , at $T_A = 25/55/85/105/125\text{ }^{\circ}\text{C}$, Stop mode with RTC disabled, all clocks off

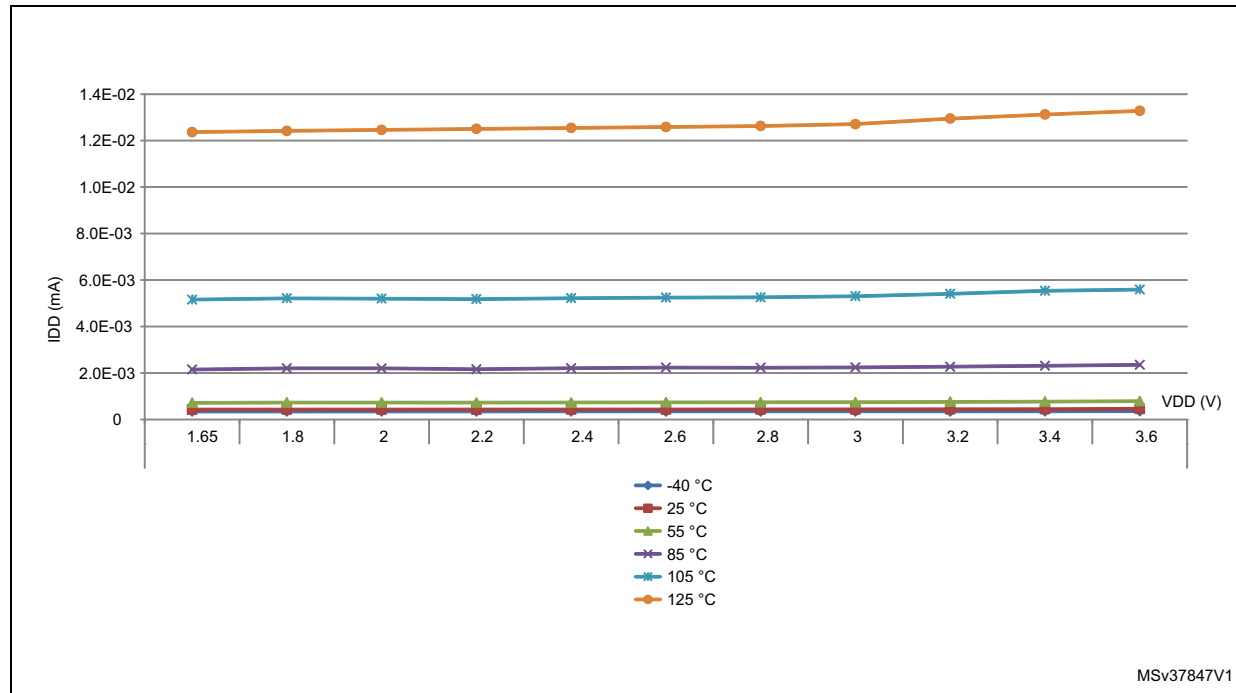


Table 38. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions		Typ	Max ⁽¹⁾	Unit
I_{DD} (Standby)	Supply current in Standby mode	Independent watchdog and LSI enabled	$T_A = -40\text{ to }25\text{ }^{\circ}\text{C}$	0,855	1,70	μA
			$T_A = 55\text{ }^{\circ}\text{C}$	-	2,90	
			$T_A = 85\text{ }^{\circ}\text{C}$	-	3,30	
			$T_A = 105\text{ }^{\circ}\text{C}$	-	4,10	
			$T_A = 125\text{ }^{\circ}\text{C}$	-	8,50	
		Independent watchdog and LSI off	$T_A = -40\text{ to }25\text{ }^{\circ}\text{C}$	0,29	0,60	
			$T_A = 55\text{ }^{\circ}\text{C}$	0,32	1,20	
			$T_A = 85\text{ }^{\circ}\text{C}$	0,5	2,30	
			$T_A = 105\text{ }^{\circ}\text{C}$	0,94	3,00	
			$T_A = 125\text{ }^{\circ}\text{C}$	2,6	7,00	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified

Table 41. Peripheral current consumption in Stop and Standby mode⁽¹⁾

Symbol	Peripheral	Typical consumption, T _A = 25 °C		Unit
		V _{DD} =1.8 V	V _{DD} =3.0 V	
I _{DD} (PVD / BOR)	-	0.7	1.2	μA
I _{REFINT}	-	-	1.7	
-	LSE Low drive ⁽²⁾	0.11	0,13	
-	LSI	0.27	0.31	
-	IWDG	0.2	0.3	
-	LPTIM1, Input 100 Hz	0.01	0,01	
-	LPTIM1, Input 1 MHz	11	12	
-	LPUART1	-	0,5	
-	RTC	0.16	0,3	

1. LPTIM, LPUART peripherals can operate in Stop mode but not in Standby mode.

2. LSE Low drive consumption is the difference between an external clock on OSC32_IN and a quartz between OSC32_IN and OSC32_OUT.-

6.3.5 Wakeup time from low-power mode

The wakeup times given in the following table are measured with the MSI or HSI16 RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is either the MSI oscillator in the range configured before entering Stop mode, the HSI16 or HSI16/4.
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 26](#).

Table 42. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Max	Unit
t _{WUSLEEP}	Wakeup from Sleep mode	f _{HCLK} = 32 MHz	7	8	Number of clock cycles
t _{WUSLEEP_LP}	Wakeup from Low-power sleep mode, f _{HCLK} = 262 kHz	f _{HCLK} = 262 kHz Flash memory enabled	7	8	
		f _{HCLK} = 262 kHz Flash memory switched OFF	9	10	

Output voltage levels

Unless otherwise specified, the parameters given in [Table 61](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 26](#). All I/Os are CMOS and TTL compliant.

Table 61. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	CMOS port ⁽²⁾ , $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD}-0.4$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	TTL port ⁽²⁾ , $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin	TTL port ⁽²⁾ , $I_{IO} = -6 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	2.4	-	
$V_{OL}^{(1)(4)}$	Output low level voltage for an I/O pin	$I_{IO} = +15 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	1.3	
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin	$I_{IO} = -15 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$V_{DD}-1.3$	-	
$V_{OL}^{(1)(4)}$	Output low level voltage for an I/O pin	$I_{IO} = +4 \text{ mA}$ $1.65 \text{ V} \leq V_{DD} < 3.6 \text{ V}$	-	0.45	
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin	$I_{IO} = -4 \text{ mA}$ $1.65 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$V_{DD}-0.45$	-	
$V_{OLFM+}^{(1)(4)}$	Output low level voltage for an FTf I/O pin in Fm+ mode	$I_{IO} = 20 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	
		$I_{IO} = 10 \text{ mA}$ $1.65 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 24](#). The sum of the currents sunk by all the I/Os (I/O ports and control pins) must always be respected and must not exceed $\Sigma I_{IO(PIN)}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 24](#). The sum of the currents sourced by all the I/Os (I/O ports and control pins) must always be respected and must not exceed $\Sigma I_{IO(PIN)}$.
4. Guaranteed by characterization results.

6.3.16 DAC electrical specifications

Data guaranteed by design, not tested in production, unless otherwise specified.

Table 67. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{REF+}	Reference supply voltage	V_{REF+} must always be below V_{DDA}	1.8	-	3.6	V
V_{REF-}	Lower reference voltage	-	V_{SSA}			V
$I_{DDVREF+}^{(1)}$	Current consumption on V_{REF+} supply $V_{REF+} = 3.3$ V	No load, middle code (0x800)	-	130	220	μ A
		No load, worst code (0x000)	-	220	350	
$I_{DDA}^{(2)}$	Current consumption on V_{DDA} supply, $V_{DDA} = 3.3$ V	No load, middle code (0x800)	-			μ A
		No load, worst code (0xF1C)	-			
$R_L^{(3)}$	Resistive load	DAC output buffer on	5	-	-	k Ω
$C_L^{(3)}$	Capacitive load		-	-	50	pF
R_O	Output impedance	DAC output buffer off	12	16	20	k Ω
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON	0.2	-	$V_{DDA} - 0.2$	V
		DAC output buffer OFF	0.5	-	$V_{REF+} - 1\text{LSB}$	mV
DNL ⁽²⁾	Differential non linearity ⁽⁴⁾	$C_L \leq 50$ pF, $R_L \geq 5$ k Ω DAC output buffer on	-	1.5	3	LSB
		No R_{LOAD} , $C_L \leq 50$ pF DAC output buffer off	-	1.5	3	
INL ⁽²⁾	Integral non linearity ⁽⁵⁾	$C_L \leq 50$ pF, $R_L \geq 5$ k Ω DAC output buffer on	-	2	4	
		No R_{LOAD} , $C_L \leq 50$ pF DAC output buffer off	-	2	4	
Offset ⁽²⁾	Offset error at code 0x800 ⁽⁶⁾	$C_L \leq 50$ pF, $R_L \geq 5$ k Ω DAC output buffer on	-	± 10	± 25	
		No R_{LOAD} , $C_L \leq 50$ pF DAC output buffer off	-	± 5	± 8	
Offset1 ⁽²⁾	Offset error at code 0x001 ⁽⁷⁾	No R_{LOAD} , $C_L \leq 50$ pF DAC output buffer off	-	± 1.5	± 5	

SPI characteristics

Unless otherwise specified, the parameters given in the following tables are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 26](#).

Refer to [Section 6.3.12: I/O current injection characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 75. SPI characteristics in voltage Range 1 ⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	16	MHz
		Slave mode receiver			16	
		Slave mode Transmitter $1.71 < V_{DD} < 3.6V$	-	-	12 ⁽²⁾	
		Slave mode Transmitter $2.7 < V_{DD} < 3.6V$	-	-	16 ⁽²⁾	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	$4 \cdot T_{pclk}$	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	$2 \cdot T_{pclk}$	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	$T_{pclk} - 2$	T_{pclk}	$T_{pclk} + 2$	
$t_{su(MI)}$	Data input setup time	Master mode	0	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	7	-	-	
$t_{h(SI)}$		Slave mode	3.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	15	-	36	
$t_{dis(SO)}$	Data output disable time	Slave mode	10	-	30	
$t_{v(SO)}$	Data output valid time	Slave mode $1.65 V < V_{DD} < 3.6 V$	-	18	41	
		Slave mode $2.7 V < V_{DD} < 3.6 V$	-	18	25	
		Master mode	-	4	7	
$t_{h(SO)}$	Data output hold time	Slave mode	10	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Guaranteed by characterization results.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)} = 0$ while $Duty_{(SCK)} = 50\%$.

Technical drawing of a square frame with dimensions and labels. The drawing shows a square frame with a central square opening. The outer dimensions are 16.7 units on all sides. The inner dimensions are 12.3 units on all sides. The frame is composed of four segments, each labeled with a number: 75 (top), 51 (right), 26 (bottom), and 76 (left). The segments are connected by small gaps. The dimensions are indicated by arrows and numerical values. The labels 1, 25, and 100 are also present near the bottom-left corner.

1. Dimensions are expressed in millimeters.

Table 86. UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 49. UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package recommended footprint

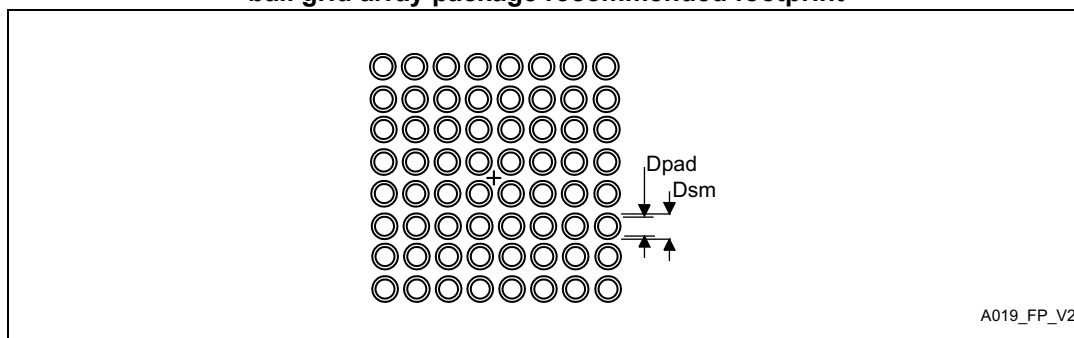


Table 87. UFBGA64 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

Table 88. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
F	-	0.750	-	-	0.0295	-
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 52. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array recommended footprint

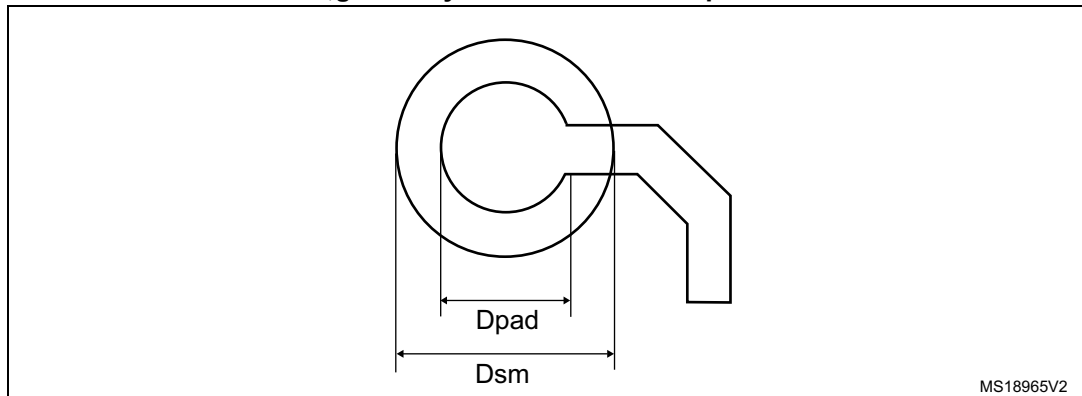


Table 89. TFBGA64 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

Note: *Non solder mask defined (NSMD) pads are recommended.
4 to 6 mils solder paste screen printing process.*

Table 90. WLCSP49 - 49-pin, 3.294 x 3.258 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3 ⁽²⁾	-	0.025	-	-	0.0010	-
b ⁽³⁾	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	3.259	3.294	3.329	0.1283	0.1297	0.1311
E	3.223	3.258	3.293	0.1269	0.1283	0.1296
e	-	0.400	-	-	0.0157	-
e1	-	2.400	-	-	0.0945	-
e2	-	2.400	-	-	0.0945	-
F	-	0.447	-	-	0.0176	-
G	-	0.429	-	-	0.0169	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. Back side coating

3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

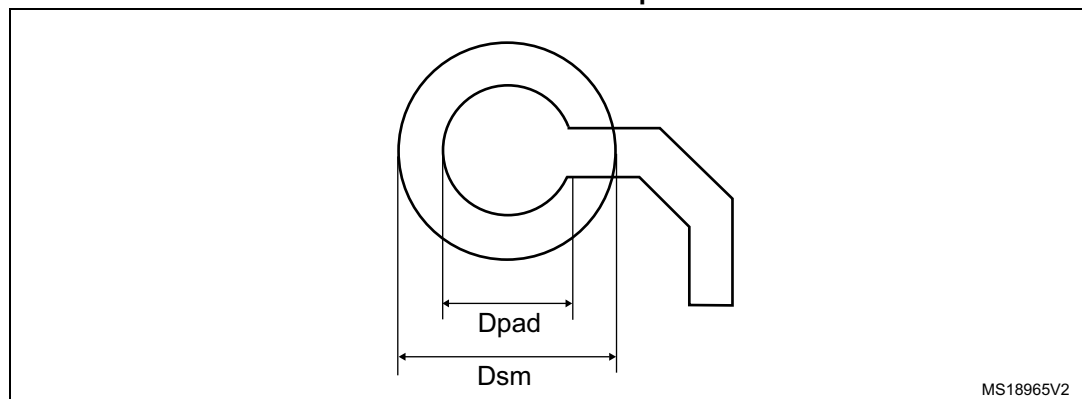
Figure 55. WLCSP49 - 49-pin, 3.294 x 3.258 mm, 0.4 mm pitch wafer level chip scale recommended footprint

Table 92. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.