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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I <sup>2</sup> C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	51
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TFBGA
Supplier Device Package	64-TFBGA (5x5)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l072rzh6tr">https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l072rzh6tr</a>

- **Stop mode without RTC**

The Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are disabled.

Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 3.5  $\mu$ s, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB/USART/I2C/LPUART/LPTIMER wakeup events.

- **Standby mode with RTC**

The Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire  $V_{CORE}$  domain is powered off. The PLL, MSI RC, HSE crystal and HSI RC oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC\_CSR register).

The device exits Standby mode in 60  $\mu$ s when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby mode without RTC**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire  $V_{CORE}$  domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC\_CSR register).

The device exits Standby mode in 60  $\mu$ s when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

*Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.*

Table 3. Functionalities depending on the operating power supply range

Operating power supply range	Functionalities depending on the operating power supply range			
	DAC and ADC operation	Dynamic voltage scaling range	I/O operation	USB
$V_{DD} = 1.65$ to $1.71$ V	ADC only, conversion time up to 570 ksp/s	Range 2 or range 3	Degraded speed performance	Not functional
$V_{DD} = 1.71$ to $1.8$ V <sup>(1)</sup>	ADC only, conversion time up to 1.14 Msp/s	Range 1, range 2 or range 3	Degraded speed performance	Functional <sup>(2)</sup>
$V_{DD} = 1.8$ to $2.0$ V <sup>(1)</sup>	Conversion time up to 1.14 Msp/s	Range 1, range 2 or range 3	Degraded speed performance	Functional <sup>(2)</sup>
$V_{DD} = 2.0$ to $2.4$ V	Conversion time up to 1.14 Msp/s	Range 1, range 2 or range 3	Full speed operation	Functional <sup>(2)</sup>
$V_{DD} = 2.4$ to $3.6$ V	Conversion time up to 1.14 Msp/s	Range 1, range 2 or range 3	Full speed operation	Functional <sup>(2)</sup>

1. CPU frequency changes from initial to final must respect " $f_{cpu\ initial} < 4 * f_{cpu\ final}$ ". It must also respect 5  $\mu$ s delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5  $\mu$ s, then switch from 16 MHz to 32 MHz.
2. To be USB compliant from the I/O voltage standpoint, the minimum  $V_{DD\_USB}$  is 3.0 V.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
32 kHz to 4.2 MHz (0ws)	Range 3

**Table 5. Functionalities depending on the working mode  
(from Run/active down to standby) (continued)<sup>(1)(2)</sup>**

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
					Wakeup capability		Wakeup capability	
Temperature sensor	O	O	O	O	O		--	
Comparators	O	O	O	O	O	O	--	
16-bit timers	O	O	O	O	--		--	
LPTIMER	O	O	O	O	O	O		
IWDG	O	O	O	O	O	O	O	O
WWDG	O	O	O	O	--		--	
Touch sensing controller (TSC)	O	O	--	--	--		--	
SysTick Timer	O	O	O	O			--	
GPIOs	O	O	O	O	O	O		2 pins
Wakeup time to Run mode	0 $\mu$ s	0.36 $\mu$ s	3 $\mu$ s	32 $\mu$ s	3.5 $\mu$ s		50 $\mu$ s	
Consumption $V_{DD}=1.8$ to $3.6$ V (Typ)	Down to 140 $\mu$ A/MHz (from Flash memory)	Down to 37 $\mu$ A/MHz (from Flash memory)	Down to 8 $\mu$ A	Down to 4.5 $\mu$ A	0.4 $\mu$ A (No RTC) $V_{DD}=1.8$ V		0.28 $\mu$ A (No RTC) $V_{DD}=1.8$ V	
					0.8 $\mu$ A (with RTC) $V_{DD}=1.8$ V		0.65 $\mu$ A (with RTC) $V_{DD}=1.8$ V	
					0.4 $\mu$ A (No RTC) $V_{DD}=3.0$ V		0.29 $\mu$ A (No RTC) $V_{DD}=3.0$ V	
					1 $\mu$ A (with RTC) $V_{DD}=3.0$ V		0.85 $\mu$ A (with RTC) $V_{DD}=3.0$ V	

- Legend:  
 "Y" = Yes (enable).  
 "O" = Optional can be enabled/disabled by software)  
 "-" = Not available
- The consumption values given in this table are preliminary data given for indication. They are subject to slight changes.
- Some peripherals with wakeup from Stop capability can request HSI to be enabled. In this case, HSI is woken up by the peripheral, and only feeds the peripheral which requested it. HSI is automatically put off when the peripheral does not need it anymore.
- UART and LPUART reception is functional in Stop mode. It generates a wakeup interrupt on Start. To generate a wakeup on address match or received frame event, the LPUART can run on LSE clock while the UART has to wake up or keep running the HSI clock.
- I2C address detection is functional in Stop mode. It generates a wakeup interrupt in case of address match. It will wake up the HSI during reception.

### 3.3 ARM® Cortex®-M0+ core with MPU

The Cortex-M0+ processor is an entry-level 32-bit ARM Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- a simple architecture that is easy to learn and program
- ultra-low power, energy-efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family
- platform security robustness, with integrated Memory Protection Unit (MPU).

The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to its embedded ARM core, the STM32L072xx are compatible with all ARM tools and software.

#### Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L072xx embed a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels and 4 priority levels.

The Cortex-M0+ processor closely integrates a configurable Nested Vectored Interrupt Controller (NVIC), to deliver industry-leading interrupt performance. The NVIC:

- includes a Non-Maskable Interrupt (NMI)
- provides zero jitter interrupt option
- provides four interrupt priority levels

The tight integration of the processor core and NVIC provides fast execution of Interrupt Service Routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to abandon and restart load-multiple and store-multiple operations. Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that include a deep sleep function that enables the entire device to enter rapidly stop or standby mode.

This hardware block provides flexible interrupt management features with minimal interrupt latency.

independent from the CPU clock, allowing the I2C1/I2C3 to wake up the MCU from Stop mode on address match.

Each I2C interface can be served by the DMA controller.

Refer to [Table 12](#) for an overview of I2C interface features.

**Table 12. STM32L072xx I<sup>2</sup>C implementation**

I2C features <sup>(1)</sup>	I2C1	I2C2	I2C3
7-bit addressing mode	X	X	X
10-bit addressing mode	X	X	X
Standard mode (up to 100 kbit/s)	X	X	X
Fast mode (up to 400 kbit/s)	X	X	X
Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X <sup>(2)</sup>	X
Independent clock	X	-	X
SMBus	X	-	X
Wakeup from STOP	X	-	X

1. X = supported.

2. See [Table 16: STM32L072xxx pin definition on page 43](#) for the list of I/Os that feature Fast Mode Plus capability

### 3.17.2 Universal synchronous/asynchronous receiver transmitter (USART)

The four USART interfaces (USART1, USART2, USART4 and USART5) are able to communicate at speeds of up to 4 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1 and USART2 also support SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock, allowing to wake up the MCU from Stop mode using baudrates up to 42 Kbaud.

All USART interfaces can be served by the DMA controller.

[Table 13](#) for the supported modes and features of USART interfaces.

**Table 13. USART implementation**

USART modes/features <sup>(1)</sup>	USART1 and USART2	USART4 and USART5
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode <sup>(2)</sup>	X	X
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	-

Table 14. SPI/I2S implementation

SPI features <sup>(1)</sup>	SPI1	SPI2
Hardware CRC calculation	X	X
I2S mode	-	X
TI mode	X	X

1. X = supported.

### 3.17.5 Universal serial bus (USB)

The STM32L072xx embeds a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up to 1 KB and suspend/resume support. It requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use a HSE crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which allows crystal-less operation.

## 3.18 Clock recovery system (CRS)

The STM32L072xx embeds a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS\_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

## 3.19 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

## 3.20 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

Table 16. STM32L072xxx pin definition (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32 <sup>(1)</sup>	LQFP48	LQFP64	UFBGA64/TFBGA64	WLCSP49	LQFP100	UFBG100						
-	-	-	-	-	-	46	M12	PE15	I/O	FT	-	SPI1_MOSI	-
-	-	21	29	G7	G3	47	L10	PB10	I/O	FT	-	TIM2_CH3, TSC_SYNC, LPUART1_TX, SPI2_SCK, I2C2_SCL, LPUART1_RX	-
-	-	22	30	H7	F3	48	L11	PB11	I/O	FT	-	EVENTOUT, TIM2_CH4, TSC_G6_IO1, LPUART1_RX, I2C2_SDA, LPUART1_TX	-
16	16	23	31	D6	D4	49	F12	VSS	S		-	-	-
17	17	24	32	E5	G2	50	G12	VDD	S		-	-	-
-	-	25	33	H8	G1	51	L12	PB12	I/O	FT	-	SPI2_NSS/I2S2_WS, LPUART1_RTS_DE, TSC_G6_IO2, I2C2_SMBA, EVENTOUT	-
-	-	26	34	G8	F2	52	K12	PB13	I/O	FTf	-	SPI2_SCK/I2S2_CK, MCO, TSC_G6_IO3, LPUART1_CTS, I2C2_SCL, TIM21_CH1	-
-	-	27	35	F8	F1	53	K11	PB14	I/O	FTf		SPI2_MISO/I2S2_MCK, RTC_OUT, TSC_G6_IO4, LPUART1_RTS_DE, I2C2_SDA, TIM21_CH2	-
-	-	28	36	F7	E1	54	K10	PB15	I/O	FT	-	SPI2_MOSI/I2S2_SD, RTC_REFIN	-
-	-	-	-	-	-	55	K9	PD8	I/O	FT	-	LPUART1_TX	-
-	-	-	-	-	-	56	K8	PD9	I/O	FT	-	LPUART1_RX	-
-	-	-	-	-	-	57	J12	PD10	I/O	FT	-	-	-
-	-	-	-	-	-	58	J11	PD11	I/O	FT	-	LPUART1_CTS	-
-	-	-	-	-	-	59	J10	PD12	I/O	FT	-	LPUART1_RTS_DE	-



Table 16. STM32L072xxx pin definition (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32 <sup>(1)</sup>	LQFP48	LQFP64	UFBGA64/TFBGA64	WLCSP49	LQFP100	UFBG100						
-	24	36	48	E6	A1	75	G11	VDD_USB	S		-	-	-
24	25	37	49	A7	B2	76	A10	PA14	I/O	FT	-	SWCLK, USART2_TX, LPUART1_TX	-
25	-	38	50	A6	A2	77	A9	PA15	I/O	FT	-	SPI1_NSS, TIM2_ETR, EVENTOUT, USART2_RX, TIM2_CH1, USART4_RTS_DE	-
-	-	-	51	B7	-	78	B11	PC10	I/O	FT	-	LPUART1_TX, USART4_TX	-
-	-	-	52	B6	-	79	C10	PC11	I/O	FT	-	LPUART1_RX, USART4_RX	-
-	-	-	53	C5	-	80	B10	PC12	I/O	FT	-	USART5_TX, USART4_CK	-
-	-	-	-	-	-	81	C9	PD0	I/O	FT	-	TIM21_CH1, SPI2_NSS/I2S2_WS	-
-	-	-	-	-	-	82	B9	PD1	I/O	FT	-	SPI2_SCK/I2S2_CK	-
-	-	-	54	B5	-	83	C8	PD2	I/O	FT	-	LPUART1_RTS_DE, TIM3_ETR, USART5_RX	-
-	-	-	-	-	-	84	B8	PD3	I/O	FT	-	USART2_CTS, SPI2_MISO/I2S2_MCK	-
-	-	-	-	-	-	85	B7	PD4	I/O	FT	-	USART2_RTS_DE, SPI2_MOSI/I2S2_SD	-
-	-	-	-	-	-	86	A6	PD5	I/O	FT	-	USART2_TX	-
-	-	-	-	-	-	87	B6	PD6	I/O	FT	-	USART2_RX	-
-	-	-	-	-	-	88	A5	PD7	I/O	FT	-	USART2_CK, TIM21_CH2	-
26	-	39	55	A5	A3	89	A8	PB3	I/O	FT	-	SPI1_SCK, TIM2_CH2, TSC_G5I_O1, EVENTOUT, USART1_RTS_DE, USART5_TX	COMP2_INM

Table 16. STM32L072xxx pin definition (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32 <sup>(1)</sup>	LQFP48	LQFP64	UFBGA64/TFBGA64	WLCSP49	LQFP100	UFBG100						
27	26	40	56	A4	B3	90	A7	PB4	I/O	FTf	-	SPI1_MISO, TIM3_CH1, TSC_G5_IO2, TIM22_CH1, USART1_CTS, USART5_RX, I2C3_SDA	COMP2_INP
28	27	41	57	C4	A4	91	C5	PB5	I/O	FT	-	SPI1_MOSI, LPTIM1_IN1, I2C1_SMBA, TIM3_CH2/TIM22_CH2, USART1_CK, USART5_CK/USART5_R TS_DE	COMP2_INP
29	28	42	58	D3	B4	92	B5	PB6	I/O	FTf	-	USART1_TX, I2C1_SCL, LPTIM1_ETR, TSC_G5_IO3	COMP2_INP
30	29	43	59	C3	C3	93	B4	PB7	I/O	FTf	-	USART1_RX, I2C1_SDA, LPTIM1_IN2, TSC_G5_IO4, USART4_CTS	COMP2_INP, VREF_PVD_IN
31	30	44	60	B4	A5	94	A4	BOOT0	I		-	-	-
-	-	45	61	B3	B5	95	A3	PB8	I/O	FTf	-	TSC_SYNC, I2C1_SCL	-
-	-	46	62	A3	A6	96	B3	PB9	I/O	FTf	-	EVENTOUT, I2C1_SDA, SPI2_NSS/I2S2_WS	-
-	-	-	-	-	-	97	C3	PE0	I/O	FT	-	EVENTOUT	-
-	-	-	-	-	-	98	A2	PE1	I/O	FT	-	EVENTOUT	-
32	31	47	63	D4	-	99	D3	VSS	S	-	-	-	-
-	32	48	64	E4	A7	100	C4	VDD	S	-	-	-	-

1. UFQFPN32 pinout differs from other STM32 devices except STM32L07xxx and STM32L8xxx.

2. PA4 offers a reduced touch sensing sensitivity. It is thus recommended to use it as sampling capacitor I/O.

3. These pins are powered by VDD\_USB. For all characteristics that refer to V<sub>DD</sub>, V<sub>DD\_USB</sub> must be used instead.

Table 17. Alternate functions port A

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/SPI2/I2S2/USART1/2/LPUART1/USB/LPTIM1/TSC/TIM2/21/22/EVENTOUT/SYS_AF	SPI1/SPI2/I2S2/I2C1/TIM2/21	SPI1/SPI2/I2S2/LPUART1/USART5/USB/LPTIM1/TIM2/3/EVENTOUT/SYS_AF	I2C1/TSC/EVENTOUT	I2C1/USART1/2/LPUART1/TIM3/22/EVENTOUT	SPI2/I2S2/I2C2/USART1/TIM2/21/22	I2C1/2/LPUART1/USART4/USART5/TIM21/EVENTOUT	I2C3/LPUART1/COMP1/2/TIM3
Port A	PA0	-	-	TIM2_CH1	TSC_G1_IO1	USART2_CTS	TIM2_ETR	USART4_TX	COMP1_OUT
	PA1	EVENTOUT		TIM2_CH2	TSC_G1_IO2	USART2_RTS_DE	TIM21_ETR	USART4_RX	-
	PA2	TIM21_CH1		TIM2_CH3	TSC_G1_IO3	USART2_TX	-	LPUART1_TX	COMP2_OUT
	PA3	TIM21_CH2		TIM2_CH4	TSC_G1_IO4	USART2_RX	-	LPUART1_RX	-
	PA4	SPI1_NSS	-	-	TSC_G2_IO1	USART2_CK	TIM22_ETR	-	-
	PA5	SPI1_SCK	-	TIM2_ETR	TSC_G2_IO2		TIM2_CH1	-	-
	PA6	SPI1_MISO		TIM3_CH1	TSC_G2_IO3	LPUART1_CTS	TIM22_CH1	EVENTOUT	COMP1_OUT
	PA7	SPI1_MOSI		TIM3_CH2	TSC_G2_IO4	-	TIM22_CH2	EVENTOUT	COMP2_OUT
	PA8	MCO		USB_CR2_SYNC	EVENTOUT	USART1_CK	-	-	I2C3_SCL
	PA9	MCO		-	TSC_G4_IO1	USART1_TX	-	I2C1_SCL	I2C3_SMBA
	PA10	-		-	TSC_G4_IO2	USART1_RX	-	I2C1_SDA	-
	PA11	SPI1_MISO	-	EVENTOUT	TSC_G4_IO3	USART1_CTS	-	-	COMP1_OUT
	PA12	SPI1_MOSI	-	EVENTOUT	TSC_G4_IO4	USART1_RTS_DE	-	-	COMP2_OUT
	PA13	SWDIO	-	USB_OE	-	-	-	LPUART1_RX	-
	PA14	SWCLK	-	-	-	USART2_TX	-	LPUART1_TX	-
	PA15	SPI1_NSS		TIM2_ETR	EVENTOUT	USART2_RX	TIM2_CH1	USART4_RTS_DE	-

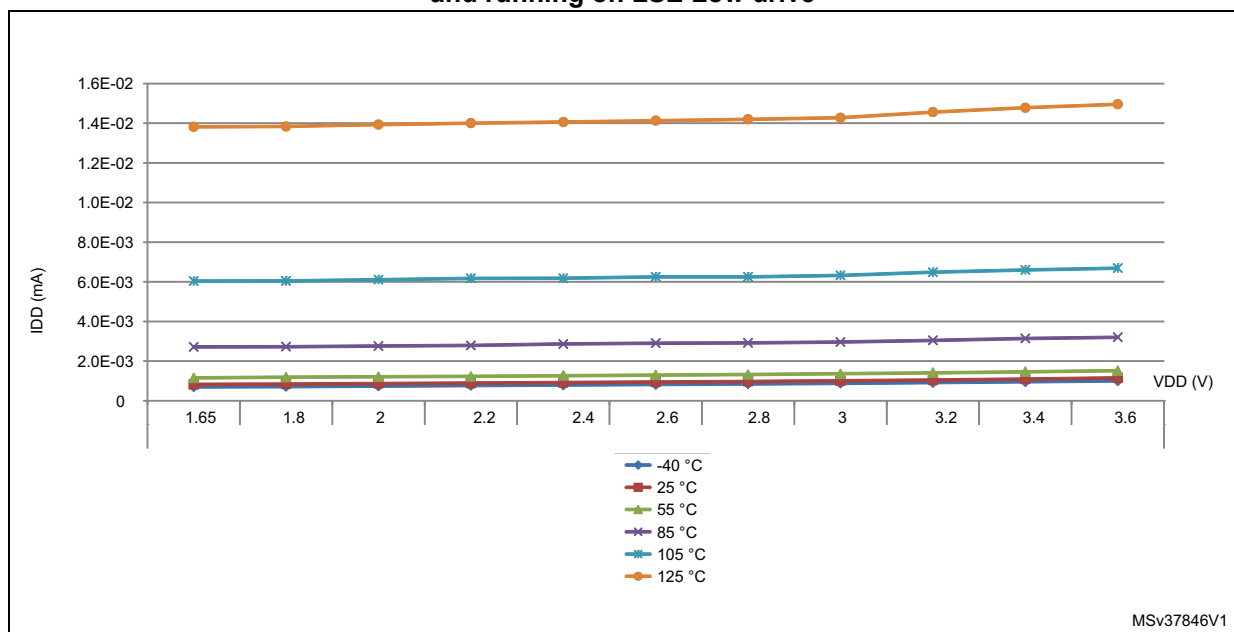
Table 21. Alternate functions port E

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/SPI2/I2S2/ USART1/2/ LPUART1/USB/ LPTIM1/TSC/ TIM2/21/22/ EVENTOUT/ SYS_AF	SPI1/SPI2/I2S2/I2C1 /TIM2/21	SPI1/SPI2/I2S2/ LPUART1/ USART5/USB/ LPTIM1/TIM2/3 /EVENTOUT/ SYS_AF	I2C1/TSC/ EVENTOUT	I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT	SPI2/I2S2 /I2C2/ USART1/ TIM2/21/22	I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/ EVENTOUT	I2C3/LPUART1/ COMP1/2/TIM3
Port E	PE0	-		EVENTOUT	-	-	-	-	-
	PE1	-		EVENTOUT	-	-	-	-	-
	PE2	-		TIM3_ETR	-	-	-	-	-
	PE3	TIM22_CH1		TIM3_CH1	-	-	-	-	-
	PE4	TIM22_CH2	-	TIM3_CH2	-	-	-	-	-
	PE5	TIM21_CH1	-	TIM3_CH3	-	-	-	-	-
	PE6	TIM21_CH2	-	TIM3_CH4	-	-	-	-	-
	PE7	-		-	-	-	-	USART5_CK/U SART5_RTS_D E	-
	PE8	-		-	-	-	-	USART4_TX	-
	PE9	TIM2_CH1		TIM2_ETR	-	-	-	USART4_RX	-
	PE10	TIM2_CH2		-	-	-	-	USART5_TX	-
	PE11	TIM2_CH3	-	-	-	-	-	USART5_RX	-
	PE12	TIM2_CH4	-	SPI1_NSS	-	-	-	-	-
	PE13	-		SPI1_SCK	-	-	-	-	-
	PE14	-		SPI1_MISO	-	-	-	-	-
	PE15	-		SPI1_MOSI	-	-	-	-	-

Table 37. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max <sup>(1)</sup>	Unit
$I_{DD}$ (Stop)	Supply current in Stop mode	$T_A = -40$ to $25^\circ\text{C}$	0,43	1,00	$\mu\text{A}$
		$T_A = 55^\circ\text{C}$	0,735	2,50	
		$T_A = 85^\circ\text{C}$	2,25	4,90	
		$T_A = 105^\circ\text{C}$	5,3	13,00	
		$T_A = 125^\circ\text{C}$	12,5	28,00	

1. Guaranteed by characterization results at  $125^\circ\text{C}$ , unless otherwise specified.

Figure 19.  $I_{DD}$  vs  $V_{DD}$ , at  $T_A = 25/55/ 85/105/125^\circ\text{C}$ , Stop mode with RTC enabled and running on LSE Low drive

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

#### Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

#### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

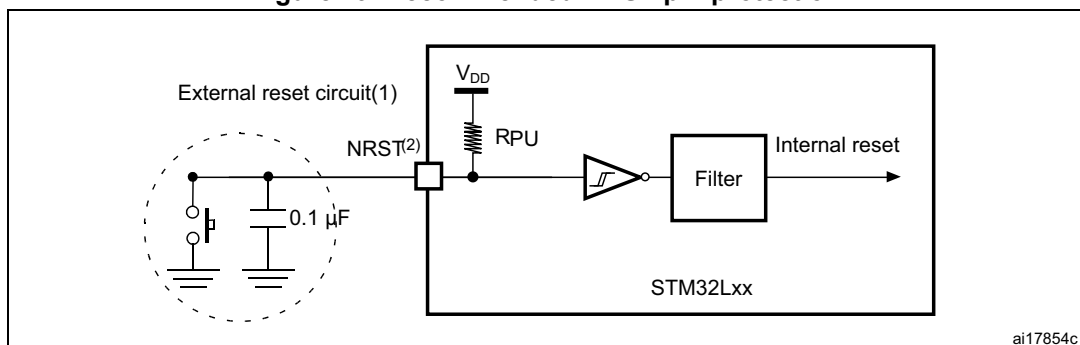
### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 56. EMI characteristics**

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. frequency range at 32 MHz	Unit
S <sub>EMI</sub>	Peak level	V <sub>DD</sub> = 3.6 V, T <sub>A</sub> = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	-7	dBμV
			30 to 130 MHz	14	
			130 MHz to 1 GHz	9	
			EMI Level	2	-

Figure 29. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the  $V_{IL(NRST)}$  max level specified in [Table 63](#). Otherwise the reset will not be taken into account by the device.

### 6.3.15 12-bit ADC characteristics

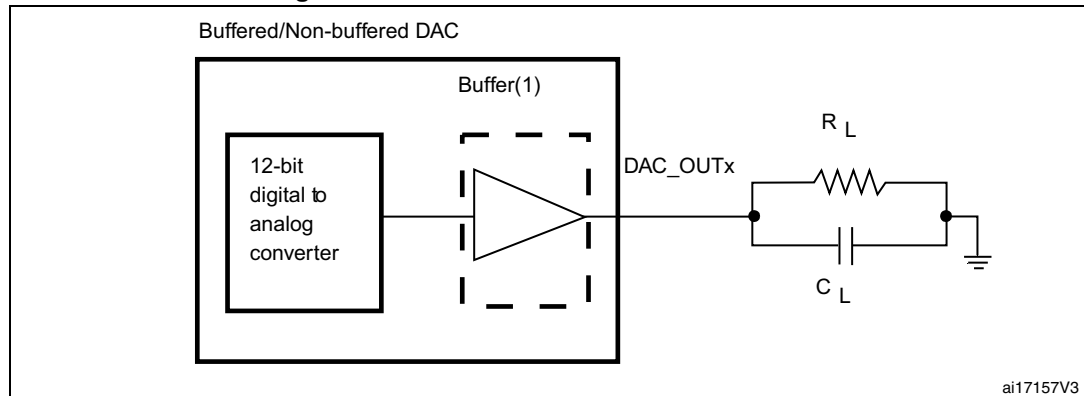
Unless otherwise specified, the parameters given in [Table 64](#) are derived from tests performed under ambient temperature,  $f_{PCLK}$  frequency and  $V_{DDA}$  supply voltage conditions summarized in [Table 26: General operating conditions](#).

**Note:** It is recommended to perform a calibration after each power-up.

Table 64. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DDA}$	Analog supply voltage for ADC on	Fast channel	1.65	-	3.6	V
		Standard channel	1.75 <sup>(1)</sup>	-	3.6	
$V_{REF+}$	Positive reference voltage	-	1.65		$V_{DDA}$	V
$V_{REF-}$	Negative reference voltage	-	-	0	-	
$I_{DDA(ADC)}$	Current consumption of the ADC on $V_{DDA}$ and $V_{REF+}$	1.14 Msps	-	200	-	µA
		10 ksps	-	40	-	
	Current consumption of the ADC on $V_{DD}$ <sup>(2)</sup>	1.14 Msps	-	70	-	
		10 ksps	-	1	-	
$f_{ADC}$	ADC clock frequency	Voltage scaling Range 1	0.14	-	16	MHz
		Voltage scaling Range 2	0.14	-	8	
		Voltage scaling Range 3	0.14	-	4	
$f_S^{(3)}$	Sampling rate	12-bit resolution	0.01	-	1.14	MHz
$f_{TRIG}^{(3)}$	External trigger frequency	$f_{ADC} = 16$ MHz, 12-bit resolution	-	-	941	kHz
		-	-	-	17	1/ $f_{ADC}$
$V_{AIN}$	Conversion voltage range	-	0	-	$V_{REF+}$	V
$R_{AIN}^{(3)}$	External input impedance	See <a href="#">Equation 1</a> and <a href="#">Table 65</a> for details	-	-	50	kΩ
$R_{ADC}^{(3)(4)}$	Sampling switch resistance	-	-	-	1	kΩ

6. Difference between the value measured at Code (0x800) and the ideal value =  $V_{REF+}/2$ .
7. Difference between the value measured at Code (0x001) and the ideal value.
8. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFFF when buffer is off, and from code giving 0.2 V and ( $V_{DDA} - 0.2$ ) V when buffer is on.
9. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

**Figure 34. 12-bit buffered/non-buffered DAC**

### 6.3.17 Temperature sensor characteristics

**Table 68. Temperature sensor calibration values**

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, $V_{DDA} = 3$ V	0x1FF8 007A - 0x1FF8 007B
TS_CAL2	TS ADC raw data acquired at temperature of 130 °C, $V_{DDA} = 3$ V	0x1FF8 007E - 0x1FF8 007F

**Table 69. Temperature sensor characteristics**

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	$V_{SENSE}$ linearity with temperature	-	$\pm 1$	$\pm 2$	°C
Avg_Slope <sup>(1)</sup>	Average slope	1.48	1.61	1.75	mV/°C
$V_{130}$	Voltage at 130°C $\pm 5^\circ\text{C}^{(2)}$	640	670	700	mV
$I_{DDA(TEMP)}^{(3)}$	Current consumption	-	3.4	6	μA
$t_{START}^{(3)}$	Startup time	-	-	10	μs
$T_{S\_temp}^{(4)(3)}$	ADC sampling time when reading the temperature	10	-	-	

1. Guaranteed by characterization results.

2. Measured at  $V_{DD} = 3$  V  $\pm 10$  mV.  $V_{130}$  ADC conversion result is stored in the TS\_CAL2 byte.

3. Guaranteed by design.

4. Shortest sampling time can be determined in the application by multiple iterations.



## 6.3.19 Timer characteristics

### TIM timer characteristics

The parameters given in the [Table 72](#) are guaranteed by design.

Refer to [Section 6.3.13: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 72. TIMx characteristics<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{\text{res(TIM)}}$	Timer resolution time		1	-	$t_{\text{TIMxCLK}}$
		$f_{\text{TIMxCLK}} = 32 \text{ MHz}$	31.25	-	ns
$f_{\text{EXT}}$	Timer external clock frequency on CH1 to CH4		0	$f_{\text{TIMxCLK}}/2$	MHz
		$f_{\text{TIMxCLK}} = 32 \text{ MHz}$	0	16	MHz
$\text{Res}_{\text{TIM}}$	Timer resolution	-		16	bit
$t_{\text{COUNTER}}$	16-bit counter clock period when internal clock is selected (timer's prescaler disabled)	-	1	65536	$t_{\text{TIMxCLK}}$
		$f_{\text{TIMxCLK}} = 32 \text{ MHz}$	0.0312	2048	$\mu\text{s}$
$t_{\text{MAX\_COUNT}}$	Maximum possible count	-	-	$65536 \times 65536$	$t_{\text{TIMxCLK}}$
		$f_{\text{TIMxCLK}} = 32 \text{ MHz}$	-	134.2	s

1. TIMx is used as a general term to refer to the TIM2, TIM6, TIM21, and TIM22 timers.

## 6.3.20 Communications interfaces

### I<sup>2</sup>C interface characteristics

The I<sup>2</sup>C interface meets the timings requirements of the I<sup>2</sup>C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm) : with a bit rate up to 100 kbit/s
- Fast-mode (Fm) : with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+) : with a bit rate up to 1 Mbit/s.

The I<sup>2</sup>C timing requirements are guaranteed by design when the I<sup>2</sup>C peripheral is properly configured (refer to the reference manual for details). The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement (refer to [Section 6.3.13: I/O port characteristics](#) for the I2C I/Os characteristics).

All I<sup>2</sup>C SDA and SCL I/Os embed an analog filter (see [Table 73](#) for the analog filter characteristics).

## I2S characteristics

Table 78. I2S characteristics<sup>(1)</sup>

Symbol	Parameter	Conditions	Min	Max	Unit
$f_{MCK}$	I2S Main clock output	-	256 x 8K	256x $F_s$ <sup>(2)</sup>	MHz
$f_{CK}$	I2S clock frequency	Master data: 32 bits	-	64x $F_s$	MHz
		Slave data: 32 bits	-	64x $F_s$	
$D_{CK}$	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	-	15	ns
$t_{h(WS)}$	WS hold time	Master mode	11	-	
$t_{su(WS)}$	WS setup time	Slave mode	6	-	
$t_{h(WS)}$	WS hold time	Slave mode	2	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	0	-	
$t_{su(SD\_SR)}$		Slave receiver	6.5	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	18	-	
$t_{h(SD\_SR)}$		Slave receiver	15.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	77	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	8	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	18	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	1.5	-	

1. Guaranteed by characterization results.

2. 256x $F_s$  maximum value is equal to the maximum clock frequency.

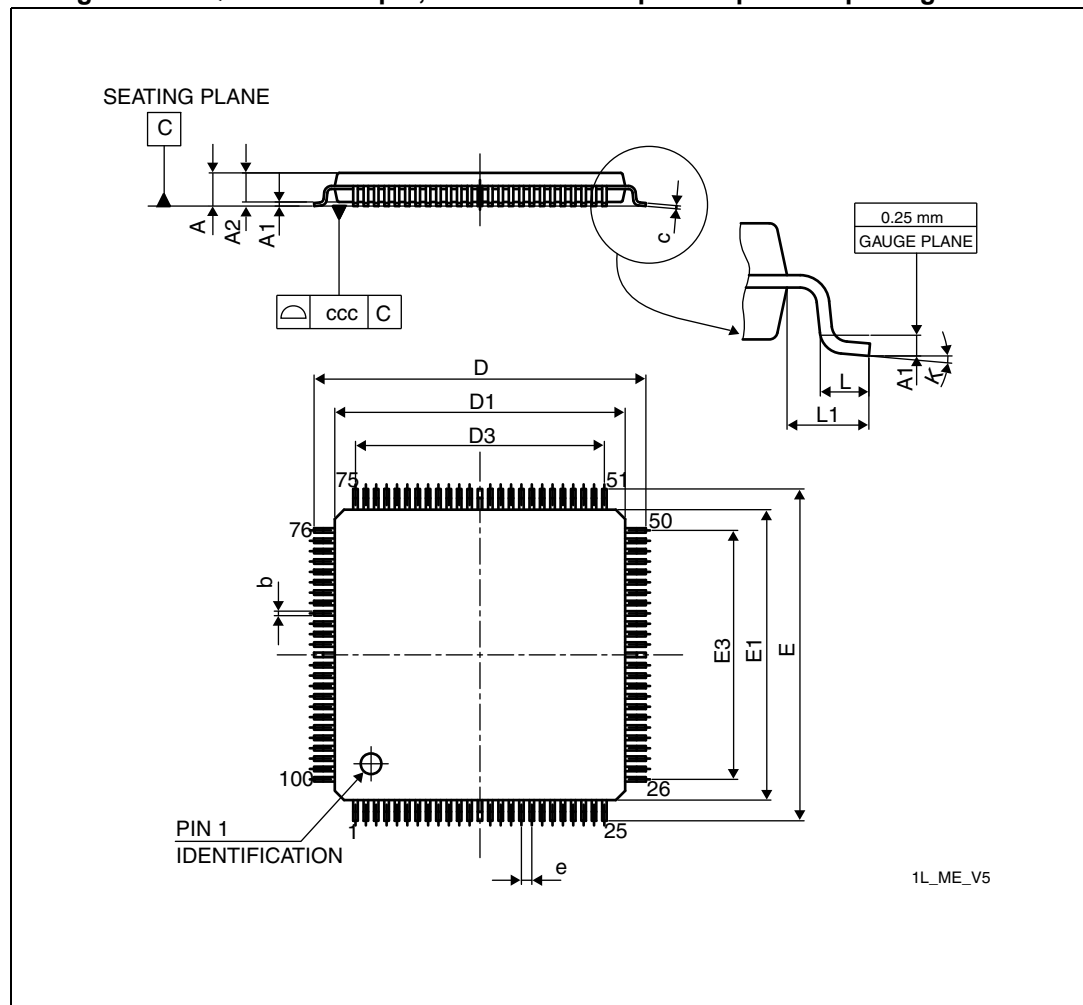
**Note:** Refer to the I2S section of the product reference manual for more details about the sampling frequency ( $F_s$ ),  $f_{MCK}$ ,  $f_{CK}$  and  $D_{CK}$  values. These values reflect only the digital peripheral behavior, source clock precision might slightly change them.  $D_{CK}$  depends mainly on the ODD bit value, digital contribution leads to a min of  $(I2SDIV/(2*I2SDIV+ODD))$  and a max of  $(I2SDIV+ODD)/(2*I2SDIV+ODD)$ .  $F_s$  max is supported for each mode/condition.

## 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status *are available at* [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 7.1 LQFP100 package information

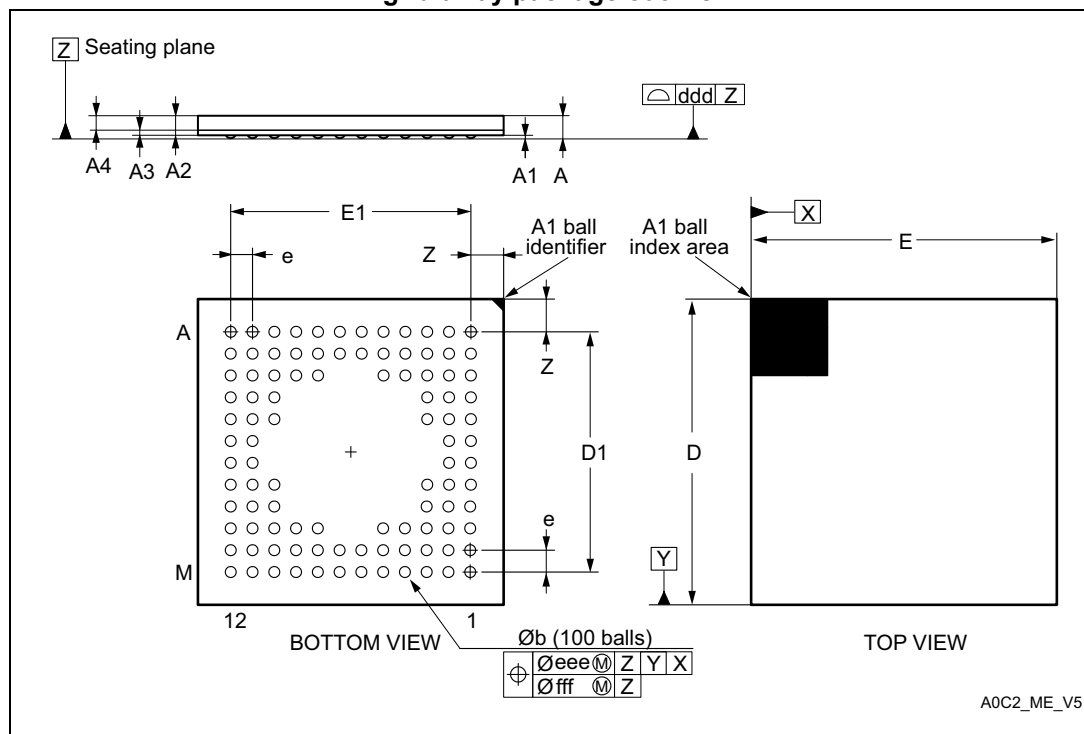
Figure 41. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale. Dimensions are in millimeters.

## 7.2 UFBGA100 package information

Figure 43. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

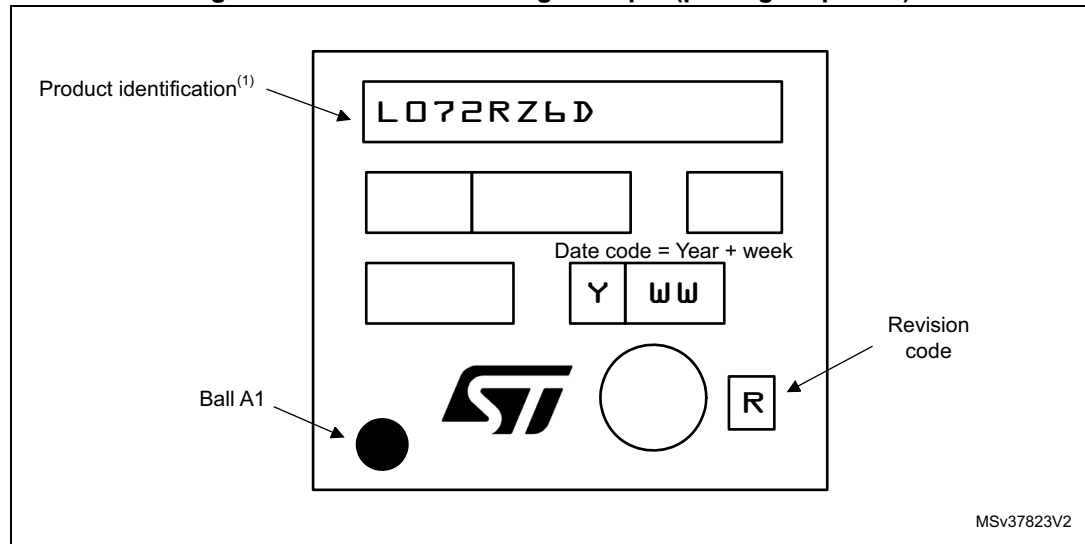
Table 83. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches <sup>(1)</sup>		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-

### Device marking for TFBGA64

The following figure gives an example of topside marking versus ball A 1 position identifier location.

**Figure 53. TFBGA64 marking example (package top view)**



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.