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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	51
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA
Supplier Device Package	64-UFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l072rzi6dtr

2 Description

The ultra-low-power STM32L072xx microcontrollers incorporate the connectivity power of the universal serial bus (USB 2.0 crystal-less) with the high-performance ARM® Cortex®-M0+ 32-bit RISC core operating at a 32 MHz frequency, a memory protection unit (MPU), high-speed embedded memories (up to 192 Kbytes of Flash program memory, 6 Kbytes of data EEPROM and 20 Kbytes of RAM) plus an extensive range of enhanced I/Os and peripherals.

The STM32L072xx devices provide high power efficiency for a wide range of performance. It is achieved with a large choice of internal and external clock sources, an internal voltage adaptation and several low-power modes.

The STM32L072xx devices offer several analog features, one 12-bit ADC with hardware oversampling, two DACs, two ultra-low-power comparators, several timers, one low-power timer (LPTIM), four general-purpose 16-bit timers and two basic timer, one RTC and one SysTick which can be used as timebases. They also feature two watchdogs, one watchdog with independent clock and window capability and one window watchdog based on bus clock.

Moreover, the STM32L072xx devices embed standard and advanced communication interfaces: up to three I2Cs, two SPIs, one I2S, four USARTs, a low-power UART (LPUART), and a crystal-less USB. The devices offer up to 24 capacitive sensing channels to simply add touch sensing functionality to any application.

The STM32L072xx also include a real-time clock and a set of backup registers that remain powered in Standby mode.

The ultra-low-power STM32L072xx devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +125 °C temperature range. A comprehensive set of power-saving modes allows the design of low-power applications.

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (continued)(1)(2)

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
Temperature sensor	O	O	O	O	O		--	
Comparators	O	O	O	O	O	O	--	
16-bit timers	O	O	O	O	--		--	
LPTIMER	O	O	O	O	O	O		
IWDG	O	O	O	O	O	O	O	O
WWDG	O	O	O	O	--		--	
Touch sensing controller (TSC)	O	O	--	--	--		--	
SysTick Timer	O	O	O	O			--	
GPIOs	O	O	O	O	O	O		2 pins
Wakeup time to Run mode	0 µs	0.36 µs	3 µs	32 µs	3.5 µs		50 µs	
Consumption V_{DD}=1.8 to 3.6 V (Typ)	Down to 140 µA/MHz (from Flash memory)	Down to 37 µA/MHz (from Flash memory)	Down to 8 µA	Down to 4.5 µA	0.4 µA (No RTC) V_{DD}=1.8 V		0.28 µA (No RTC) V_{DD}=1.8 V	
					0.8 µA (with RTC) V_{DD}=1.8 V		0.65 µA (with RTC) V_{DD}=1.8 V	
					0.4 µA (No RTC) V_{DD}=3.0 V		0.29 µA (No RTC) V_{DD}=3.0 V	
					1 µA (with RTC) V_{DD}=3.0 V		0.85 µA (with RTC) V_{DD}=3.0 V	

1. Legend:
   “Y” = Yes (enable).
   “O” = Optional can be enabled/disabled by software)
   “-” = Not available
2. The consumption values given in this table are preliminary data given for indication. They are subject to slight changes.
3. Some peripherals with wakeup from Stop capability can request HSI to be enabled. In this case, HSI is woken up by the peripheral, and only feeds the peripheral which requested it. HSI is automatically put off when the peripheral does not need it anymore.
4. UART and LPUART reception is functional in Stop mode. It generates a wakeup interrupt on Start. To generate a wakeup on address match or received frame event, the LPUART can run on LSE clock while the UART has to wake up or keep running the HSI clock.
5. I2C address detection is functional in Stop mode. It generates a wakeup interrupt in case of address match. It will wake up the HSI during reception.

3.8 Memories

The STM32L072xx devices have the following features:

- 20 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 64, 128 or 192 Kbytes of embedded Flash program memory
  - 6 Kbytes of data EEPROM
  - Information block containing 32 user and factory options bytes plus 8 Kbytes of system memory

Flash program and data EEPROM are divided into two banks. This allows writing in one bank while running code or reading data from the other bank.

The user options bytes are used to write-protect or read-out protect the memory (with 4 Kbyte granularity) and/or readout-protect the whole memory with the following options:

- **Level 0**: no protection
- **Level 1**: memory readout protected.

  The Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- **Level 2**: chip readout protected, debug features (Cortex-M0+ serial wire) and boot in RAM selection disabled (debugline fuse)

The firewall protects parts of code/data from access by the rest of the code that is executed outside of the protected area. The granularity of the protected code segment or the non-volatile data segment is 256 bytes (Flash memory or EEPROM) against 64 bytes for the volatile data segment (RAM).

The whole non-volatile memory embeds the error correction code (ECC) feature.

3.9 Boot modes

At startup, BOOT0 pin and nBOOT1 option bit are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using USB (PA11, PA12), USART1(PA9, PA10) or USART2(PA2, PA3). See STM32™ microcontroller system memory boot mode AN2606 for details.

3.10 Direct memory access (DMA)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, LPUART, general-purpose timers, DAC, and ADC.

3.11 Analog-to-digital converter (ADC)

A native 12-bit, extended to 16-bit through hardware oversampling, analog-to-digital converter is embedded into STM32L072xx device. It has up to 16 external channels and 3 internal channels (temperature sensor, voltage reference). Three channels, PA0, PA4 and PA5, are fast channels, while the others are standard channels.

The ADC performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of 1.14 MSPS even with a low CPU speed. The ADC consumption is low at all frequencies (~25 µA at 10 kSPS, ~240 µA at 1MSPS). An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.

The ADC can be served by the DMA controller. It can operate from a supply voltage down to 1.65 V.

The ADC features a hardware oversampler up to 256 samples, this improves the resolution to 16 bits (see AN2668).

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers.

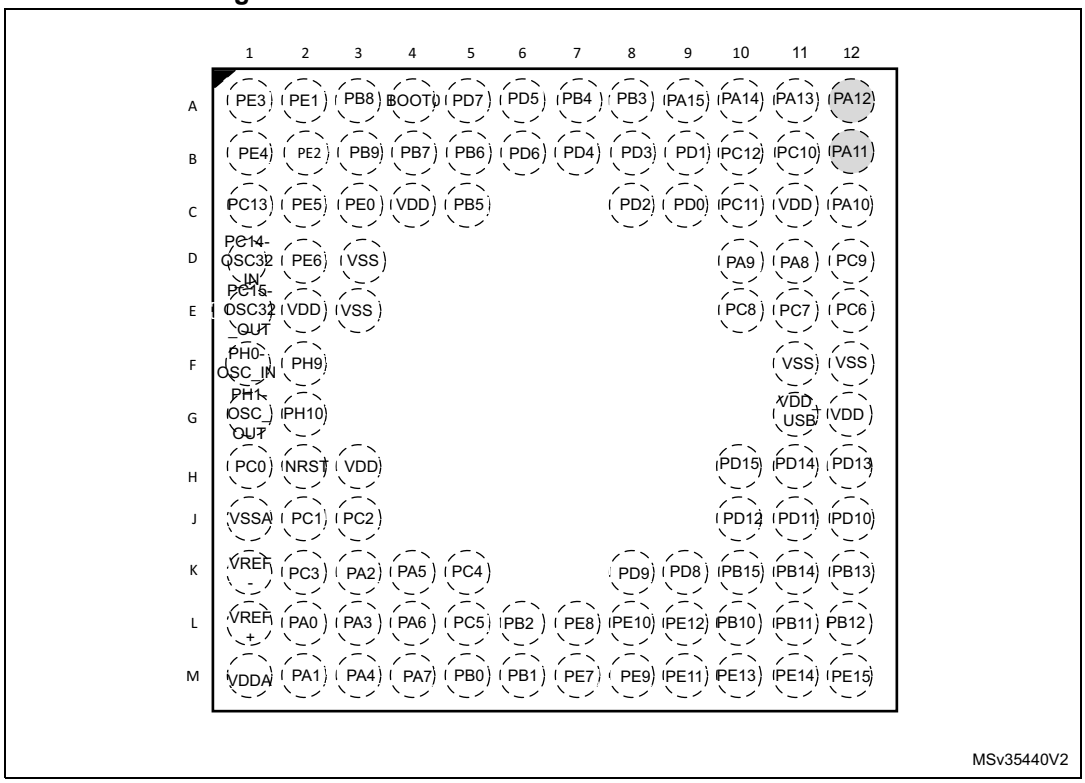
3.12 Temperature sensor

The temperature sensor (T_{SENSE}) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value.

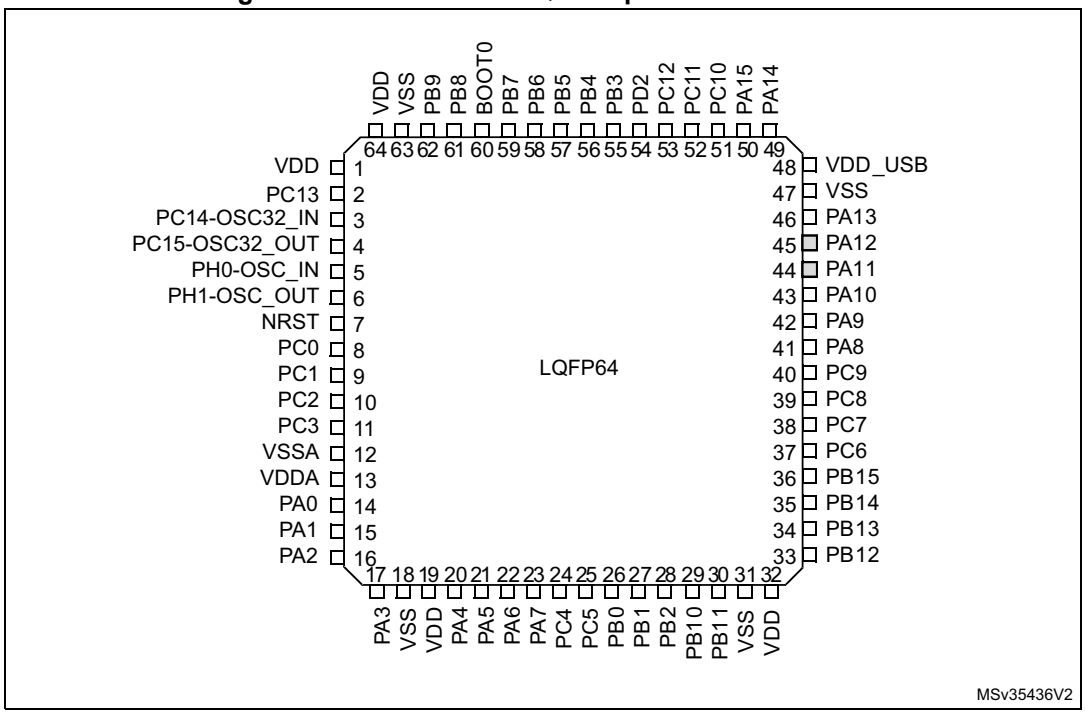
The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

Figure 4. STM32L072xx UFBGA100 ballout - 7x 7 mm



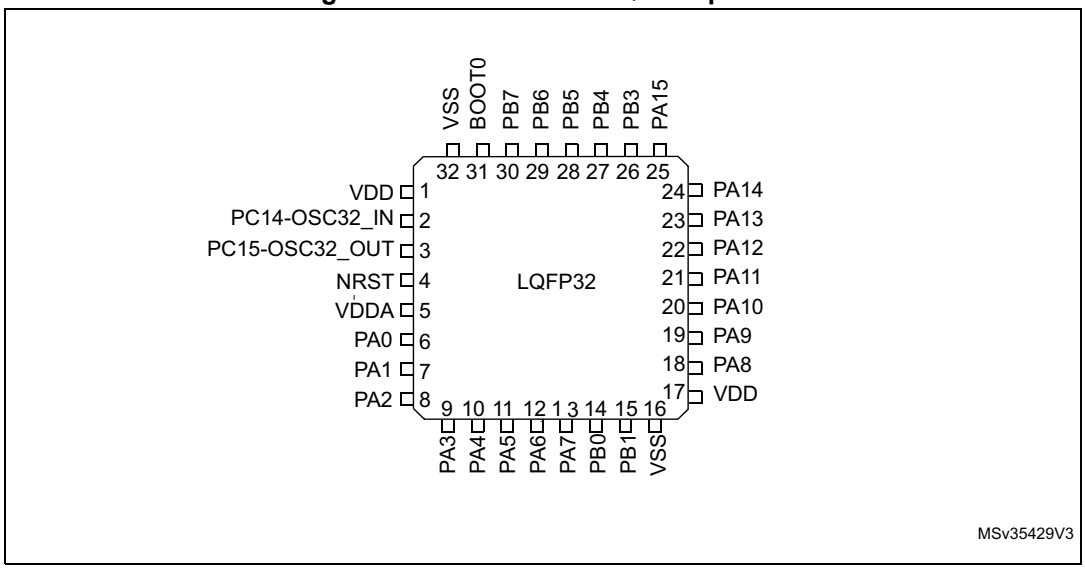
1. The above figure shows the package top view.
2. I/O pin supplied by VDD_USB.

Figure 5. STM32L072xx LQFP64 pinout - 10 x 10 mm



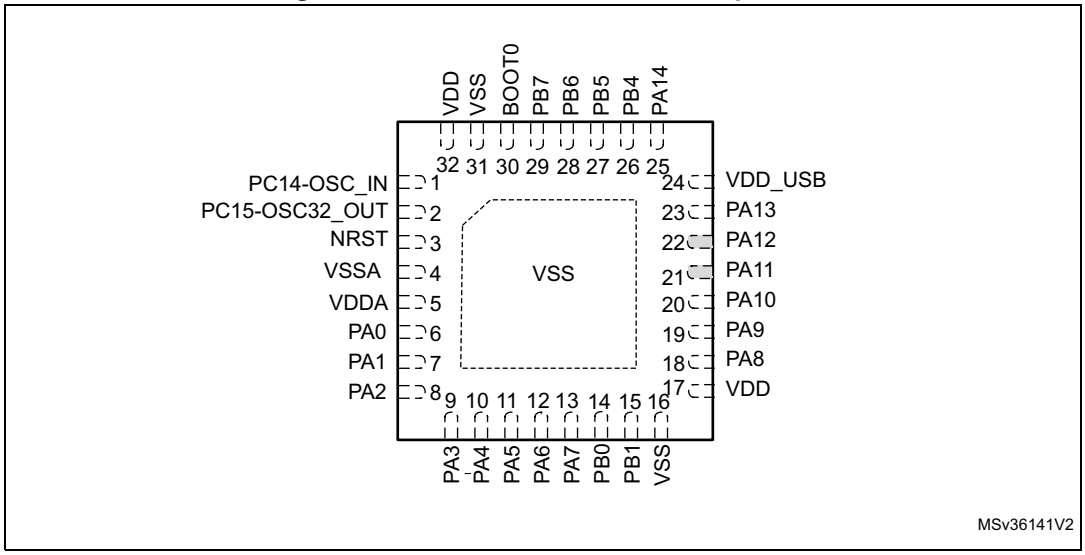
1. The above figure shows the package top view.
2. I/O pin supplied by VDD_USB.

Figure 9. STM32L072xx LQFP32 pinout



1. The above figure shows the package top view.

Figure 10. STM32L072xx UFQFPN32 pinout



1. The above figure shows the package top view.
2. I/O pin supplied by VDD_USB.

Table 16. STM32L072xxx pin definition (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32[1]	LQFP48	LQFP64	UFBGA64/TFBGA64	WLCSP49	LQFP100	UFBG100						
-	-	2	2	A2	B7	7	C1	PC13	I/O	FT	-	-	RTC_TAMP1/RTC_TS/ RTC_OUT/WKUP2
2	1	3	3	A1	C6	8	D1	PC14-OSC32_IN (PC14)	I/O	FT	-	-	OSC32_IN
3	2	4	4	B1	C7	9	E1	PC15-OSC32_OUT (PC15)	I/O	TC	-	-	OSC32_OUT
-	-	-	-	-	-	10	F2	PH9	I/O	FT	-	-	-
-	-	-	-	-	-	11	G2	PH10	I/O	FT	-	-	-
-	-	5	5	C1	D6	12	F1	PH0-OSC_IN (PH0)	I/O	TC	-	USB_CRS_SYNC	OSC_IN
-	-	6	6	D1	D7	13	G1	PH1-OSC_OUT (PH1)	I/O	TC	-	-	OSC_OUT
4	3	7	7	E1	D5	14	H2	NRST	I/O		-	-	-
-	-	-	8	E3	C5	15	H1	PC0	I/O	FTf	-	LPTIM1_IN1, EVENTOUT, TSC_G7_IO1, LPUART1_RX, I2C3_SCL	ADC_IN10
-	-	-	9	E2	C4	16	J2	PC1	I/O	FTf	-	LPTIM1_OUT, EVENTOUT, TSC_G7_IO2, LPUART1_TX, I2C3_SDA	ADC_IN11
-	-	-	10	F2	E7	17	J3	PC2	I/O	FTf	-	LPTIM1_IN2, SPI2_MISO/I2S2_MCK, TSC_G7_IO3	ADC_IN12
-	-	-	11	-	-	18	K2	PC3	I/O	FT	-	LPTIM1_ETR, SPI2_MOSI/I2S2_SD, TSC_G7_IO4	ADC_IN13
-	4	8	12	F1	-	19	J1	VSSA	S		-	-	-

Table 16. STM32L072xxx pin definition (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32[1]	LQFP48	LQFP64	UFBGA64/TFBGA64	WLCSP49	LQFP100	UFBG100						
-	-	-	-	-	-	46	M12	PE15	I/O	FT	-	SPI1_MOSI	-
-	-	21	29	G7	G3	47	L10	PB10	I/O	FT	-	TIM2_CH3, TSC_SYNC, LPUART1_TX, SPI2_SCK, I2C2_SCL, LPUART1_RX	-
-	-	22	30	H7	F3	48	L11	PB11	I/O	FT	-	EVENTOUT, TIM2_CH4, TSC_G6_IO1, LPUART1_RX, I2C2_SDA, LPUART1_TX	-
16	16	23	31	D6	D4	49	F12	VSS	S		-	-	-
17	17	24	32	E5	G2	50	G12	VDD	S		-	-	-
-	-	25	33	H8	G1	51	L12	PB12	I/O	FT	-	SPI2_NSS/I2S2_WS, LPUART1_RTS_DE, TSC_G6_IO2, I2C2_SMBA, EVENTOUT	-
-	-	26	34	G8	F2	52	K12	PB13	I/O	FTf	-	SPI2_SCK/I2S2_CK, MCO, TSC_G6_IO3, LPUART1_CTS, I2C2_SCL, TIM21_CH1	-
-	-	27	35	F8	F1	53	K11	PB14	I/O	FTf		SPI2_MISO/I2S2_MCK, RTC_OUT, TSC_G6_IO4, LPUART1_RTS_DE, I2C2_SDA, TIM21_CH2	-
-	-	28	36	F7	E1	54	K10	PB15	I/O	FT	-	SPI2_MOSI/I2S2_SD, RTC_REFIN	-
-	-	-	-	-	-	55	K9	PD8	I/O	FT	-	LPUART1_TX	-
-	-	-	-	-	-	56	K8	PD9	I/O	FT	-	LPUART1_RX	-
-	-	-	-	-	-	57	J12	PD10	I/O	FT	-	-	-
-	-	-	-	-	-	58	J11	PD11	I/O	FT	-	LPUART1_CTS	-
-	-	-	-	-	-	59	J10	PD12	I/O	FT	-	LPUART1_RTS_DE	-

Table 16. STM32L072xxx pin definition (continued)

Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32(1)	LQFP48	LQFP64	UFBGA64/TFBGA64	WLCSP49	LQFP100	UFBG100						
27	26	40	56	A4	B3	90	A7	PB4	I/O	FTf	-	SPI1_MISO, TIM3_CH1, TSC_G5_IO2, TIM22_CH1, USART1_CTS, USART5_RX, I2C3_SDA	COMP2_INP
28	27	41	57	C4	A4	91	C5	PB5	I/O	FT	-	SPI1_MOSI, LPTIM1_IN1, I2C1_SMBA, TIM3_CH2/TIM22_CH2, USART1_CK, USART5_CK/USART5_RTS_DE	COMP2_INP
29	28	42	58	D3	B4	92	B5	PB6	I/O	FTf	-	USART1_TX, I2C1_SCL, LPTIM1_ETR, TSC_G5_IO3	COMP2_INP
30	29	43	59	C3	C3	93	B4	PB7	I/O	FTf	-	USART1_RX, I2C1_SDA, LPTIM1_IN2, TSC_G5_IO4, USART4_CTS	COMP2_INP, VREF_PVD_IN
31	30	44	60	B4	A5	94	A4	BOOT0	I		-	-	-
-	-	45	61	B3	B5	95	A3	PB8	I/O	FTf	-	TSC_SYNC, I2C1_SCL	-
-	-	46	62	A3	A6	96	B3	PB9	I/O	FTf	-	EVENTOUT, I2C1_SDA, SPI2_NSS/I2S2_WS	-
-	-	-	-	-	-	97	C3	PE0	I/O	FT	-	EVENTOUT	-
-	-	-	-	-	-	98	A2	PE1	I/O	FT	-	EVENTOUT	-
32	31	47	63	D4	-	99	D3	VSS	S	-	-	-	-
-	32	48	64	E4	A7	100	C4	VDD	S	-	-	-	-

1. UFQFPN32 pinout differs from other STM32 devices except STM32L07xxx and STM32L8xxx.
2. PA4 offers a reduced touch sensing sensitivity. It is thus recommended to use it as sampling capacitor I/O.
3. These pins are powered by VDD_USB. For all characteristics that refer to V_{DD}, V_{DD_USB} must be used instead.

Table 32. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Condition		f_{HCLK} (MHz)	Typ	Max(1)	Unit
I_{DD} (Run from RAM)	Supply current in Run mode code executed from RAM, Flash memory switched off	$f_{HSE} = f_{HCLK}$ up to 16 MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range3, Vcore=1.2 V VOS[1:0]=11	1	175	230	µA
				2	315	360	
				4	570	630	
			Range2, Vcore=1.5 V VOS[1:0]=10	4	0,71	0,78	mA
				8	1,35	1,6	
				16	2,7	3	
			Range1, Vcore=1.8 V VOS[1:0]=01	8	1,7	1,9	
				16	3,2	3,7	
				32	6,65	7,1	
		MSI clock	Range3, Vcore=1.2 V VOS[1:0]=11	0,065	38	98	µA
				0,524	105	160	
				4,2	615	710	
		HSI clock source (16 MHz)	Range2, Vcore=1.5 V VOS[1:0]=10	16	2,85	3	mA
			Range1, Vcore=1.8 V VOS[1:0]=01	32	6,85	7,3	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 33. Current consumption in Run mode vs code type, code with data processing running from RAM(1)

Symbol	Parameter	Conditions			f_{HCLK}	Typ	Unit
I_{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash memory switched off	$f_{HSE} = f_{HCLK}$ up to 16 MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL on)(2)	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	Dhrystone	4 MHz	570	µA
				CoreMark		670	
				Fibonacci		410	
				while(1)		375	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	Dhrystone	32 MHz	6,65	mA
				CoreMark		6,95	
				Fibonacci		5,9	
				while(1)		5,2	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 39. Average current consumption during Wakeup

Symbol	parameter	System frequency	Current consumption during wakeup	Unit
I_{DD} (Wakeup from Stop)	Supply current during Wakeup from Stop mode	HSI	1	mA
		HSI/4	0,7	
		MSI clock = 4,2 MHz	0,7	
		MSI clock = 1,05 MHz	0,4	
		MSI clock = 65 KHz	0,1	
I_{DD} (Reset)	Reset pin pulled down	-	0,21	
I_{DD} (Power-up)	BOR on	-	0,23	
I_{DD} (Wakeup from StandBy)	With Fast wakeup set	MSI clock = 2,1 MHz	0,5	
	With Fast wakeup disabled	MSI clock = 2,1 MHz	0,12	

Table 40. Peripheral current consumption in Run or Sleep mode(1) (continued)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	Low-power sleep and run	
APB2	ADC1(2)	5.5	5	3.5	4	µA/MHz (f_{HCLK})
	SPI1	4	3	3	2.5	
	USART1	14.5	11.5	9.5	12	
	TIM21	7.5	6	5	5.5	
	TIM22	7	6	5	6	
	FIREWALL	1.5	1	1	0.5	
	DBGMCU	1.5	1	1	0.5	
	SYSCFG	2.5	2	2	1.5	
Cortex-M0+ core I/O port	GPIOA	3.5	3	2.5	2.5	µA/MHz (f_{HCLK})
	GPIOB	3.5	2.5	2	2.5	
	GPIOC	8.5	6.5	5.5	7	
	GPIOD	1	0.5	0.5	0.5	
	GPIOE	8	6	5	6	
	GPIOH	1.5	1	1	0.5	
AHB	CRC	1.5	1	1	1	µA/MHz (f_{HCLK})
	FLASH	0(3)	0(3)	0(3)	0(3)	
	DMA1	10	8	6.5	8.5	
	RNG	5.5	1	0.5	0.5	
	TSC	3	2.5	2	3	
All enabled		204	162	130	202	µA/MHz (f_{HCLK})
PWR		2.5	2	2	1	µA/MHz (f_{HCLK})

1. Data based on differential I_{DD} measurement between all peripherals off an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz (range 1), f_{HCLK} = 16 MHz (range 2), f_{HCLK} = 4 MHz (range 3), f_{HCLK} = 64kHz (Low-power run/sleep), $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.
2. HSI oscillator is off for this measure.
3. Current consumption is negligible and close to 0 µA.

6.3.7 Internal clock source characteristics

The parameters given in *Table 47* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 26*.

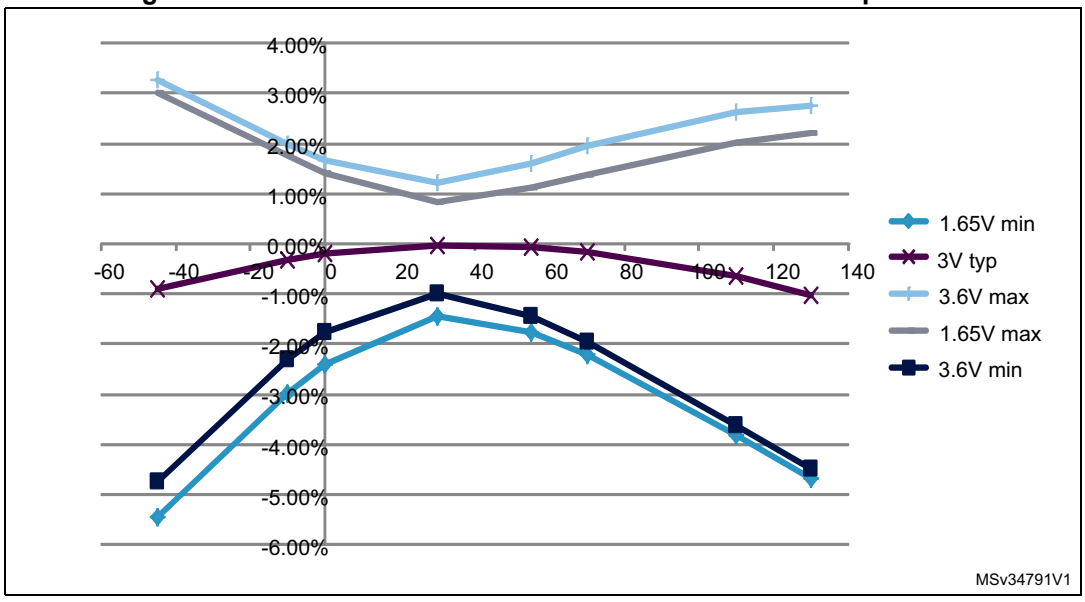
High-speed internal 16 MHz (HSI16) RC oscillator

Table 47. 16 MHz HSI16 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
$TRIM^{(1)(2)}$	HSI16 user-trimmed resolution	Trimming code is not a multiple of 16	-	± 0.4	0.7	%
		Trimming code is a multiple of 16	-	-	± 1.5	%
$ACC_{HSI16}^{(2)}$	Accuracy of the factory-calibrated HSI16 oscillator	V_{DDA} = 3.0 V, T_A = 25 °C	-1(3)	-	1(3)	%
		V_{DDA} = 3.0 V, T_A = 0 to 55 °C	-1.5	-	1.5	%
		V_{DDA} = 3.0 V, T_A = -10 to 70 °C	-2	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 85 °C	-2.5	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 105 °C	-4	-	2	%
		V_{DDA} = 1.65 V to 3.6 V T_A = − 40 to 125 °C	-5.45	-	3.25	%
$t_{SU(HSI16)}^{(2)}$	HSI16 oscillator startup time	-	-	3.7	6	µs
$I_{DD(HSI16)}^{(2)}$	HSI16 oscillator power consumption	-	-	100	140	µA

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).
2. Guaranteed by characterization results.
3. Guaranteed by test in production.

Figure 25. HSI16 minimum and maximum value versus temperature



6.3.16 DAC electrical specifications

Data guaranteed by design, not tested in production, unless otherwise specified.

Table 67. DAC characteristics

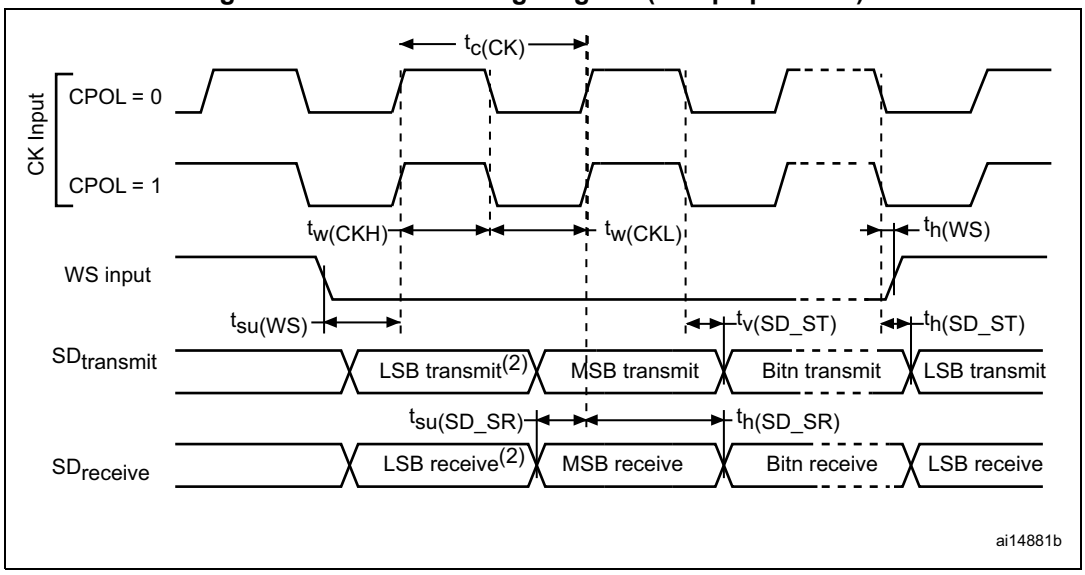
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{REF+}	Reference supply voltage	V_{REF+} must always be below V_{DDA}	1.8	-	3.6	V
V_{REF-}	Lower reference voltage	-	V_{SSA}			V
$I_{DDVREF+}$(1)	Current consumption on V_{REF+} supply V_{REF+} = 3.3 V	No load, middle code (0x800)	-	130	220	µA
		No load, worst code (0x000)	-	220	350	
I_{DDA} (2)	Current consumption on V_{DDA} supply, V_{DDA} = 3.3 V	No load, middle code (0x800)	-			µA
		No load, worst code (0xF1C)	-			
R_L(3)	Resistive load	DAC output buffer on	5	-	-	kΩ
C_L(3)	Capacitive load		-	-	50	pF
R_O	Output impedance	DAC output buffer off	12	16	20	kΩ
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON	0.2	-	V_{DDA} – 0.2	V
		DAC output buffer OFF	0.5	-	V_{REF+} – 1LSB	mV
DNL(2)	Differential non linearity(4)	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ DAC output buffer on	-	1.5	3	LSB
		No R_{LOAD}, $C_L \leq$ 50 pF DAC output buffer off	-	1.5	3	
INL(2)	Integral non linearity(5)	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ DAC output buffer on	-	2	4	
		No R_{LOAD}, $C_L \leq$ 50 pF DAC output buffer off	-	2	4	
Offset(2)	Offset error at code 0x800 (6)	$C_L \leq$ 50 pF, $R_L \geq$ 5 kΩ DAC output buffer on	-	±10	±25	
		No R_{LOAD}, $C_L \leq$ 50 pF DAC output buffer off	-	±5	±8	
Offset1(2)	Offset error at code 0x001(7)	No R_{LOAD}, $C_L \leq$ 50 pF DAC output buffer off	-	±1.5	±5	

Table 76. SPI characteristics in voltage Range 2 (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	8	MHz
		Slave mode Transmitter $1.65<V_{DD}<3.6V$			8	
		Slave mode Transmitter $2.7<V_{DD}<3.6V$			8(2)	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	0	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	11	-	-	
$t_{h(SI)}$		Slave mode	4.5	-	-	
$t_{a(SO}$	Data output access time	Slave mode	18	-	52	
$t_{dis(SO)}$	Data output disable time	Slave mode	12	-	42	
$t_{v(SO)}$	Data output valid time	Slave mode	-	20	56.5	
$t_{v(MO)}$		Master mode	-	5	9	
$t_{h(SO)}$	Data output hold time	Slave mode	13	-	-	
$t_{h(MO)}$		Master mode	3	-	-	

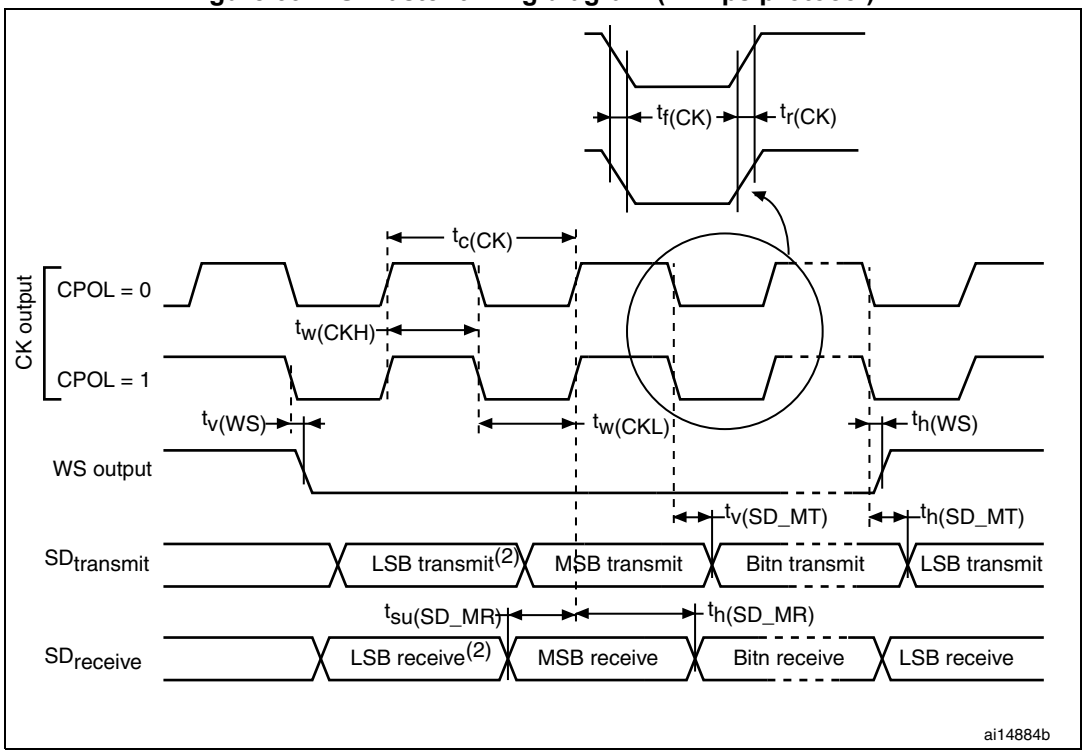
1. Guaranteed by characterization results.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

Figure 38. I²S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 39. I²S master timing diagram (Philips protocol)(1)



1. Guaranteed by characterization results.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

8 Part numbering

Table 96. STM32L072xx ordering information scheme

Example: STM32 L 072 R 8 T 6 D TR

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

L = Low power

Device subfamily

072 = USB

Pin count

K = 32 pins

C = 48/49 pins

R = 64 pins

V = 100 pins

Flash memory size

8 = 64 Kbytes

B = 128 Kbytes

Z = 192 Kbytes

Package

T = LQFP

H = TFBGA

I = UFBGA

U = UFQFPN

Y = WLCSP pins

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

3 = Industrial temperature range, –40 to 125 °C

Options

No character = V_{DD} range: 1.8 to 3.6 V and BOR enabled

D = V_{DD} range: 1.65 to 3.6 V and BOR disabled

Packing

TR = tape and reel

No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

9 Revision history

Table 97. Document revision history

Date	Revision	Changes
02-Sep-2015	1	Initial release
26-Oct-2015	2	Changed confidentiality level to public. Updated datasheet status to “production data”. Modified ultra-low-power platform features on cover page. Added note related to UFQFPN32 in *Table 16: STM32L072xxx pin definition*. In *Section 6: Electrical characteristics*, updated notes related to values guaranteed by characterization. Updated $\lvert\Delta V_{SS}\rvert$ definition to include V_{REF-} in *Table 23: Voltage characteristics*. Updated f_{TRIG} and V_{AIN} maximum value, added V_{REF+} and V_{REF-} in *Table 64: ADC characteristics*. Updated *Figure 43: UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline* and *Table 83: UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data*. Added *Section : Device marking for LQFP64*. Add “U” package type in *Section 8: Part numbering*