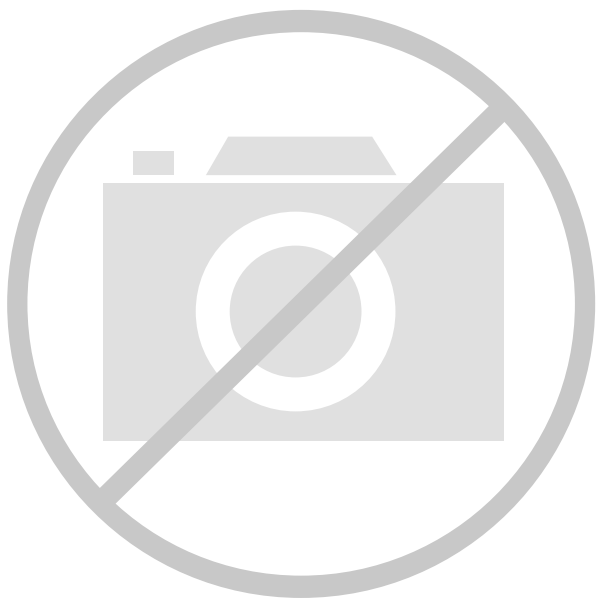




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	51
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	6K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA
Supplier Device Package	64-UFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l072rzi6tr

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Figure 1. STM32L072xx block diagram

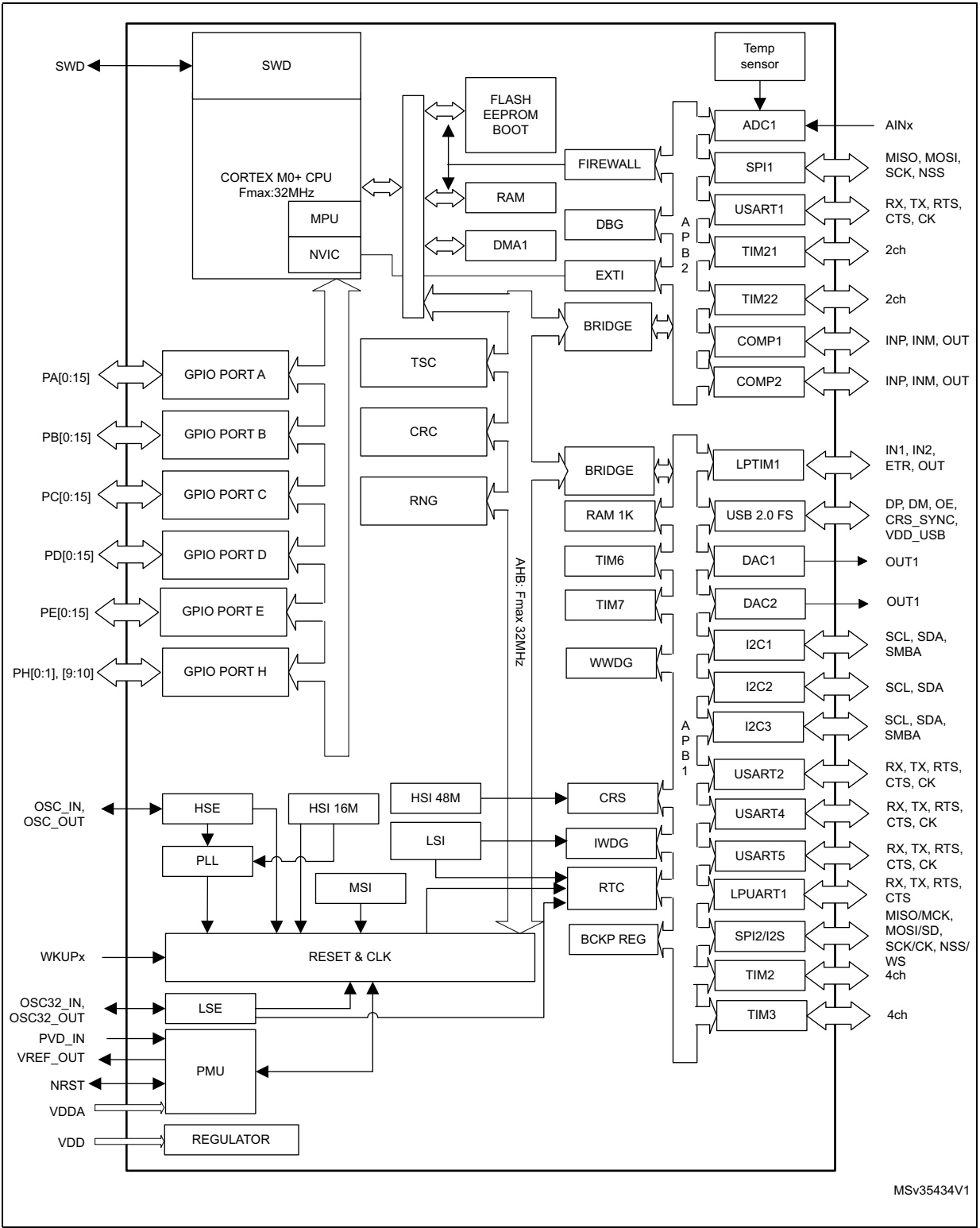


Table 9. Capacitive sensing GPIOs available on STM32L072xx devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	5	TSC_G5_IO1	PB3
	TSC_G1_IO2	PA1		TSC_G5_IO2	PB4
	TSC_G1_IO3	PA2		TSC_G5_IO3	PB6
	TSC_G1_IO4	PA3		TSC_G5_IO4	PB7
2	TSC_G2_IO1	PA4	6	TSC_G6_IO1	PB11
	TSC_G2_IO2	PA5		TSC_G6_IO2	PB12
	TSC_G2_IO3	PA6		TSC_G6_IO3	PB13
	TSC_G2_IO4	PA7		TSC_G6_IO4	PB14
3	TSC_G3_IO1	PC5	7	TSC_G7_IO1	PC0
	TSC_G3_IO2	PB0		TSC_G7_IO2	PC1
	TSC_G3_IO3	PB1		TSC_G7_IO3	PC2
	TSC_G3_IO4	PB2		TSC_G7_IO4	PC3
4	TSC_G4_IO1	PA9	8	TSC_G8_IO1	PC6
	TSC_G4_IO2	PA10		TSC_G8_IO2	PC7
	TSC_G4_IO3	PA11		TSC_G8_IO3	PC8
	TSC_G4_IO4	PA12		TSC_G8_IO4	PC9

3.16 Timers and watchdogs

The ultra-low-power STM32L072xx devices include three general-purpose timers, one low-power timer (LPTIM), one basic timer, two watchdog timers and the SysTick timer.

[Table 10](#) compares the features of the general-purpose and basic timers.

Table 10. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM21, TIM22	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Table 15. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 16. STM32L072xxx pin definition

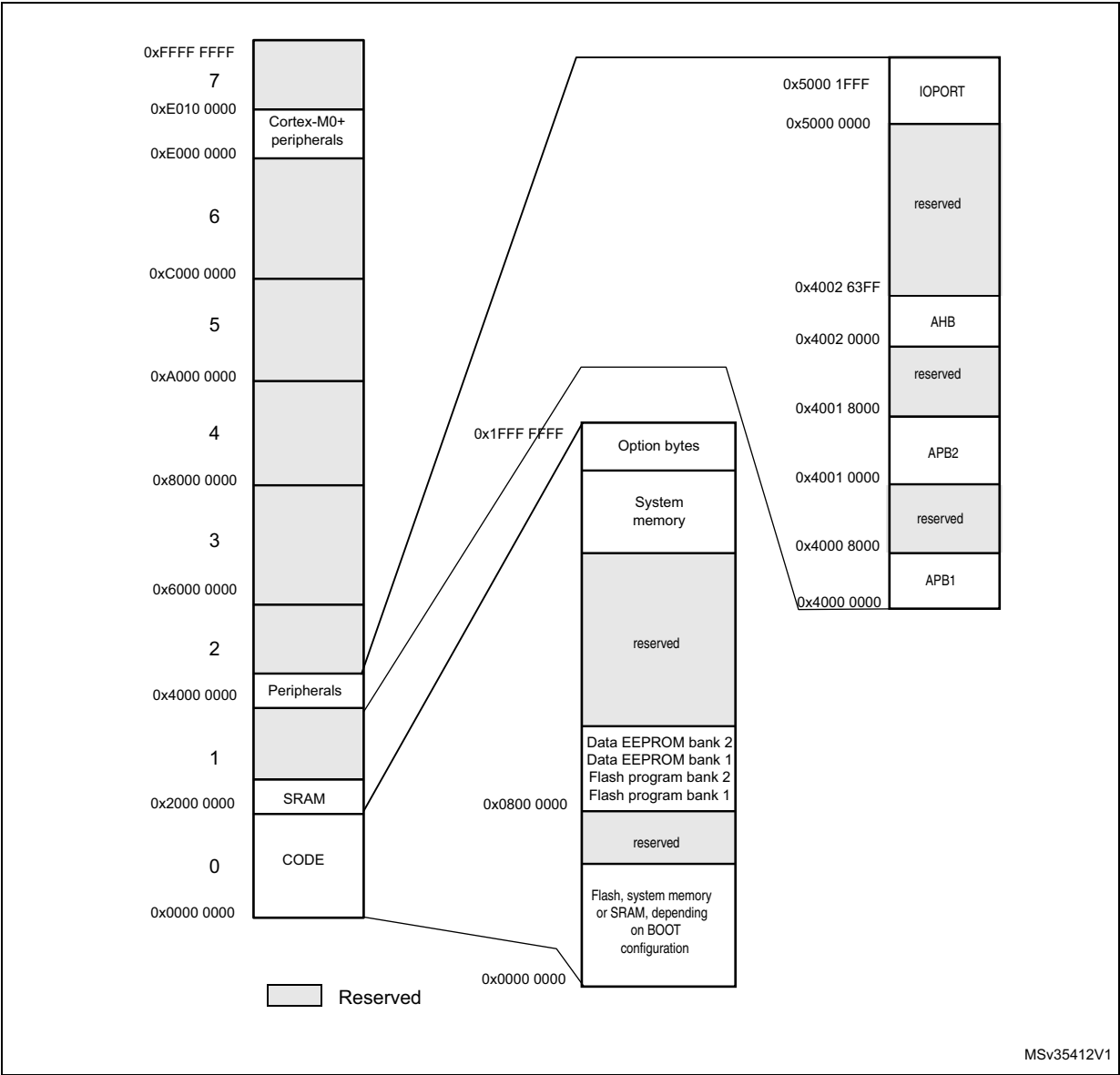
Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32 ⁽¹⁾	LQFP48	LQFP64	UFBGA64/TFBGA64	WLCSP49	LQFP100	UFBG100						
-	-	-	-	-	-	1	B2	PE2	I/O	FT	-	TIM3_ETR	-
-	-	-	-	-	-	2	A1	PE3	I/O	FT	-	TIM22_CH1, TIM3_CH1	-
-	-	-	-	-	-	3	B1	PE4	I/O	FT	-	TIM22_CH2, TIM3_CH2	-
-	-	-	-	-	-	4	C2	PE5	I/O	FT	-	TIM21_CH1, TIM3_CH3	-
-	-	-	-	-	-	5	D2	PE6	I/O	FT	-	TIM21_CH2, TIM3_CH4	RTC_TAMP3/WKUP3
1	-	1	1	B2	B6	6	E2	VDD	S		-	-	-

Table 22. Alternate functions port H

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/SPI2/ I2S2/USART1/2/ LPUART1/USB/ LPTIM1/TSC/ TIM2/21/22/ EVENTOUT/ SYS_AF	SPI1/SPI2/I2S2 /I2C1/TIM2/21	SPI1/SPI2/I2S2/ LPUART1/ USART5/USB/ LPTIM1/TIM2/3/ EVENTOUT/ SYS_AF	I2C1/TSC/ EVENTOUT	I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT	SPI2/I2S2/I2C2/ USART1/ TIM2/21/22	I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/ EVENTOUT	I2C3/ LPUART1/ COMP1/2/ TIM3
Port H	PH0	USB_CRD_SYNC	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-
	PH9	-	-	-	-	-	-	-	-
	PH10	-	-	-	-	-	-	-	-

5 Memory mapping

Figure 11. Memory map



1. Refer to the STM32L072xx reference manual for details on the Flash memory organization for each memory size.

Table 30. Current consumption in Run mode, code with data processing running from Flash memory

Symbol	Parameter	Condition		f _{HCLK} (MHz)	Typ	Max ⁽¹⁾	Unit
I _{DD} (Run from Flash memory)	Supply current in Run mode code executed from Flash memory	f _{HSE} = f _{HCLK} up to 16MHz included, f _{HSE} = f _{HCLK} /2 above 16 MHz (PLL ON) ⁽²⁾	Range3, V _{core} =1.2 V VOS[1:0]=11	1	190	250	μA
				2	345	380	
				4	650	670	
			Range2, V _{core} =1.5 V VOS[1:0]=10	4	0,8	0,86	mA
				8	1,55	1,7	
				16	2,95	3,1	
			Range1, V _{core} =1.8 V VOS[1:0]=01	8	1,9	2,1	
				16	3,55	3,8	
				32	6,65	7,2	
		MSI clock source	Range3, V _{core} =1.2 V VOS[1:0]=11	0,065	39	130	μA
				0,524	115	210	
				4,2	700	770	
		HSI clock source (16MHz)	Range2, V _{core} =1.5 V VOS[1:0]=10	16	2,9	3,2	mA
			Range1, V _{core} =1.8 V VOS[1:0]=01	32	7,15	7,4	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 31. Current consumption in Run mode vs code type, code with data processing running from Flash memory

Symbol	Parameter	Conditions			f _{HCLK}	Typ	Unit
I _{DD} (Run from Flash memory)	Supply current in Run mode, code executed from Flash memory	f _{HSE} = f _{HCLK} up to 16 MHz included, f _{HSE} = f _{HCLK} /2 above 16 MHz (PLL on) ⁽¹⁾	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	Dhrystone	4 MHz	650	μA
				CoreMark		655	
				Fibonacci		485	
				while(1)		385	
				while(1), 1WS, prefetch off		375	
			Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	Dhrystone	32 MHz	6,65	mA
				CoreMark		6,9	
				Fibonacci		6,75	
				while(1)		5,8	
				while(1), prefetch off		5,5	

1. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Figure 18. I_{DD} vs V_{DD} , at $T_A = 25^\circ\text{C}$, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS

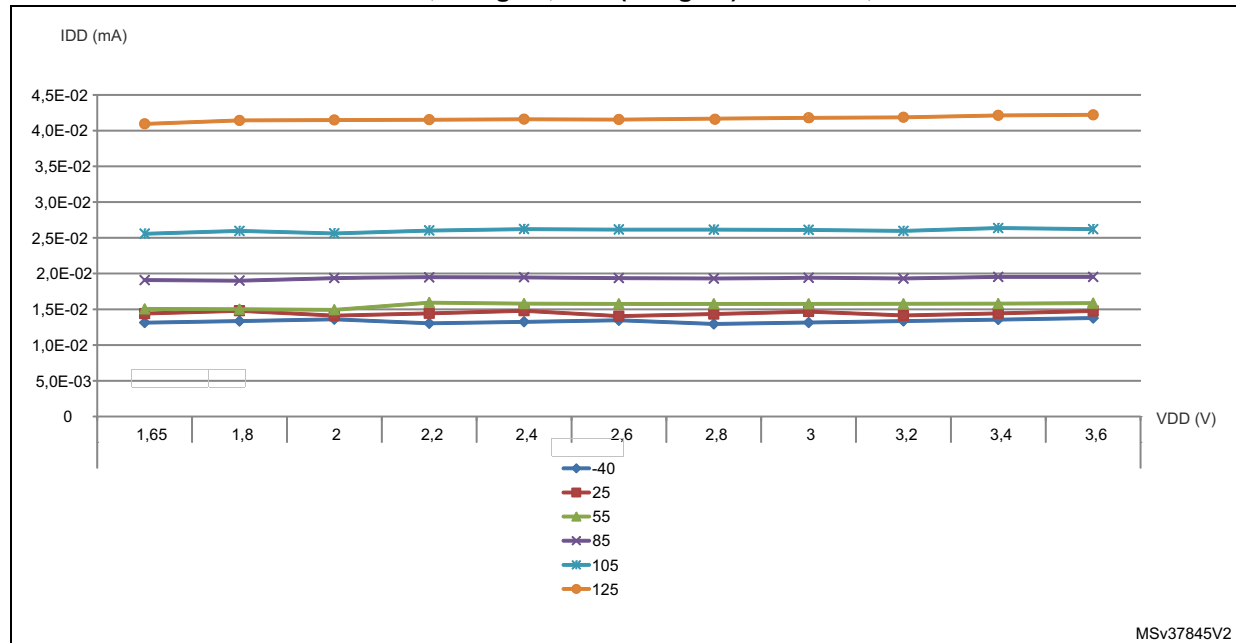


Table 36. Current consumption in Low-power sleep mode

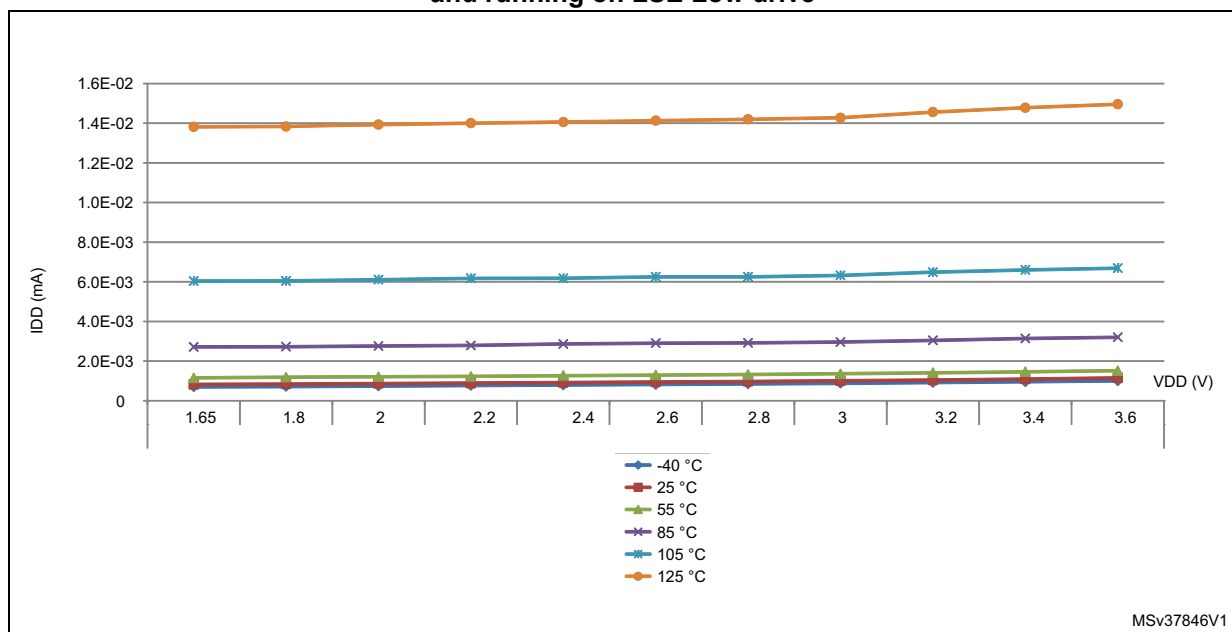
Symbol	Parameter	Condition			Typ	Max (1)	Unit
I_{DD} (LP Sleep)	Supply current in Low-power sleep mode	All peripherals OFF, code executed from Flash memory, V_{DD} from 1.65 to 3.6 V	MSI clock = 65 kHz, $f_{HCLK} = 32$ kHz, Flash memory OFF	$T_A = -40$ to 25°C	4,7	-	μA
			MSI clock = 65 kHz, $f_{HCLK} = 32$ kHz	$T_A = -40$ to 25°C	17	24	
				$T_A = 85^\circ\text{C}$	19,5	30	
				$T_A = 105^\circ\text{C}$	23	47	
				$T_A = 125^\circ\text{C}$	32,5	70	
			MSI clock = 65 kHz, $f_{HCLK} = 65$ kHz	$T_A = -40$ to 25°C	17	24	
				$T_A = 85^\circ\text{C}$	20	31	
				$T_A = 105^\circ\text{C}$	23,5	47	
				$T_A = 125^\circ\text{C}$	32,5	70	
			MSI clock = 131kHz, $f_{HCLK} = 131$ kHz	$T_A = -40$ to 25°C	19,5	27	
				$T_A = 55^\circ\text{C}$	20,5	28	
				$T_A = 85^\circ\text{C}$	22,5	33	
				$T_A = 105^\circ\text{C}$	26	50	
				$T_A = 125^\circ\text{C}$	35	73	

1. Guaranteed by characterization results at 125°C , unless otherwise specified.

Table 37. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max ⁽¹⁾	Unit
I_{DD} (Stop)	Supply current in Stop mode	$T_A = -40$ to 25°C	0,43	1,00	μA
		$T_A = 55^\circ\text{C}$	0,735	2,50	
		$T_A = 85^\circ\text{C}$	2,25	4,90	
		$T_A = 105^\circ\text{C}$	5,3	13,00	
		$T_A = 125^\circ\text{C}$	12,5	28,00	

1. Guaranteed by characterization results at 125°C , unless otherwise specified.

Figure 19. I_{DD} vs V_{DD} , at $T_A = 25/55/ 85/105/125^\circ\text{C}$, Stop mode with RTC enabled and running on LSE Low drive

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in [Section 6.3.12](#). However, the recommended clock input waveform is shown in [Figure 21](#).

Table 43. High-speed external user clock characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is on or PLL is used	1	8	32	MHz
		CSS is off, PLL not used	0	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time		12	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance		-	2.6	-	pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 1	μA

1. Guaranteed by design.

Figure 21. High-speed external clock source AC timing diagram

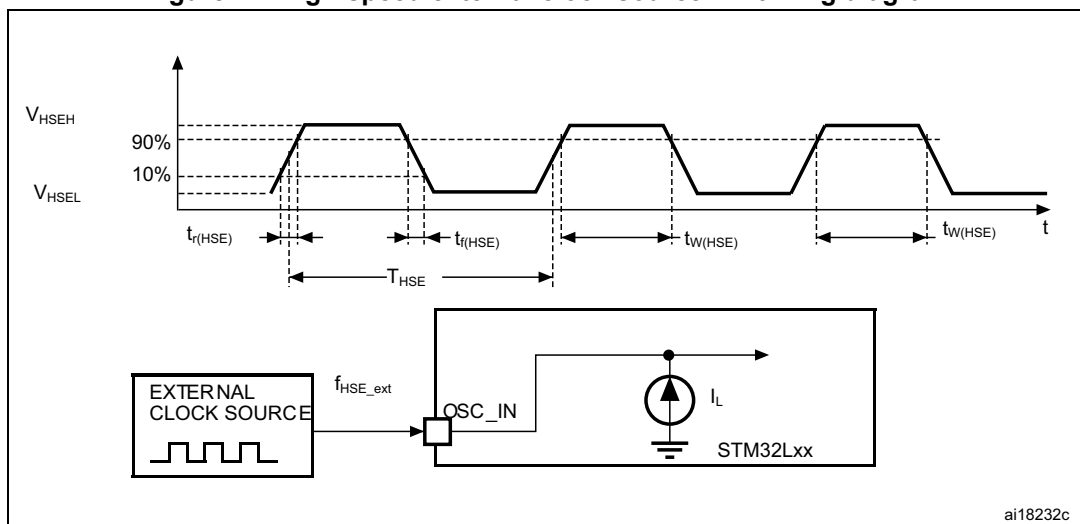


Table 54. Flash memory and data EEPROM endurance and retention (continued)

Symbol	Parameter	Conditions	Value	Unit
			Min ⁽¹⁾	
t _{RET} ⁽²⁾	Data retention (program memory) after 10 kcycles at T _A = 85 °C	T _{RET} = +85 °C	30	years
	Data retention (EEPROM data memory) after 100 kcycles at T _A = 85 °C		30	
	Data retention (program memory) after 10 kcycles at T _A = 105 °C	T _{RET} = +105 °C	10	
	Data retention (EEPROM data memory) after 100 kcycles at T _A = 105 °C			
	Data retention (program memory) after 200 cycles at T _A = 125 °C	T _{RET} = +125 °C		
	Data retention (EEPROM data memory) after 2 kcycles at T _A = 125 °C			

1. Guaranteed by characterization results.

2. Characterization is done according to JEDEC JESD22-A117.

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 55](#). They are based on the EMS levels and classes defined in application note AN1709.

Table 55. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{\text{DD}} = 3.3\text{ V}$, LQFP100, $T_A = +25\text{ }^{\circ}\text{C}$, $f_{\text{HCLK}} = 32\text{ MHz}$ conforms to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{\text{DD}} = 3.3\text{ V}$, LQFP100, $T_A = +25\text{ }^{\circ}\text{C}$, $f_{\text{HCLK}} = 32\text{ MHz}$ conforms to IEC 61000-4-4	4A

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of $-5\ \mu\text{A}/+0\ \mu\text{A}$ range), or other functional failure (for example reset occurrence oscillator frequency deviation).

The test results are given in the [Table 59](#).

Table 59. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	-0	NA	mA
	Injected current on PA0, PA4, PA5, PC15, PH0 and PH1	-5	0	
	Injected current on any other FT, FTf pins	-5 ⁽¹⁾	NA	
	Injected current on any other pins	-5 ⁽¹⁾	+5	

1. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

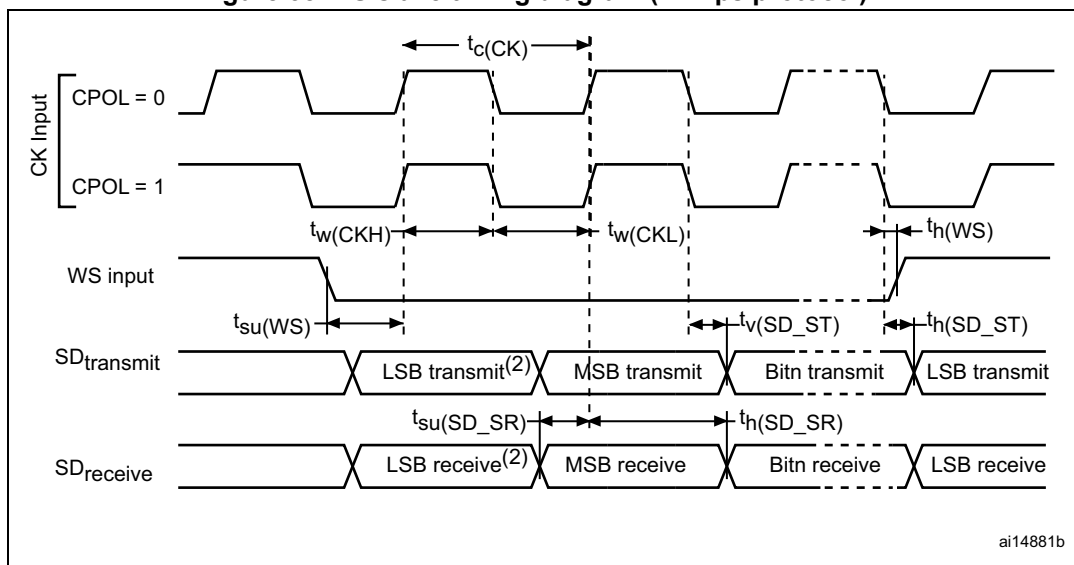
Output voltage levels

Unless otherwise specified, the parameters given in [Table 61](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 26](#). All I/Os are CMOS and TTL compliant.

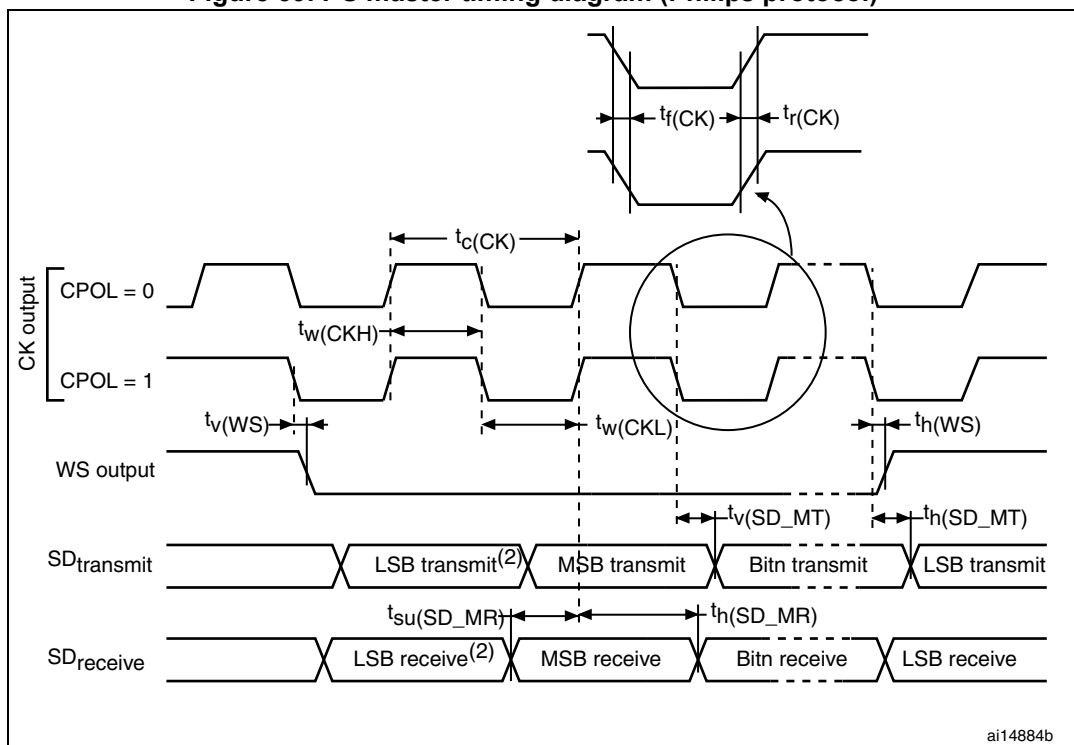
Table 61. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	CMOS port ⁽²⁾ , $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD}-0.4$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	TTL port ⁽²⁾ , $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin	TTL port ⁽²⁾ , $I_{IO} = -6 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	2.4	-	
$V_{OL}^{(1)(4)}$	Output low level voltage for an I/O pin	$I_{IO} = +15 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	1.3	
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin	$I_{IO} = -15 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$V_{DD}-1.3$	-	
$V_{OL}^{(1)(4)}$	Output low level voltage for an I/O pin	$I_{IO} = +4 \text{ mA}$ $1.65 \text{ V} \leq V_{DD} < 3.6 \text{ V}$	-	0.45	
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin	$I_{IO} = -4 \text{ mA}$ $1.65 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$V_{DD}-0.45$	-	
$V_{OLFM+}^{(1)(4)}$	Output low level voltage for an FTf I/O pin in Fm+ mode	$I_{IO} = 20 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	
		$I_{IO} = 10 \text{ mA}$ $1.65 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 24](#). The sum of the currents sunk by all the I/Os (I/O ports and control pins) must always be respected and must not exceed $\Sigma I_{IO(PIN)}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 24](#). The sum of the currents sourced by all the I/Os (I/O ports and control pins) must always be respected and must not exceed $\Sigma I_{IO(PIN)}$.
4. Guaranteed by characterization results.

Figure 38. I²S slave timing diagram (Philips protocol)⁽¹⁾

1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

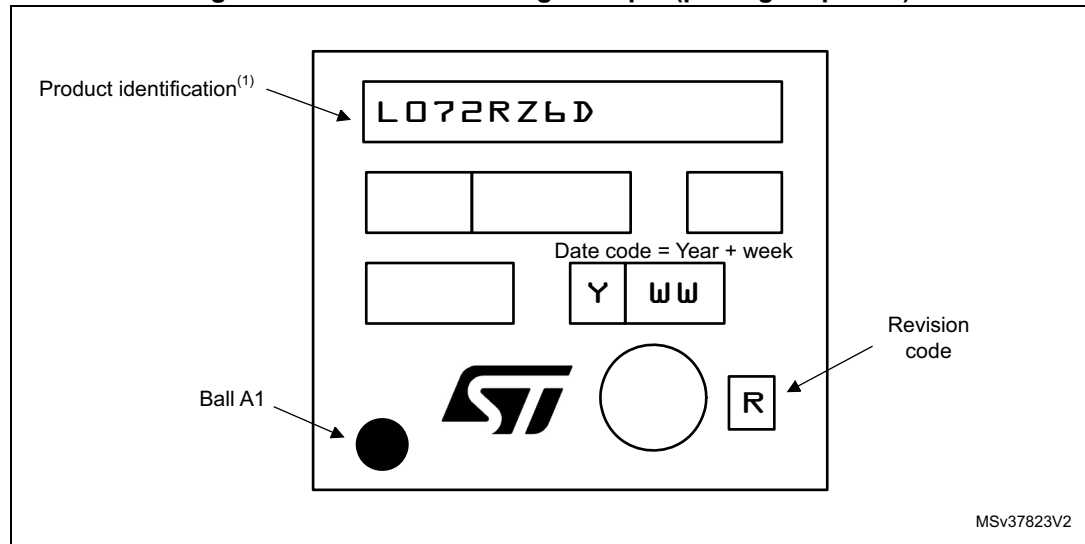
Figure 39. I²S master timing diagram (Philips protocol)⁽¹⁾

1. Guaranteed by characterization results.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Device marking for TFBGA64

The following figure gives an example of topside marking versus ball A 1 position identifier location.

Figure 53. TFBGA64 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

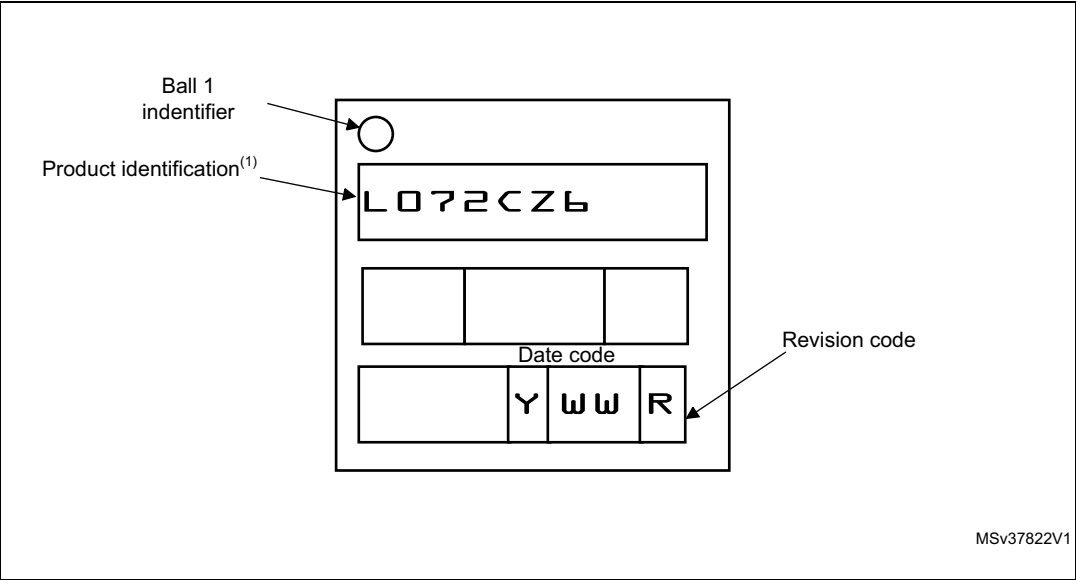
Table 91. WLCSP49 recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4
Dpad	260 µm max. (circular) 220 µm recommended
Dsm	300 µm min. (for 260 µm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed.

Device marking for WLCSP49

The following figure gives an example of topside marking versus ball A 1 position identifier location.

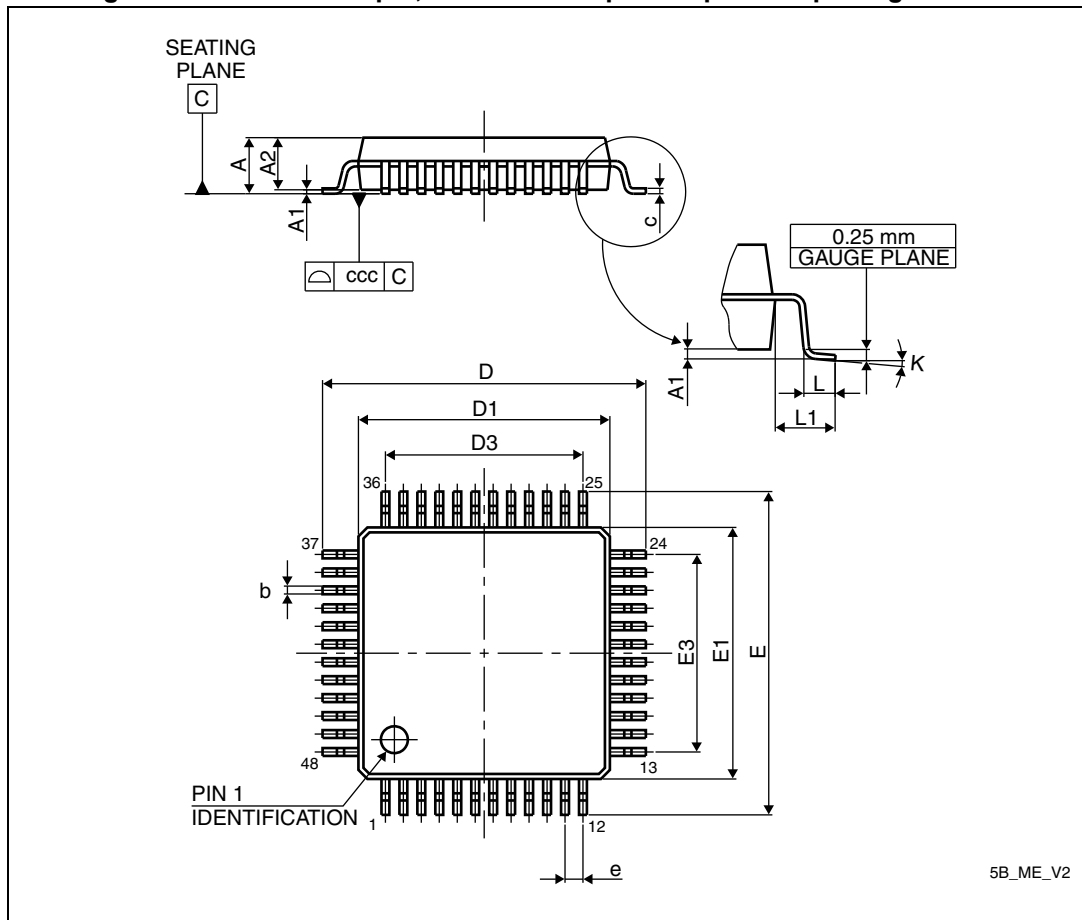
Figure 56. WLCSP49 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.7 LQFP48 package information

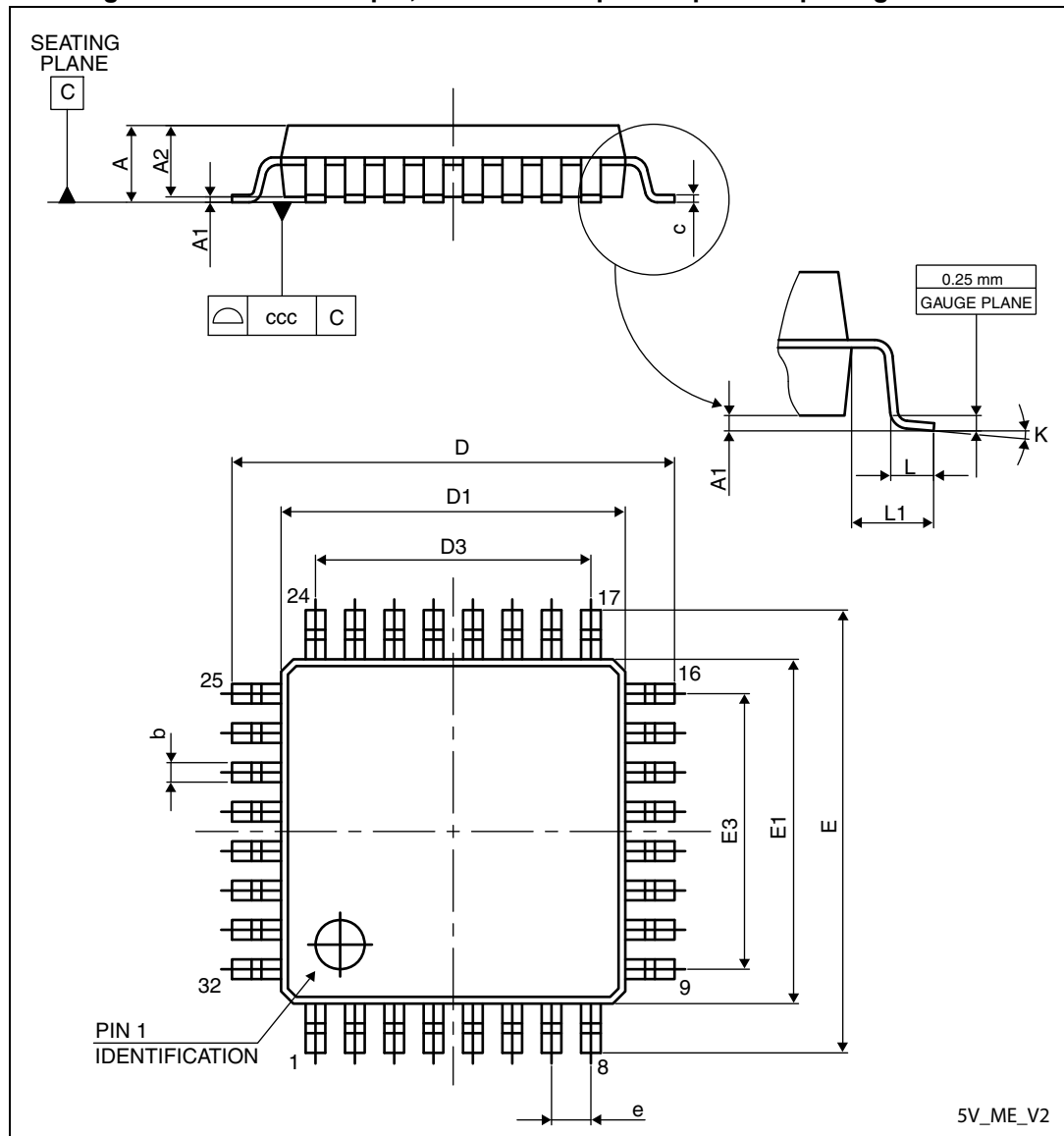
Figure 57. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

7.8 LQFP32 package information

Figure 59. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.