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What is "Embedded - Microcontrollers"?

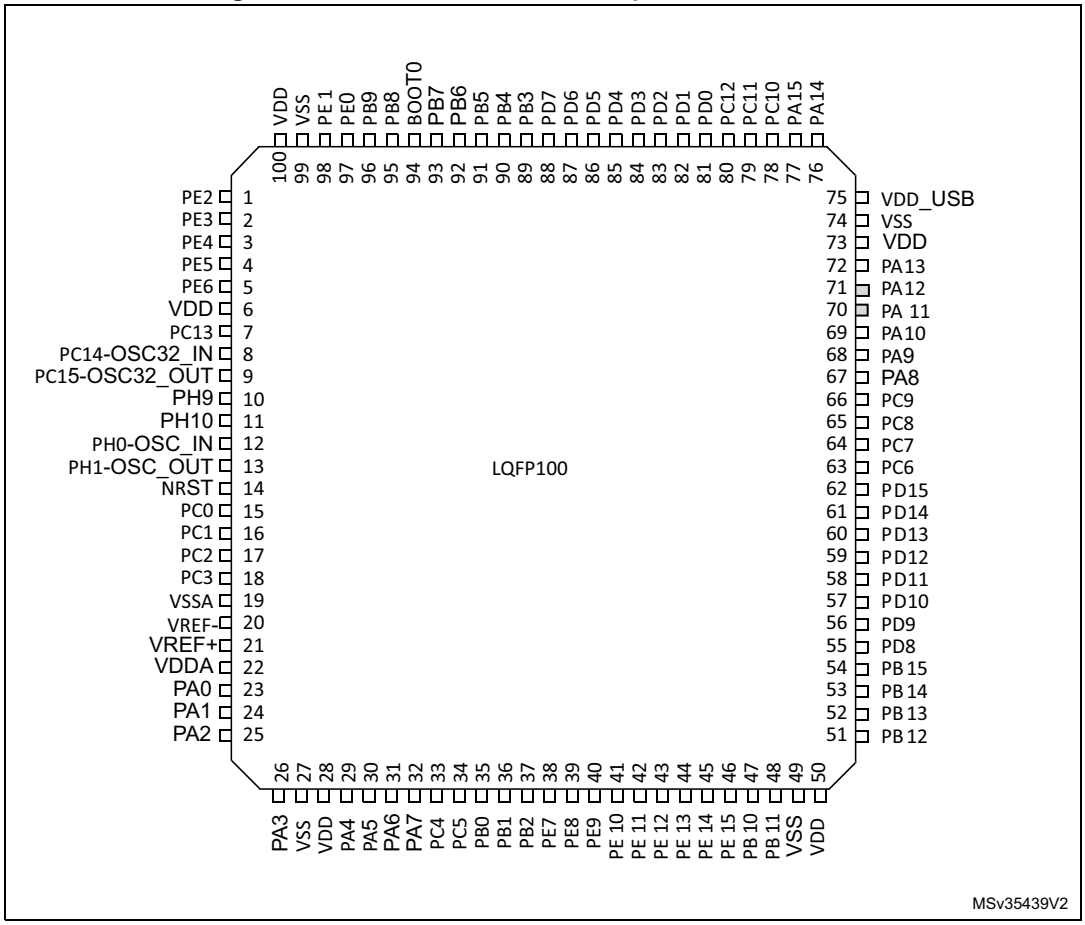
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	84
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	3K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l072v8t6

4 Pin descriptions

Figure 3. STM32L072xx LQFP100 pinout - 14 x 14 mm



1. The above figure shows the package top view.
2. I/O pin supplied by VDD_USB.

Table 15. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 16. STM32L072xxx pin definition

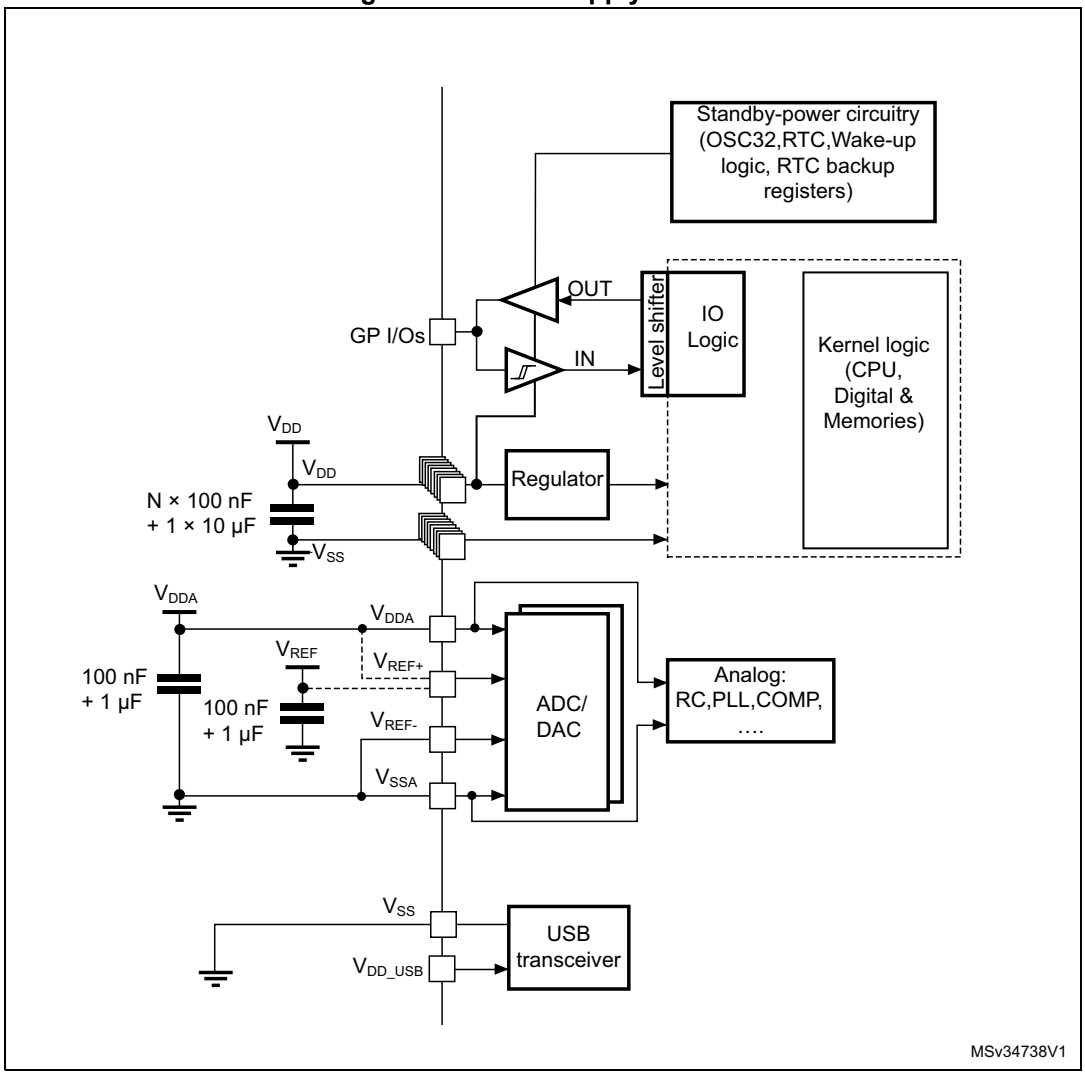
Pin number								Pin name (function after reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
LQFP32	UFQFPN32(1)	LQFP48	LQFP64	UFBGA64/TFBGA64	WLCSP49	LQFP100	UFBG100						
-	-	-	-	-	-	1	B2	PE2	I/O	FT	-	TIM3_ETR	-
-	-	-	-	-	-	2	A1	PE3	I/O	FT	-	TIM22_CH1, TIM3_CH1	-
-	-	-	-	-	-	3	B1	PE4	I/O	FT	-	TIM22_CH2, TIM3_CH2	-
-	-	-	-	-	-	4	C2	PE5	I/O	FT	-	TIM21_CH1, TIM3_CH3	-
-	-	-	-	-	-	5	D2	PE6	I/O	FT	-	TIM21_CH2, TIM3_CH4	RTC_TAMP3/WKUP3
1	-	1	1	B2	B6	6	E2	VDD	S		-	-	-

Table 21. Alternate functions port E

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/SPI2/I2S2/ USART1/2/ LPUART1/USB/ LPTIM1/TSC/ TIM2/21/22/ EVENTOUT/ SYS_AF	SPI1/SPI2/I2S2/I2C1 /TIM2/21	SPI1/SPI2/I2S2/ LPUART1/ USART5/USB/ LPTIM1/TIM2/3 /EVENTOUT/ SYS_AF	I2C1/TSC/ EVENTOUT	I2C1/USART1/2/ LPUART1/ TIM3/22/ EVENTOUT	SPI2/I2S2 /I2C2/ USART1/ TIM2/21/22	I2C1/2/ LPUART1/ USART4/ UASRT5/TIM21/ EVENTOUT	I2C3/LPUART1/ COMP1/2/TIM3
Port E	PE0	-		EVENTOUT	-	-	-	-	-
	PE1	-		EVENTOUT	-	-	-	-	-
	PE2	-		TIM3_ETR	-	-	-	-	-
	PE3	TIM22_CH1		TIM3_CH1	-	-	-	-	-
	PE4	TIM22_CH2	-	TIM3_CH2	-	-	-	-	-
	PE5	TIM21_CH1	-	TIM3_CH3	-	-	-	-	-
	PE6	TIM21_CH2	-	TIM3_CH4	-	-	-	-	-
	PE7	-		-	-	-	-	USART5_CK/U SART5_RTS_D E	-
	PE8	-		-	-	-	-	USART4_TX	-
	PE9	TIM2_CH1		TIM2_ETR	-	-	-	USART4_RX	-
	PE10	TIM2_CH2		-	-	-	-	USART5_TX	-
	PE11	TIM2_CH3	-	-	-	-	-	USART5_RX	-
	PE12	TIM2_CH4	-	SPI1_NSS	-	-	-	-	-
	PE13	-		SPI1_SCK	-	-	-	-	-
	PE14	-		SPI1_MISO	-	-	-	-	-
	PE15	-		SPI1_MOSI	-	-	-	-	-

6.1.6 Power supply scheme

Figure 14. Power supply scheme



6.1.7 Current consumption measurement

Figure 15. Current consumption measurement scheme

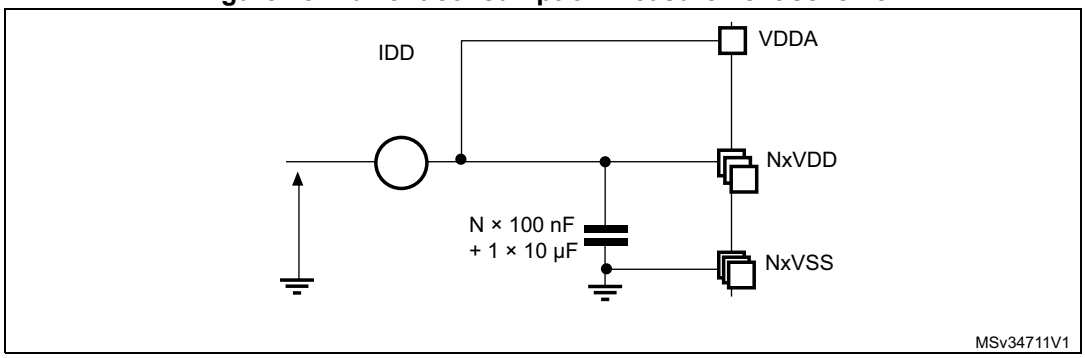


Table 27. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09	V
		Rising edge	3.08	3.15	3.20	
V_{hyst}	Hysteresis voltage	BOR0 threshold	-	40	-	mV
		All BOR and PVD thresholds excepting BOR0	-	100	-	

1. Guaranteed by characterization results.
2. Valid for device version without BOR at power up. Please see option "D" in Ordering information scheme for more details.

6.3.3 Embedded internal reference voltage

The parameters given in *Table 29* are based on characterization results, unless otherwise specified.

Table 28. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25 °C V_{DDA}= 3 V	0x1FF8 0078 - 0x1FF8 0079

Table 29. Embedded internal reference voltage(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT\ out}$(2)	Internal reference voltage	– 40 °C < T_J < +125 °C	1.202	1.224	1.242	V
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} and V_{REF+} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REFINT} value(3)	Including uncertainties due to ADC and V_{DDA}/V_{REF+} values	-	-	±5	mV
T_{Coeff}(4)	Temperature coefficient	–40 °C < T_J < +125 °C	-	25	100	ppm/°C
A_{Coeff}(4)	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
$V_{DDCoeff}$(4)	Voltage coefficient	3.0 V < V_{DDA} < 3.6 V	-	-	2000	ppm/V
$T_{S\_vrefint}$(4)(5)	ADC sampling time when reading the internal reference voltage	-	5	10	-	µs
T_{ADC_BUF}(4)	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
I_{BUF_ADC}(4)	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
I_{VREF_OUT}(4)	VREF_OUT output current(6)	-	-	-	1	µA
C_{VREF_OUT}(4)	VREF_OUT output load	-	-	-	50	pF

Table 34. Current consumption in Sleep mode

Symbol	Parameter	Condition		f_{HCLK} (MHz)	Typ	Max(1)	Unit
I_{DD} (Sleep)	Supply current in Sleep mode, Flash memory switched OFF	$f_{HSE} = f_{HCLK}$ up to 16 MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range3, Vcore=1.2 V VOS[1:0]=11	1	43,5	110	µA
				2	72	140	
				4	130	200	
			Range2, Vcore=1.5 V VOS[1:0]=10	4	160	220	
				8	305	380	
				16	590	690	
			Range1, Vcore=1.8 V VOS[1:0]=01	8	370	460	
				16	715	840	
				32	1650	2000	
		MSI clock	Range3, Vcore=1.2 V VOS[1:0]=11	0,065	18	93	
				0,524	31,5	110	
				4,2	140	230	
		HSI clock source (16 MHz)	Range2, Vcore=1.5 V VOS[1:0]=10	16	665	850	
			Range1, Vcore=1.8 V VOS[1:0]=01	32	1750	2100	
	Supply current in Sleep mode, Flash memory switched ON	$f_{HSE} = f_{HCLK}$ up to 16MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range3, Vcore=1.2 V VOS[1:0]=11	1	57,5	130	
				2	84	160	
				4	150	220	
			Range2, Vcore=1.5 V VOS[1:0]=10	4	170	240	
				8	315	400	
				16	605	710	
			Range1, Vcore=1.8 V VOS[1:0]=01	8	380	470	
				16	730	860	
				32	1650	2000	
		MSI clock	Range3, Vcore=1.2 V VOS[1:0]=11	0,065	29,5	110	
				0,524	44,5	120	
				4,2	150	240	
		HSI clock source (16MHz)	Range2, Vcore=1.5 V VOS[1:0]=10	16	680	930	
			Range1, Vcore=1.8 V VOS[1:0]=01	32	1750	2200	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 37. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
I_{DD} (Stop)	Supply current in Stop mode	T_A = − 40 to 25°C	0,43	1,00	µA
		T_A = 55°C	0,735	2,50	
		T_A= 85°C	2,25	4,90	
		T_A = 105°C	5,3	13,00	
		T_A = 125°C	12,5	28,00	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

Figure 19. I_{DD} vs V_{DD}, at T_A= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive

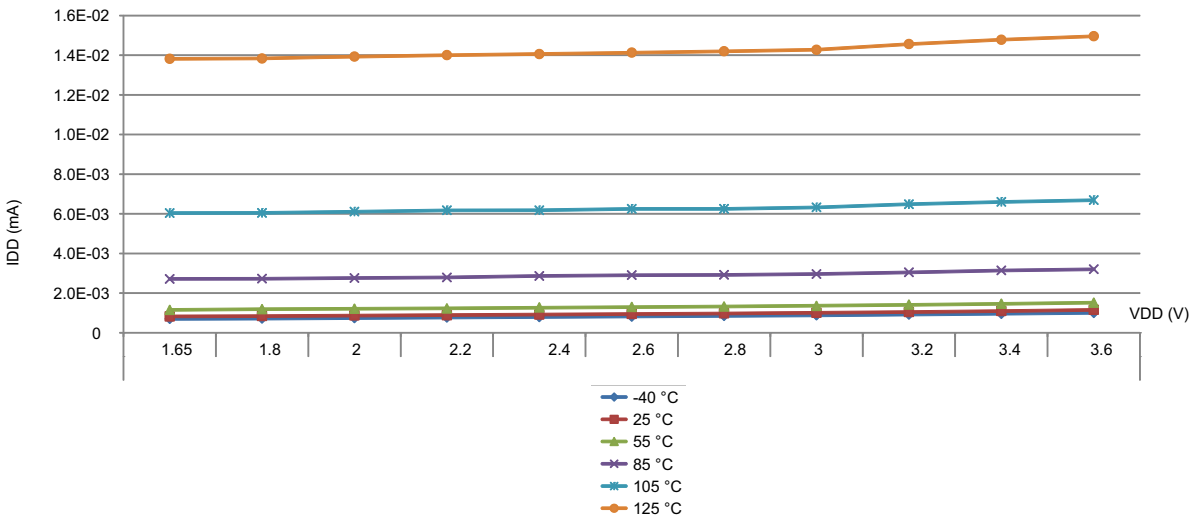


Table 39. Average current consumption during Wakeup

Symbol	parameter	System frequency	Current consumption during wakeup	Unit
I_{DD} (Wakeup from Stop)	Supply current during Wakeup from Stop mode	HSI	1	mA
		HSI/4	0,7	
		MSI clock = 4,2 MHz	0,7	
		MSI clock = 1,05 MHz	0,4	
		MSI clock = 65 KHz	0,1	
I_{DD} (Reset)	Reset pin pulled down	-	0,21	
I_{DD} (Power-up)	BOR on	-	0,23	
I_{DD} (Wakeup from StandBy)	With Fast wakeup set	MSI clock = 2,1 MHz	0,5	
	With Fast wakeup disabled	MSI clock = 2,1 MHz	0,12	

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following tables. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on

Table 40. Peripheral current consumption in Run or Sleep mode(1)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	Low-power sleep and run	
APB1	CRS	2.5	2	2	2	µA/MHz (f_{HCLK})
	DAC1/2	4	3.5	3	2.5	
	I2C1	11	9.5	7.5	9	
	I2C3	11	9	7	9	
	LPTIM1	10	8.5	6.5	8	
	LPUART1	8	6.5	5.5	6	
	SPI2	9	4.5	3.5	4	
	USB	8.5	4.5	4	4.5	
	USART2	14.5	12	9.5	11	
	USART4	5	4	3	5	
	USART5	5	4	3	5	
	TIM2	10.5	8.5	7	9	
	TIM3	12	10	8	11	
	TIM6	3.5	3	2.5	2	
	TIM7	3.5	3	2.5	2	
	WWDG	3	2	2	2	

High-speed internal 48 MHz (HSI48) RC oscillator

Table 48. HSI48 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	Frequency		-	48	-	MHz
TRIM	HSI48 user-trimming step		0.09(2)	0.14	0.2(2)	%
$DuCy_{(HSI48)}$	Duty cycle		45(2)	-	55(2)	%
ACC_{HSI48}	Accuracy of the HSI48 oscillator (factory calibrated before CRS calibration)	T_A = 25 °C	-4(3)	-	4(3)	%
$t_{su(HSI48)}$	HSI48 oscillator startup time		-	-	6(2)	µs
$I_{DDA(HSI48)}$	HSI48 oscillator power consumption		-	330	380(2)	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 125 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.

Low-speed internal (LSI) RC oscillator

Table 49. LSI oscillator characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(1)	LSI frequency	26	38	56	kHz
D_{LSI}(2)	LSI oscillator frequency drift $0°C \le T_A \le 85°C$	-10	-	4	%
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	200	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	400	510	nA

1. Guaranteed by test in production.
2. This is a deviation for an individual part, once the initial frequency has been measured.
3. Guaranteed by design.

Multi-speed internal (MSI) RC oscillator

Table 50. MSI oscillator characteristics

Symbol	Parameter	Condition	Typ	Max	Unit
f_{MSI}	Frequency after factory calibration, done at V_{DD}= 3.3 V and T_A = 25 °C	MSI range 0	65.5	-	kHz
		MSI range 1	131	-	
		MSI range 2	262	-	
		MSI range 3	524	-	
		MSI range 4	1.05	-	MHz
		MSI range 5	2.1	-	
		MSI range 6	4.2	-	

6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 57. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1.	C4	500	

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

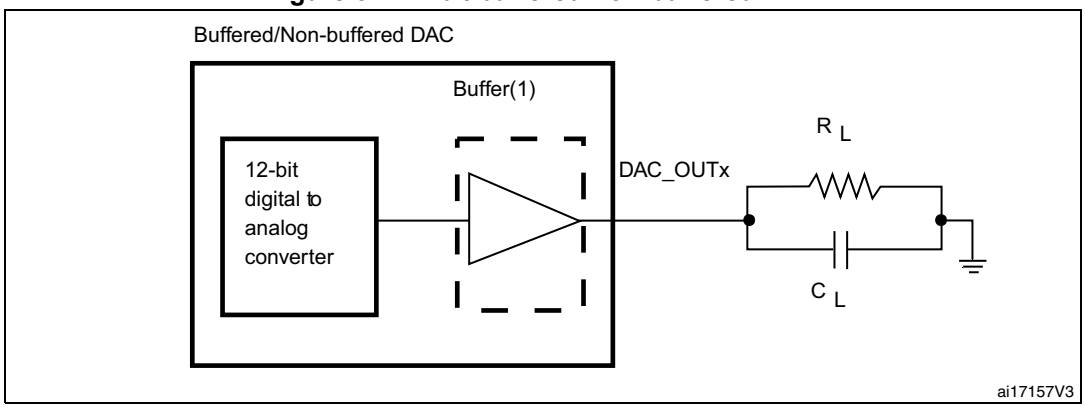
These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 58. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +125 °C conforming to JESD78A	II level A

6. Difference between the value measured at Code (0x800) and the ideal value = $V_{REF+}/2$.
7. Difference between the value measured at Code (0x001) and the ideal value.
8. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is off, and from code giving 0.2 V and (V_{DDA} – 0.2) V when buffer is on.
9. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

Figure 34. 12-bit buffered/non-buffered DAC



6.3.17 Temperature sensor characteristics

Table 68. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3 V	0x1FF8 007A - 0x1FF8 007B
TS_CAL2	TS ADC raw data acquired at temperature of 130 °C, V_{DDA}= 3 V	0x1FF8 007E - 0x1FF8 007F

Table 69. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	1.48	1.61	1.75	mV/°C
V_{130}	Voltage at 130°C ±5°C(2)	640	670	700	mV
$I_{DDA(TEMP)}$(3)	Current consumption	-	3.4	6	µA
t_{START}(3)	Startup time	-	-	10	µs
T_{S_temp}(4)(3)	ADC sampling time when reading the temperature	10	-	-	

1. Guaranteed by characterization results.
2. Measured at V_{DD} = 3 V ±10 mV. V130 ADC conversion result is stored in the TS_CAL2 byte.
3. Guaranteed by design.
4. Shortest sampling time can be determined in the application by multiple iterations.

6.3.19 Timer characteristics

TIM timer characteristics

The parameters given in the *Table 72* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 72. TIMx characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	31.25	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 32 MHz	0	16	MHz
Res_{TIM}	Timer resolution	-		16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected (timer's prescaler disabled)	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	0.0312	2048	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	-	134.2	s

1. TIMx is used as a general term to refer to the TIM2, TIM6, TIM21, and TIM22 timers.

6.3.20 Communications interfaces

I^2C interface characteristics

The I^2C interface meets the timings requirements of the I^2C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm) : with a bit rate up to 100 kbit/s
- Fast-mode (Fm) : with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+) : with a bit rate up to 1 Mbit/s.

The I^2C timing requirements are guaranteed by design when the I^2C peripheral is properly configured (refer to the reference manual for details). The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement (refer to *Section 6.3.13: I/O port characteristics* for the I2C I/Os characteristics).

All I^2C SDA and SCL I/Os embed an analog filter (see *Table 73* for the analog filter characteristics).

The analog spike filter is compliant with I^2C timings requirements only for the following voltage ranges:

- Fast mode Plus: 2.7 V ≤ V_{DD} ≤ 3.6 V and voltage scaling Range 1
- Fast mode:
  - 2 V ≤ V_{DD} ≤ 3.6 V and voltage scaling Range 1 or Range 2.
  - V_{DD} < 2 V, voltage scaling Range 1 or Range 2, C_{load} < 200 pF.

In other ranges, the analog filter should be disabled. The digital filter can be used instead.

Note: In Standard mode, no spike filter is required.

Table 73. I2C analog filter characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	Range 1	50(2)	100(3)	ns
		Range 2		-	
		Range 3		-	

1. Guaranteed by characterization results.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

USART/LPUART characteristics

The parameters given in the following table are guaranteed by design.

Table 74. USART/LPUART characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$	Wakeup time needed to calculate the maximum USART/LPUART baudrate allowing to wake up from Stop mode	Stop mode with main regulator in Run mode, Range 2 or 3	-	8.7	µs
		Stop mode with main regulator in Run mode, Range 1	-	8.1	
		Stop mode with main regulator in low-power mode, Range 2 or 3	-	12	
		Stop mode with main regulator in low-power mode, Range 1	-	11.4	

USB characteristics

The USB interface is USB-IF certified (full speed).

Table 79. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

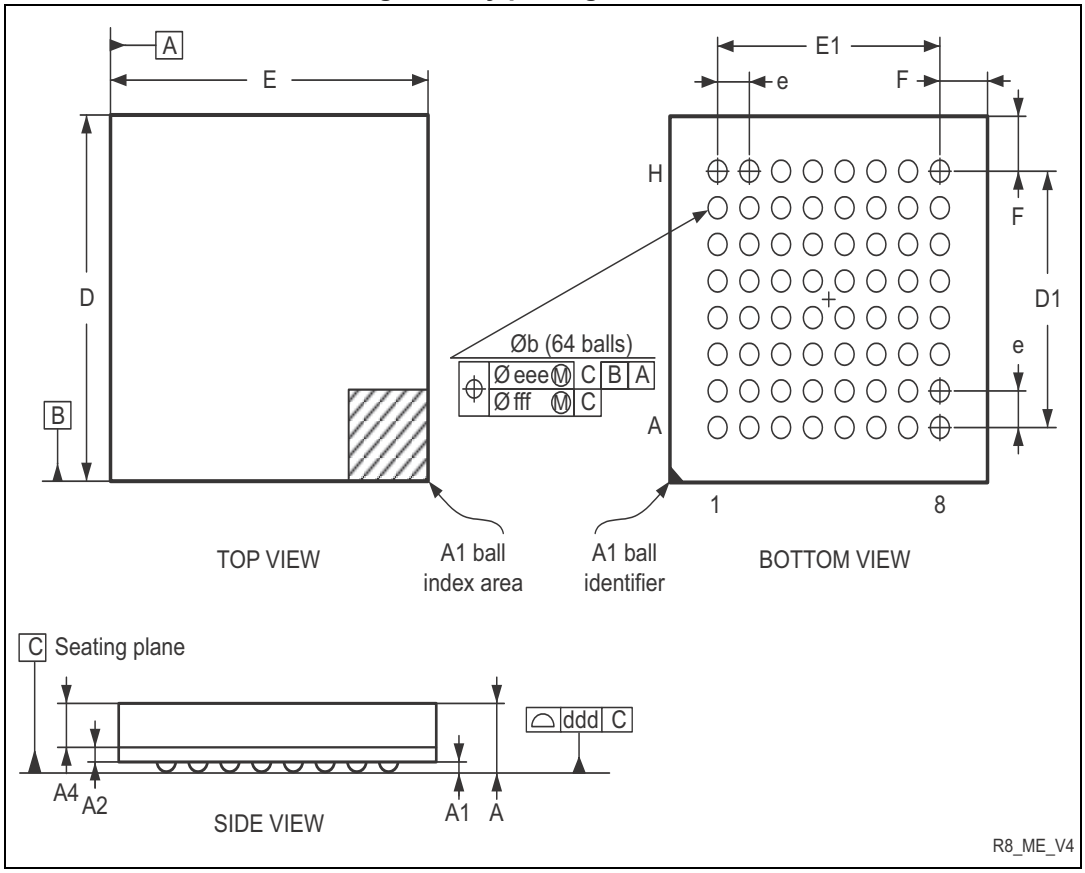
Table 80. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage	-	3.0	3.6	V
V_{DI}(2)	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(2)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(2)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}(3)	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	0.3	V
V_{OH}(3)	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. Guaranteed by characterization results.
3. Guaranteed by test in production.
4. R_L is the load connected on the USB drivers.

7.5 TFBGA64 package information

Figure 51. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch thin profile fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 88. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data

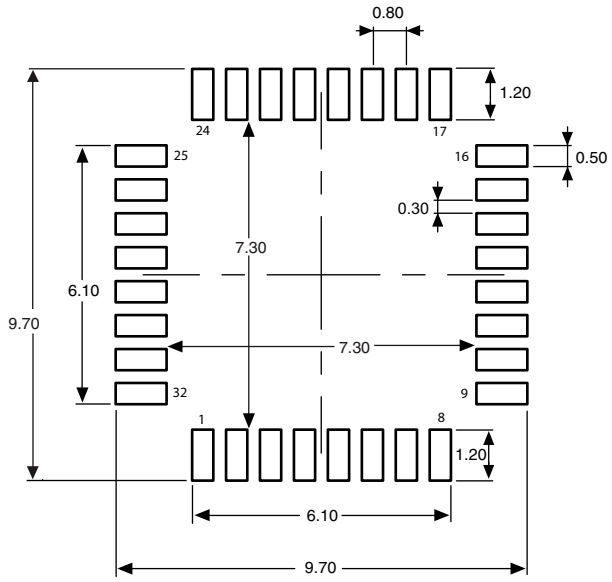
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.150	-	-	0.0059	-	-
A2	-	0.200	-	-	0.0079	-
A4	-	-	0.600	-	-	0.0236
b	0.250	0.300	0.350	0.0098	0.0118	0.0138
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	-	3.500	-	-	0.1378	-
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	-	3.500	-	-	0.1378	-

Table 93. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 60. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat recommended footprint



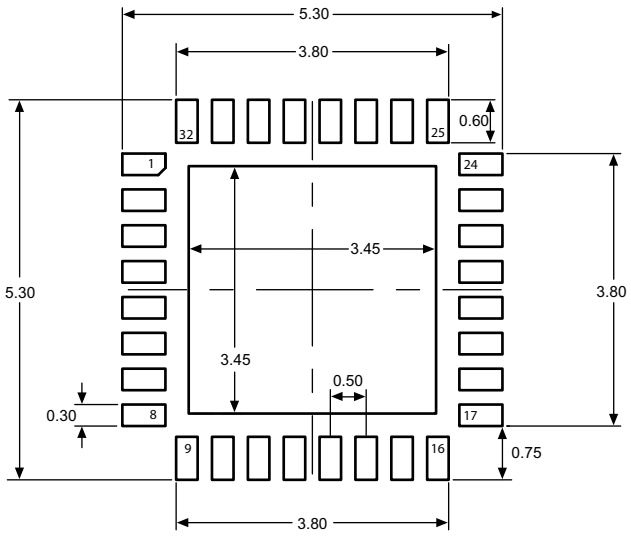
1. Dimensions are expressed in millimeters.

Table 94. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 62. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat recommended footprint



1. Dimensions are expressed in millimeters.