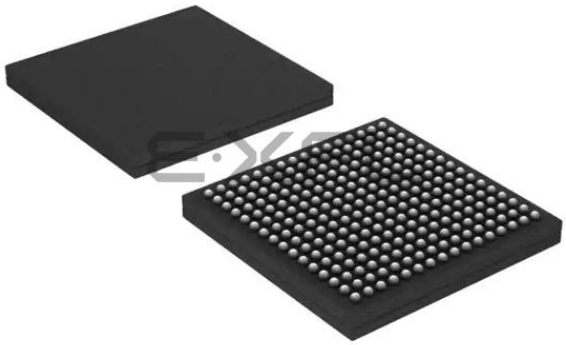

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	AVR
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	EBI/EMI, Ethernet, I²C, Memory Card, PS/2, SPI, SSC, UART/USART, USB
Peripherals	AC'97, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	160
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	D/A 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-CTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at32ap7000-ctut

2.0.1 AVR32AP CPU

- 32-bit load/store AVR32B RISC architecture.
  - Up to 15 general-purpose 32-bit registers.
  - 32-bit Stack Pointer, Program Counter and Link Register reside in register file.
  - Fully orthogonal instruction set.
  - Privileged and unprivileged modes enabling efficient and secure Operating Systems.
  - Innovative instruction set together with variable instruction length ensuring industry leading code density.
  - DSP extention with saturating arithmetic, and a wide variety of multiply instructions.
  - SIMD extention for media applications.
- 7 stage pipeline allows one instruction per clock cycle for most instructions.
  - Java Hardware Acceleration.
  - Byte, half-word, word and double word memory access.
  - Unaligned memory access.
  - Shadowed interrupt context for INT3 and multiple interrupt priority levels.
  - Dynamic branch prediction and return address stack for fast change-of-flow.
  - Coprocessor interface.
- Full MMU allows for operating systems with memory protection.
- 16Kbyte Instruction and 16Kbyte data caches.
  - Virtually indexed, physically tagged.
  - 4-way associative.
  - Write-through or write-back.
- Nexus Class 3 On-Chip Debug system.
  - Low-cost NanoTrace supported.

2.0.2 Pixel Coprocessor (PICO)

- Coprocessor coupled to the AVR32 CPU Core through the TCB Bus.
  - Coprocessor number one on the TCB bus.
- Three parallel Vector Multiplication Units (VMU) where each unit can:
  - Multiply three pixel components with three coefficients.
  - Add the products from the multiplications together.
  - Accumulate the result or add an offset to the sum of the products.
- Can be used for accelerating:
  - Image Color Space Conversion.
    - Configurable Conversion Coefficients.
    - Supports packed and planar input and output formats.
    - Supports subsampled input color spaces (i.e 4:2:2, 4:2:0).
  - Image filtering/scaling.
    - Configurable Filter Coefficients.
    - Throughput of one sample per cycle for a 9-tap FIR filter.
    - Can use the built-in accumulator to extend the FIR filter to more than 9-taps.
    - Can be used for bilinear/bicubic interpolations.
  - MPEG-4/H.264 Quarter Pixel Motion Compensation.
- Flexible input Pixel Selector.
  - Can operate on numerous different image storage formats.
- Flexible Output Pixel Inserter.
  - Scales and saturates the results back to 8-bit pixel values.
  - Supports packed and planar output formats.

- Configurable coefficients with flexible fixed-point representation.

2.0.3 Debug and Test system

- IEEE1149.1 compliant JTAG and boundary scan
- Direct memory access and programming capabilities through JTAG interface
- Extensive On-Chip Debug features in compliance with IEEE-ISTO 5001-2003 (Nexus 2.0) Class 3
- Auxiliary port for high-speed trace information
- Hardware support for 6 Program and 2 data breakpoints
- Unlimited number of software breakpoints supported
- Advanced Program, Data, Ownership, and Watchpoint trace supported

2.0.4 DMA Controller

- 2 HSB Master Interfaces
- 3 Channels
- Software and Hardware Handshaking Interfaces
  - 11 Hardware Handshaking Interfaces
- Memory/Non-Memory Peripherals to Memory/Non-Memory Peripherals Transfer
- Single-block DMA Transfer
- Multi-block DMA Transfer
  - Linked Lists
  - Auto-Reloading
  - Contiguous Blocks
- DMA Controller is Always the Flow Controller
- Additional Features
  - Scatter and Gather Operations
  - Channel Locking
  - Bus Locking
  - FIFO Mode
  - Pseudo Fly-by Operation

2.0.5 Peripheral DMA Controller

- Transfers from/to peripheral to/from any memory space without intervention of the processor.
- Next Pointer Support, forbids strong real-time constraints on buffer management.
- Eighteen channels
  - Two for each USART
  - Two for each Serial Synchronous Controller
  - Two for each Serial Peripheral Interface

2.0.6 Bus system

- HSB bus matrix with 10 Masters and 8 Slaves handled
  - Handles Requests from the CPU Icache, CPU Dcache, HSB bridge, HISI, USB 2.0 Controller, LCD Controller, Ethernet Controller 0, Ethernet Controller 1, DMA Controller 0, DMA Controller 1, and to internal SRAM 0, internal SRAM 1, PB A, PB B, EBI and, USB.

  - Round-Robin Arbitration (three modes supported: no default master, last accessed default master, fixed default master)
  - Burst Breaking with Slot Cycle Limit
  - One Address Decoder Provided per Master
- 2 Peripheral buses allowing each bus to run on different bus speeds.
  - PB A intended to run on low clock speeds, with peripherals connected to the PDC.
  - PB B intended to run on higher clock speeds, with peripherals connected to the DMACA.
- HSB-HSB Bridge providing a low-speed HSB bus running at the same speed as PBA
  - Allows PDC transfers between a low-speed PB bus and a bus matrix of higher clock speeds

An overview of the bus system is given in Figure 2-1 on page 4. All modules connected to the same bus use the same clock, but the clock to each module can be individually shut off by the Power Manager. The figure identifies the number of master and slave interfaces of each module connected to the HSB bus, and which DMA controller is connected to which peripheral.

4. Power Considerations

4.1 Power Supplies

The AT32AP7000 has several types of power supply pins:

- **VDDCORE pins: Power the core, memories, and peripherals. Voltage is 1.8V nominal.**
- **VDDIO pins: Power I/O lines. Voltage is 3.3V nominal.**
- **VDDPLL pin: Powers the PLL. Voltage is 1.8V nominal.**
- **VDDUSB pin: Powers the USB. Voltage is 1.8V nominal.**
- **VDDOSC pin: Powers the oscillators. Voltage is 1.8V nominal.**

The ground pins GND are common to VDDCORE and VDDIO. The ground pin for VDDPLL is GNDPLL, and the GND pin for VDDOSC is GNDOSC.

See ”Electrical Characteristics” on page 928 for power consumption on the various supply pins.

4.2 Power Supply Connections

Special considerations should be made when connecting the power and ground pins on a PCB. Figure 4-1 shows how this should be done.

Figure 4-1. Connecting analog power supplies

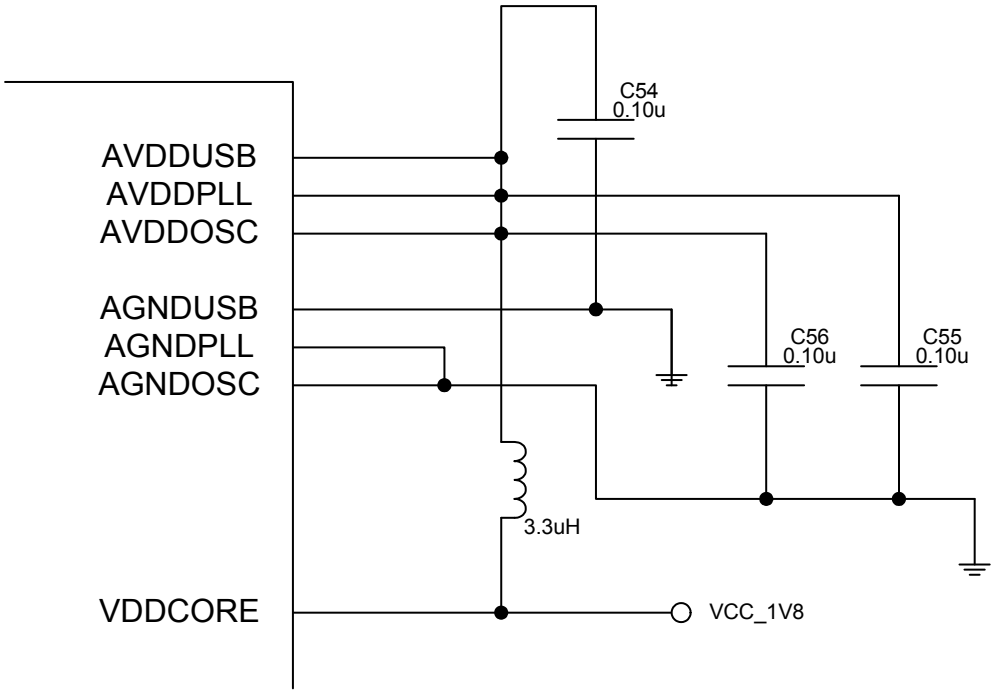

Table 6-2. HSB masters

Master 0	CPU Dcache
Master 1	CPU Icache
Master 2	HSB-HSB Bridge
Master 3	ISI DMA
Master 4	USBA DMA
Master 5	LCD Controller DMA
Master 6	Ethernet MAC0 DMA
Master 7	Ethernet MAC1 DMA
Master 8	DMAC Master Interface 0
Master 9	DMAC Master Interface 1

Each slave has its own arbiter, thus allowing a different arbitration per slave. The slave number in the table below can be used to index the HMATRIX control registers. For example, SCFG3 is associated with PBB.

Table 6-3. HSB slaves

Slave 0	Internal SRAM 0
Slave 1	Internal SRAM1
Slave 2	PBA
Slave 3	PBB
Slave 4	EBI
Slave 5	USBA data
Slave 6	LCDC configuration
Slave 7	DMACA configuration

Table 7-1. Peripheral Address Mapping (Continued)

Address		Peripheral Name	Bus
0xFFE03800	PIOE	Parallel Input/Output 2 - PIOE	PB A
0xFFE03C00	PSIF	PS2 Interface - PSIF	PB A
0xFFF00000	PM	Power Manager - PM	PB B
0xFFF00080	RTC	Real Time Counter- RTC	PB B
0xFFF000B0	WDT	WatchDog Timer- WDT	PB B
0xFFF00100	EIC	External Interrupt Controller - EIC	PB B
0xFFF00400	INTC	Interrupt Controller - INTC	PB B
0xFFF00800	HMATRIX	HSB Matrix - HMATRIX	PB B
0xFFF00C00	TC0	Timer/Counter - TC0	PB B
0xFFF01000	TC1	Timer/Counter - TC1	PB B
0xFFF01400	PWM	Pulse Width Modulation Controller - PWM	PB B
0xFFF01800	MACB0	Ethernet MAC - MACB0	PB B
0xFFF01C00	MACB1	Ethernet MAC - MACB1	PB B
0xFFF02000	ABDAC	Audio Bitstream DAC - ABDAC	PB B
0xFFF02400	MCI	MultiMedia Card Interface - MCI	PB B
0xFFF02800	AC97C	AC97 Controller - AC97C	PB B
0xFFF02C00	ISI	Image Sensor Interface - ISI	PB B
0xFFF03000	USBA	USB Configuration Interface - USBA	PB B
0xFFF03400	SMC	Static Memory Controller - SMC	PB B

Table 7-2. Interrupt Request Signal Map

Group	Line	Signal
12	0	SSC2
13	0	PIOA
14	0	PIOB
15	0	PIOC
16	0	PIOD
17	0	PIOE
18	0	PSIF
19	0	EIC0
	1	EIC1
	2	EIC2
	3	EIC3
20	0	PM
21	0	RTC
22	0	TC00
	1	TC01
	2	TC02
23	0	TC10
	1	TC11
	2	TC12
24	0	PWM
25	0	MACB0
26	0	MACB1
27	0	ABDAC
28	0	MCI
29	0	AC97C
30	0	ISI
31	0	USBA
32	0	EBI

7.3 DMACA Handshake Interface Map

The following table details the hardware handshake map between the DMACA and the peripherals attached to it: :

Table 7-3. Hardware Handshaking Connection

Request	Hardware Handshaking Interface
MCI RX	0
MCI TX	1
ABDAC TX	2
AC97C CHANNEL A RX	3
AC97C CHANNEL A TX	4
AC97C CHANNEL B RX	5
AC97C CHANNEL B TX	6
EXTERNAL DMA REQUEST 0	7
EXTERNAL DMA REQUEST 1	8
EXTERNAL DMA REQUEST 2	9
EXTERNAL DMA REQUEST 3	10

7.4 Clock Connections

7.4.1 Timer/Counters

Each Timer/Counter channel can independently select an internal or external clock source for its counter:

Table 7-4. Timer/Counter clock connections

Timer/Counter	Source	Name	Connection
0	Internal	TIMER_CLOCK1	clk_osc32
		TIMER_CLOCK2	clk_pbb / 4
		TIMER_CLOCK3	clk_pbb / 8
		TIMER_CLOCK4	clk_pbb / 16
		TIMER_CLOCK5	clk_pbb / 32
	External	XC0	See Section 7.7
		XC1	
		XC2	
1	Internal	TIMER_CLOCK1	clk_osc32
		TIMER_CLOCK2	clk_pbb / 4
		TIMER_CLOCK3	clk_pbb / 8
		TIMER_CLOCK4	clk_pbb / 16
		TIMER_CLOCK5	clk_pbb / 32
	External	XC0	See Section 7.7
		XC1	
		XC2	

7.4.2 USARTs

Each USART can be connected to an internally divided clock:

Table 7-5. USART clock connections

USART	Source	Name	Connection
0	Internal	CLK_DIV	clk_pba / 8
1			
2			
3			

Table 7-14. IO Pins without multiplexing (Continued)

PX32	EBI - ADDR[16]
PX33	EBI - ADDR[17]
PX34	EBI - ADDR[18]
PX35	EBI - ADDR[19]
PX36	EBI - ADDR[20]
PX37	EBI - ADDR[21]
PX38	EBI - ADDR[22]
PX39	EBI - NCS[0]
PX40	EBI - NCS[1]
PX41	EBI - NCS[3]
PX42	EBI - NRD
PX43	EBI - NWE0
PX44	EBI - NWE1
PX45	EBI - NWE3
PX46	EBI - SDCK
PX47	EBI - SDCKE
PX48	EBI - RAS
PX49	EBI - CAS
PX50	EBI - SDWE
PX51	EBI - SDA10
PX52	EBI - NANDOE
PX53	EBI - NANDWE

7.8 Peripheral overview

7.8.1 External Bus Interface

- Optimized for Application Memory Space support
- Integrates Three External Memory Controllers:
  - Static Memory Controller
  - SDRAM Controller
  - ECC Controller
- Additional Logic for NAND Flash/SmartMedia™ and CompactFlash™ Support
  - SmartMedia support: 8-bit as well as 16-bit devices are supported
  - CompactFlash support: all modes (Attribute Memory, Common Memory, I/O, True IDE) are supported but the signals _IOIS16 (I/O and True IDE modes) and _ATA SEL (True IDE mode) are not handled.
- Optimized External Bus:
  - 16- or 32-bit Data Bus
  - Up to 26-bit Address Bus, Up to 64-Mbytes Addressable
  - Optimized pin multiplexing to reduce latencies on External Memories
- Up to 6 Chip Selects, Configurable Assignment:
  - Static Memory Controller on NCS0
  - SDRAM Controller or Static Memory Controller on NCS1
  - Static Memory Controller on NCS2
  - Static Memory Controller on NCS3, Optional NAND Flash/SmartMedia™ Support
  - Static Memory Controller on NCS4 - NCS5, Optional CompactFlash™ Support

7.8.2 Static Memory Controller

- 6 Chip Selects Available
- 64-Mbyte Address Space per Chip Select
- 8-, 16- or 32-bit Data Bus
-

7.8.17 Ethernet MAC

- Compatibility with IEEE Standard 802.3
- 10 and 100 Mbits per second data throughput capability
- Full- and half-duplex operations
- MII or RMII interface to the physical layer
- Register Interface to address, data, status and control registers
- DMA Interface, operating as a master on the Memory Controller
- Interrupt generation to signal receive and transmit completion
- 28-byte transmit and 28-byte receive FIFOs
- Automatic pad and CRC generation on transmitted frames
- Address checking logic to recognize four 48-bit addresses
- Support promiscuous mode where all valid frames are copied to memory
- Support physical layer management through MDIO interface control of alarm and update time/calendar data in

7.8.18 Image Sensor Interface

- ITU-R BT. 601/656 8-bit mode external interface support
- Support for ITU-R BT.656-4 SAV and EAV synchronization
- Vertical and horizontal resolutions up to 2048 x 2048
- Preview Path up to 640*480
- Support for packed data formatting for YCbCr 4:2:2 formats
- Preview scaler to generate smaller size image 50
- Programmable frame capture rate

TCMR.START = Receive start

RFMR.FSOS = None (Input)

RCMR.START = any on RF (edge/level)

Fix/Workaround

None.

30. USART - TXD signal is floating in Modem and Hardware Handshaking mode

    The TXD signal is floating in Modem and Hardware Handshaking mode, but should be pulled up.

    Fix/Workaround

    Enable pullup on this line in the PIO.

31. PWM - Impossible to update a period equal to 0 by using the CUPD register

    It is impossible to UPDATE a period equal to 0 by the using of the UPDATE register (CUPD).

    Fix/Workaround

    To update a period equal to 0, write directly to the CPRD register.

32. WDT Clear is blocked after WDT Reset

    A watchdog timer event will, after reset, block writes to the WDT_CLEAR register, preventing the program to clear the next Watchdog Timer Reset.

    Fix/Workaround

    If the RTC is not used a write to AVR32_RTC.ctrl.pclr = 1, instead of writing to AVR32_WDT.clr, will reset the prescaler and th

18. JTAG CLAMP instruction does not work as intended

    During the CLAMP instruction, the Boundary Scan register should be stable and only the BYPASS register selected. Instead, the bscan register will capture and shift as if it was selected, reducing the usefulness of the CLAMP instruction.

    Fix/Workaround

    None.

19. High current consumption in reset with no clocks enabled

    In connection with the datacache RAM access, a higher current consumption than expected can be observed during reset. The error is non-functional and does not affect reliability of the device.

    Fix/Workaround