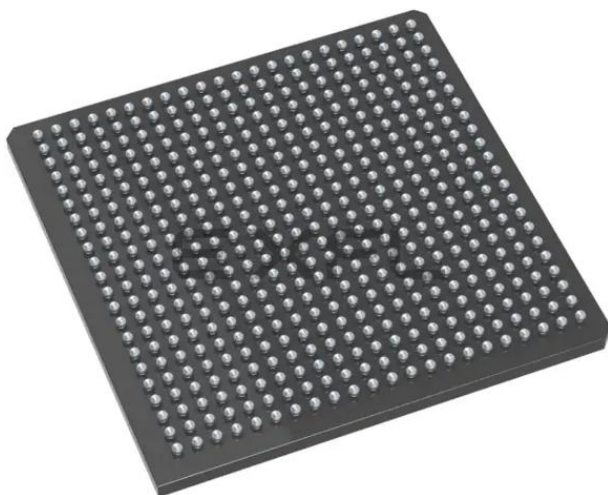




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	12084
Total RAM Bits	933888
Number of I/O	233
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl010t-1fg484m

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Table 3 • Recommended Operating Conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
VPPNVM	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
Notes:							
1. Programming at this temperature range is available only with VPP in 3.3 V Range							
2. Power supply ramps must all be strictly monotonic, without plateaus.							

Table 4 • FPGA Operating Limits

Product Grade	Element	Programming Temperature	Operating Temperature	Programming Cycles	Retention (Biased/Unbiased)	Note
Military	FPGA	Min T _J = 0°C Max T _J = 85°C	Min T _J = -55°C Max T _J = 125°C	500	10 Years	—
		Min T _J = -40°C Max T _J = 100°C	Min T _J = -55°C Max T _J = 125°C	500	10 Years	*
Note: *: Programming at this temperature range is available only with VPP in 3.3 V Range						

Table 5 • Embedded Flash Limits

Product Grade	Element	Programming Temperature	Maximum Operating Temperature	Programming Cycles	Retention (Biased/Unbiased)
Military	Embedded flash	Min T _J = -55°C Max T _J = 125°C	Min T _J = -55°C Max T _J = 125°C	< 10,000 cycles per pages, up to one million cycles per eNVM array	10 Years

Table 6 • Device Storage Temperature and Retention

Product Grade	Storage Temperature (Tstg)	Retention
Military	Min T _J = -55°C Max T _J = 125°C	10 Years

4.2 Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to -1.0 V for no longer than 10% or the period. The current during the transition must not exceed 100mA.

For AC signals, the input signal may overshoot during transitions to VCCI + 1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100mA.

Note: The above specification does not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant to the PCI standard including the PCI overshoot/undershoot specifications.

8.2. Output Buffer and AC Loading

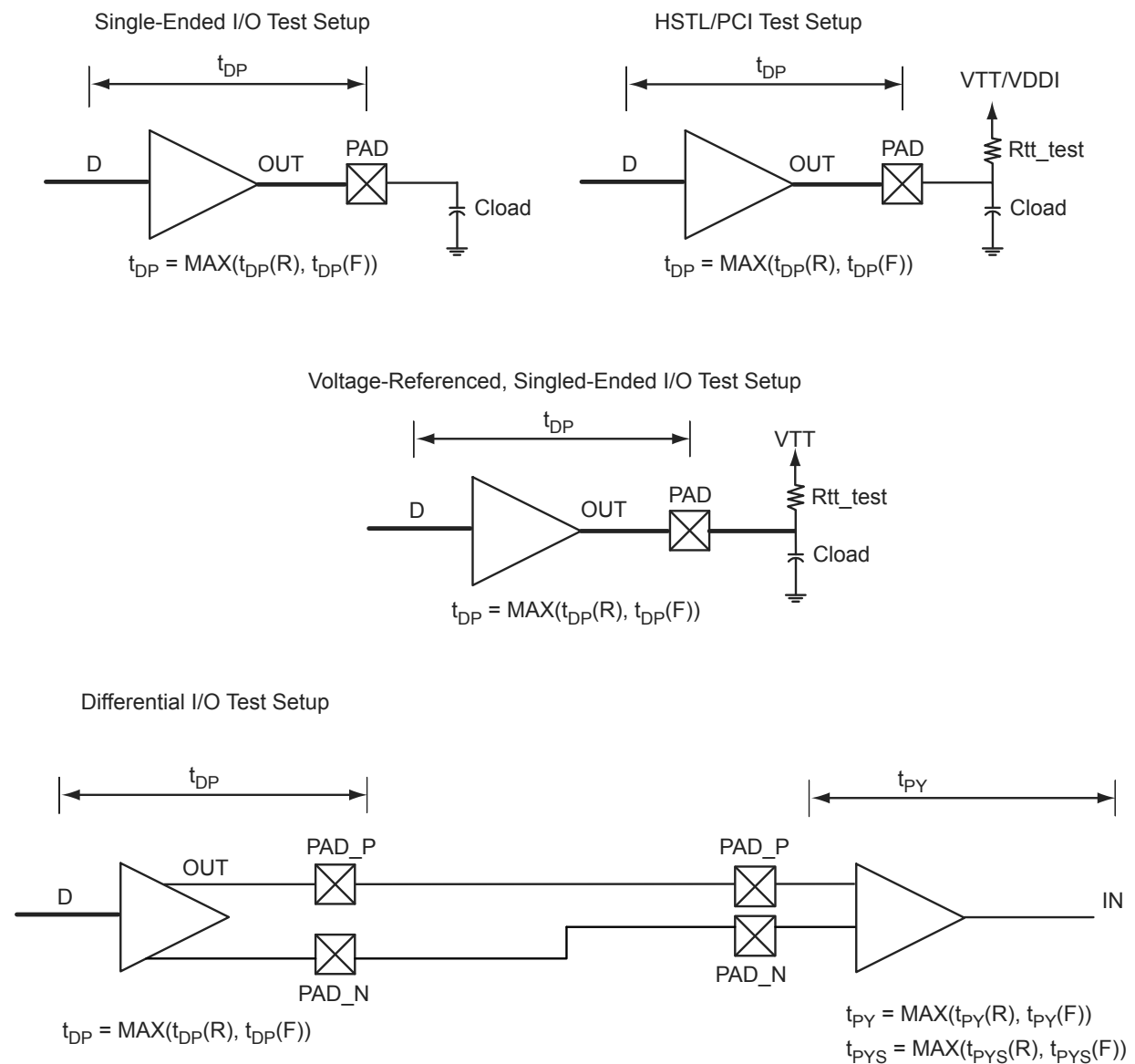


Figure 3 • Output Buffer AC Loading

Table 17 • Maximum Frequency Summary for Worst-Case Military Conditions

Single-Ended I/O	MSIO	MSIOD	DDRIO	Units
PCI 3.3 V	280	–	–	MHz
LVTTL 3.3 V	270	–	–	MHz
LVC MOS 3.3 V	270	–	–	MHz
LVC MOS 2.5 V	180	185	180	MHz
LVC MOS 1.8 V	130	180	180	MHz
LVC MOS 1.5 V	70	95	105	MHz
LVC MOS 1.2 V	50	70	90	MHz
LPDDR - LVC MOS 1.8 V mode	–	–	180	MHz
Voltage-Referenced I/O	MSIO	MSIOD	DDRIO	Units
LPDDR	–	–	180	MHz
HSTL 1.5 V	–	–	180	MHz
SSTL 2.5 V	225	240	180	MHz
SSTL 1.8 V	–	–	300	MHz
SSTL 1.5 V	–	–	300	MHz
Differential I/O	MSIO	MSIOD	DDRIO	Units
LVPECL (input only)	405	–	–	MHz
LVDS 3.3 V	240	240	–	MHz
LVDS 2.5 V	240	240	–	MHz
RS DS	230	240	–	MHz
BLVDS	225	–	–	MHz
MLVDS	225	–	–	MHz
Mini-LVDS	230	240	–	MHz

Table 24 • LVTTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications
(Applicable to MSIO Bank* Only)

Output Drive Selection	VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
2 mA	2.4	0.4	2	2
4 mA	2.4	0.4	4	4
8 mA	2.4	0.4	8	8
12 mA	2.4	0.4	12	12
16 mA	2.4	0.4	16	16
20 mA	2.4	0.4	18	18
Note: * Software Configurator GUI displays the Commercial/Industrial numeric values. The actual drive capability at temperature is defined in Table 24.				

8.6.2.2 AC Switching Characteristics

Worst-case Military conditions: $T_J = 125^{\circ}\text{C}$, VDD = 1.14 V, VDDI = 3.15 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 25 • LVTTTL/LVCMOS 3.3 V Receiver Characteristics for MSIO I/O Banks (Input Buffers)

Worst-case Military conditions: $T_J = 125^{\circ}\text{C}$, VDD = 1.14 V, VDDI = 3.15 V

	On-Die Termination (ODT)	Speed Grade -1		Units
		t_{PY}	t_{PYS}	
LVTTTL/LVCMOS 3.3 V (for MSIO I/O Bank)	None	2.416	2.443	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 26 • LVTTTL/LVCMOS 3.3 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

Worst-case Military conditions: $T_J = 125^{\circ}\text{C}$, VDD = 1.14 V, VDDI = 3.15 V

Output Drive Selection	Slew Control	Speed Grade -1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
2mA	slow	3.515	3.826	3.242	2.024	3.636	ns
4mA	slow	2.565	2.948	2.774	3.339	4.896	ns
8mA	slow	2.349	2.568	2.528	5.013	5.329	ns
12mA	slow	2.261	2.324	2.386	6.389	6.05	ns
16mA	slow	2.274	2.287	2.369	6.671	6.256	ns
20mA	slow	2.372	2.206	2.306	6.976	6.541	ns

Table 32 • LVCMOS 2.5 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-case Military conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$ (continued)

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
6 mA	slow	3.189	2.716	3.169	5.56	5.092	ns
	medium	2.886	2.473	2.876	5.273	4.752	ns
	medium_fast	2.749	2.355	2.738	5.127	4.167	ns
	fast	2.731	2.345	2.72	5.115	4.6	ns
8 mA	slow	3.132	2.646	3.109	5.686	5.207	ns
	medium	2.832	2.407	2.82	5.402	4.864	ns
	medium_fast	2.698	2.292	2.685	5.262	4.732	ns
	fast	2.684	2.282	2.671	5.252	4.724	ns
12 mA	slow	3.013	2.504	2.984	5.918	5.416	ns
	medium	2.72	2.284	2.707	5.657	5.074	ns
	medium_fast	2.592	2.176	2.578	5.537	4.949	ns
	fast	2.58	2.166	2.566	5.529	4.946	ns
16 mA	slow	2.936	2.415	2.902	6.136	5.577	ns
	medium	2.66	2.206	2.645	5.901	5.261	ns
	medium_fast	2.536	2.102	2.519	5.815	5.142	ns
	fast	2.523	2.093	2.506	5.81	5.137	ns
LVCMOS 2.5 V (for MSIO I/O Bank)							
2 mA	slow	3.933	4.352	4.22	2.358	3.838	ns
4 mA	slow	2.905	3.423	3.508	4.681	5.262	ns
6 mA	slow	2.687	2.995	3.155	5.561	5.73	ns
8 mA	slow	2.594	2.877	3.07	6.602	6.248	ns
12 mA	slow	2.623	2.732	2.944	6.974	6.478	ns
16 mA	slow	2.717	2.617	2.84	7.455	6.824	ns
LVCMOS 2.5 V (for MSIOD I/O Bank)							
2 mA	slow	2.403	2.922	2.89	5.397	5.202	ns
4 mA	slow	1.998	2.446	2.468	5.936	5.665	ns
6 mA	slow	1.861	2.329	2.375	6.391	6.068	ns
8 mA	slow	1.781	2.145	2.208	6.884	6.44	ns
12 mA	slow	1.804	2.039	2.108	7.23	6.685	ns

Table 39 • LVCMOS 1.8 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-case Military conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.71\text{ V}$ (continued)

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
12 mA	slow	3.795	3.096	3.773	6.773	6.067	ns
	medium	3.408	2.764	3.389	6.47	5.743	ns
	medium_fast	3.215	2.599	3.194	6.346	5.61	ns
	fast	3.196	2.584	3.175	6.335	5.604	ns
16 mA	slow	3.744	3.035	3.719	6.944	6.207	ns
	medium	3.358	2.712	3.339	6.657	5.868	ns
	medium_fast	3.175	2.546	3.153	6.547	5.751	ns
	fast	3.156	2.531	3.133	6.541	5.747	ns
LVCMOS 1.8 V (for MSIO I/O Bank)							
2 mA	slow	3.957	4.784	5.023	5.643	5.866	ns
4 mA	slow	3.668	4.162	4.485	6.543	6.382	ns
6 mA	slow	3.586	3.994	4.358	7.622	6.941	ns
8 mA	slow	3.616	3.782	4.162	7.988	7.161	ns
10 mA	slow	3.662	3.732	4.121	8.396	7.423	ns
12 mA	slow	3.75	3.615	4.006	8.576	7.543	ns
LVCMOS 1.8 V (for MSIOD I/O Bank)							
2 mA	slow	3.048	3.692	3.898	5.818	5.609	ns
4 mA	slow	2.5	3.088	3.288	6.421	6.121	ns
6 mA	slow	2.225	2.747	2.937	7.18	6.753	ns
8 mA	slow	2.233	2.72	2.904	7.49	6.992	ns
10 mA	slow	2.263	2.577	2.759	7.851	7.253	ns

8.6.5 1.5 V LVCMOS

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-11A.

8.6.5.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 40 • LVCMOS 1.5 V Minimum and Maximum DC Input and Output Levels

Symbols	Parameters	Min	Typ	Max	Units
LVCMOS 1.5 V Recommended DC Operating Conditions					
VDDI	Supply voltage	1.425	1.5	1.575	V
LVCMOS 1.5 V DC Input Voltage Specification					
VIH (DC)	DC input logic High for (MSIOD and DDRIO I/O banks)	$0.65 \times V_{DDI}$	–	1.575	V
VIH (DC)	DC input logic High (for MSIO I/O Bank)	$0.65 \times V_{DDI}$	–	2.75	V
VIL (DC)	DC input logic Low	–0.3	–	$0.35 \times V_{DDI}$	V
IIH (DC)	Input current High	–	–	10	μA
IIL (DC)	Input current Low	–	–	10	μA
LVCMOS 1.5 V DC Output Voltage Specification					
VOH	DC output logic High	$V_{DDI} \times 0.75$	–	–	V
VOL	DC output logic Low	–	–	$V_{DDI} \times 0.25$	V

Table 51 • LVCMOS 1.2 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Military Conditions: $T_J=125^{\circ}\text{C}$, $V_{DD}=1.14\text{ V}$, $V_{DDI}=1.14\text{ V}$ (continued)

Output Drive Selection	Slew Control	Speed Grade -1					Units
		t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
LVCMOS 1.2 V (for MSIOD I/O Bank)							
2 mA	slow	4.048	5.123	5.552	8.401	7.824	ns
4 mA	slow	3.941	4.406	4.814	9.422	8.656	ns

8.6.7 3.3 V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3 V standards specify support for 33 MHz and 66 MHz PCI bus applications.

8.6.7.1 Minimum and Maximum Input and Output Levels Specification

Table 52 • PCI/PCI-X DC Voltage Specification (Applicable to MSIO Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
PCI/PCIX Recommended DC Operating Conditions						
V_{DDI}	Supply voltage		3.15	3.3	3.45	V
PCI/PCIX DC Input Voltage Specification						
V_I	DC input voltage		0	—	3.45	V
$I_{IH}(\text{DC})$	Input current High		—	—	10	μA
$I_{IL}(\text{DC})$	Input current Low		—	—	10	μA
PCI/PCIX DC Output Voltage Specification						
V_{OH}	DC output logic High		Per PCI Specification			V
V_{OL}	DC output logic Low		Per PCI Specification			V

Table 53 • PCI/PCI-X AC Specifications (Applicable to MSIO Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
PCI/PCI-X AC Specifications						
D_{max}	Maximum data rate (MSIO I/O Bank)	AC Loading: per JEDEC specifications	—	—	560	Mbps
PCI/PCI-X AC Test Parameters Specifications						
V_{trip}	Measuring/trip point for data path (falling edge)		—	$0.615 \times V_{DDI}$	—	V
V_{trip}	Measuring/trip point for data path (rising edge)		—	$0.285 \times V_{DDI}$	—	V
R_{tt_test}	Resistance for data test path		—	25	—	Ω
R_{ent}	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		—	2k	—	Ω
C_{ent}	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		—	5	—	pF
C_{load}	Capacitive loading for data path (t_{DP})		—	10	—	pF

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 82 • LPDDR - LVCMOS 1.8 V AC Switching Characteristics for Transmitter DDRIO I/O Bank (Output and Tristate Buffers)

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.71\text{ V}$

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
2 mA	slow	4.681	4.017	4.69	5.388	4.852	ns
	medium	4.211	3.599	4.219	5.058	4.488	ns
	medium_fast	3.978	3.392	3.986	4.874	4.327	ns
	fast	3.953	3.373	3.961	4.858	4.316	ns
4 mA	slow	4.355	3.657	4.346	5.967	5.399	ns
	medium	3.886	3.246	3.879	5.628	5.01	ns
	medium_fast	3.656	3.05	3.647	5.461	4.845	ns
	fast	3.635	3.033	3.626	5.447	4.838	ns
6 mA	slow	4.105	3.422	4.092	6.221	5.599	ns
	medium	3.68	3.05	3.668	5.9	5.257	ns
	medium_fast	3.477	2.867	3.463	5.739	5.118	ns
	fast	3.451	2.849	3.437	5.72	5.104	ns
8 mA	slow	4.015	3.32	3.998	6.458	5.808	ns
	medium	3.59	2.947	3.574	6.129	5.449	ns
	medium_fast	3.383	2.761	3.366	5.963	5.304	ns
	fast	3.357	2.746	3.34	5.954	5.289	ns
10 mA	slow	3.888	3.18	3.864	6.739	6.045	ns
	medium	3.485	2.822	3.467	6.422	5.7	ns
	medium_fast	3.281	2.642	3.26	6.277	5.553	ns
	fast	3.258	2.627	3.238	6.27	5.546	ns
12 mA	slow	3.795	3.096	3.773	6.773	6.067	ns
	medium	3.408	2.764	3.389	6.47	5.743	ns
	medium_fast	3.215	2.599	3.194	6.346	5.61	ns
	fast	3.196	2.584	3.175	6.335	5.604	ns
16 mA	slow	3.744	3.035	3.719	6.944	6.207	ns
	medium	3.358	2.712	3.339	6.657	5.868	ns
	medium_fast	3.175	2.546	3.153	6.547	5.751	ns
	fast	3.156	2.531	3.133	6.541	5.747	ns

8.8.1.2 LVDS25 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 85 • LVDS25 Receiver Characteristics

Worst-Case Military Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	On-Die Termination (ODT)	Speed Grade -1	Units
		t_{PY}	
LVDS (for MSIO I/O Bank)	None	3.061	ns
	100	3.057	ns
LVDS (for MSIOD I/O Bank)	None	2.792	ns
	100	2.787	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 86 • LVDS25 Transmitter Characteristics

Worst-Case Military Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	Speed Grade -1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVDS (for MSIO I/O Bank)	2.299	2.602	2.589	2.305	2.32	ns
LVDS (for MSIOD I/O Bank)						
No pre-emphasis	1.656	1.845	1.838	1.992	1.969	ns
Min pre-emphasis	1.583	1.868	1.866	2.018	1.998	ns
Med pre-emphasis	1.559	1.893	1.886	2.045	2.021	ns

8.8.1.3 LVDS33 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 87 • LVDS33 Receiver Characteristics

Worst-Case Military Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 3.15\text{ V}$

	On Die Termination (ODT)	Speed Grade -1	Units
		t_{PY}	
LVDS33 (for MSIO I/O Bank)	None	2.763	ns
	100	2.76	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 88 • LVDS33 Transmitter Characteristics

Worst-Case Military Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 3.15\text{ V}$

	Speed Grade -1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVDS33 (for MSIO I/O Bank)	2.069	2.112	2.106	2.078	2.09	ns

8.8.2 B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

8.8.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 89 • B-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Bus-LVDS Recommended DC Operating Conditions						
VDDI	Supply voltage		2.375	2.5	2.625	V
Bus-LVDS DC Input Voltage Specification						
VI	DC input voltage		0	–	2.925	V
IIH (DC)	Input current High		–	–	10	μA
IIL (DC)	Input current Low		–	–	10	μA
Bus-LVDS DC Output Voltage Specification (for MSIO I/O Bank only)						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
Bus-LVDS Differential Voltage Specification						
VOD	Differential output voltage swing (for MSIO I/O Bank only)		65	–	460	mV
VOCM	Output common mode voltage (for MSIO I/O Bank only)		1.1	–	1.5	V
VICM	Input common mode voltage		0.05	–	2.4	V
VID	Input differential voltage		0.1	–	VDDI	V

Table 90 • B-LVDS AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Bus-LVDS Maximum AC Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	450	Mbps
Bus-LVDS Impedance Specifications						
Rt	Termination resistance		–	27	–	Ω
Bus-LVDS AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF

Table 106 • LVPECL Maximum AC Switching Speeds (Applicable to MSIO I/O Banks Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVPECL AC Specifications						
Fmax	Maximum data rate (for MSIO I/O Bank)		–	–	810	Mbps

8.8.6.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 107 • LVPECL Receiver Characteristics

Worst-case Military conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 3.15\text{ V}$

	On-Die Termination (ODT)	t _{py}	Units
		Speed Grade –1	
LVPECL (for MSIO I/O Bank)	None	2.71	ns
	100	2.71	ns

8.9 I/O Register Specifications

8.9.1 Input Register

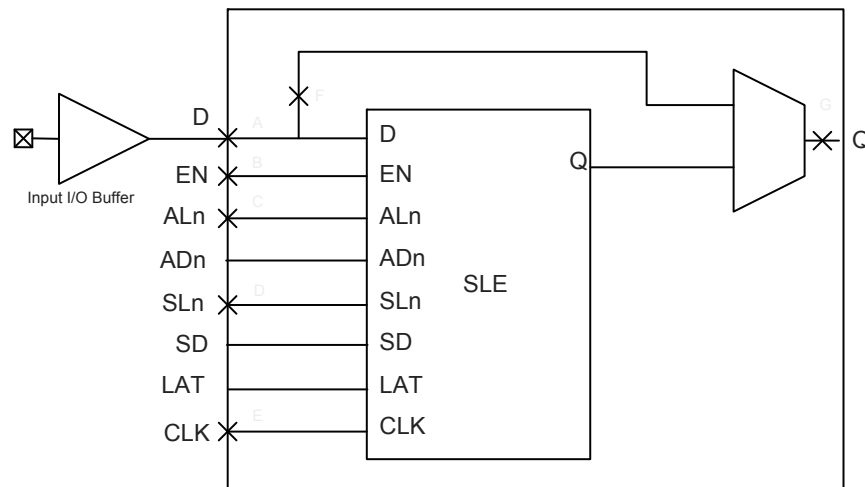


Figure 5 • Timing Model for Input Register

9. Logic Element Specifications

9.1 4-input LUT (LUT-4)

The IGLOO2 and SmartFusion2 SoC FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *SmartFusion2 and IGLOO2 Macro Library Guide*.

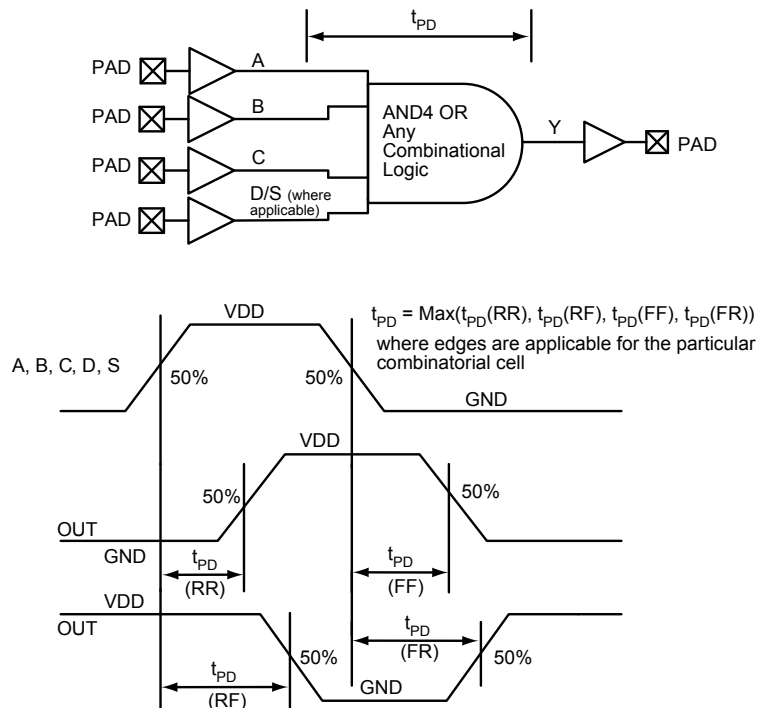


Figure 13 • LUT-4

Timing Characteristics

Table 112 • Combinatorial Cell Propagation Delays

Worst-Case Military Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Combinatorial Cell	Equation	Parameter	Speed Grade -1	Units
INV	$Y = !A$	t_{PD}	0.106	ns
AND2	$Y = A \cdot B$	t_{PD}	0.17	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.157	ns
OR2	$Y = A + B$	t_{PD}	0.17	ns
NOR2	$Y = !(A + B)$	t_{PD}	0.157	ns
XOR2	$Y = A \oplus B$	t_{PD}	0.17	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	0.236	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	0.217	ns
AND4	$Y = A \cdot B \cdot C \cdot D$	t_{PD}	0.384	ns

Table 119 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1Kx18
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tsrstsu	Synchronous Reset Setup Time	0.233	–	ns
tsrsthd	Synchronous Reset Hold Time	0.037	–	ns
twesu	Write Enable Setup Time	0.402	–	ns
twehd	Write Enable Hold Time	0.25	–	ns
Fmax	Maximum Frequency	–	300	MHz

Table 120 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2Kx9
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tcy	Clock Period	3.333	–	ns
tclkmpwh	Clock Minimum Pulse Width High	1.5	–	ns
tclkmpwl	Clock Minimum pulse Width Low	1.5	–	ns
tpicy	Pipelined Clock Period	3.333	–	ns
tpclkmpwh	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
tpclkmpwl	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.346	ns
	Read Access Time without Pipeline Register	–	2.346	ns
	Access Time with Feed-Through Write Timing	–	1.578	ns
taddrsu	Address Setup Time	0.49	–	ns
taddrhd	Address Hold Time	0.282	–	ns
tdsu	Data Setup Time	0.346	–	ns
tdhd	Data Hold Time	0.084	–	ns
tblksu	Block Select Setup Time	0.214	–	ns
tblkhd	Block Select Hold Time	0.223	–	ns
tblk2q	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	1.578	ns
tblkmpw	Block Select Minimum Pulse Width	0.218	–	ns
trdesu	Read Enable Setup Time	0.5	–	ns
trdehd	Read Enable Hold Time	0.073	–	ns
trdplesu	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
trdpleshd	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
tr2q	Asynchronous Reset to Output Propagation Delay	–	1.569	ns

Table 128 • uSRAM (RAM128x8) in 128x8 Mode
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
tr2q	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.865	ns
tsrstu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.062	–	ns
tccy	Write Clock Period	4	–	ns
tcclkmph	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclkmpl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblksu	Write Block Setup Time	0.417	–	ns
tblkhd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.104	–	ns
tdinchd	Write Input Data hold Time	0.142	–	ns
taddrsu	Write Address Setup Time	0.091	–	ns
taddrhd	Write Address Hold Time	0.24	–	ns
twecsu	Write Enable Setup Time	0.41	–	ns
twechd	Write Enable Hold Time	-0.027	–	ns
fmax	Maximum Frequency	–	250	MHz

Table 129 • uSRAM (RAM256x4) in 256x4 Mode
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
tcy	Read Clock Period	4	–	ns
tclkmph	Read Clock Minimum Pulse Width High	1.8	–	ns
tclkmpl	Read Clock Minimum pulse Width Low	1.8	–	ns
tpcy	Read Pipe-line clock period	4	–	ns
tpclkmph	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
tpclkmpl	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.812	ns
taddrsu	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	1.993	–	ns
taddrhd	Read Address Hold Time in Synchronous Mode	0.125	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.669	–	ns
trdensu	Read Enable Setup Time	0.287	–	ns

Table 136 • Electrical Characteristics of the Crystal Oscillator – Low Gain Mode (32 kHz)

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Min	Typ	Max	Units
IDYNXTAL	Operating current	–	0.044	–	mA
VIHXTAL	Input logic level High	$0.9 \times V_{PP}$	–	–	V
VILXTAL	Input logic level Low	–	–	$0.1 \times V_{PP}$	V
SUXTAL	Startup time (with regard to stable oscillator output)	–	–	120	ms

14. On-Chip Oscillator

Table 137 and Table 138 describe the electrical characteristics of the available on-chip oscillators in the IGLOO2 FPGAs and SmartFusion2 SoC FPGAs.

Table 137 • Electrical Characteristics of the 50 MHz RC Oscillator

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Condition	Min	Typ	Max	Units
F50RC	Operating frequency	–	–	50	–	MHz
ACC50RC	Accuracy	–	–	1	8	%
CYC50RC	Output duty cycle	–	–	49–51	46–54	%
JIT50RC	Output jitter (peak to peak)	Period Jitter	–	200	500	ps
		Cycle-to-Cycle Jitter	–	320	900	ps
IDYN50RC	Operating current	–	–	8.5	–	mA

Table 138 • Electrical Characteristics of the 1 MHz RC Oscillator

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Condition	Min	Typ	Max	Units
F1RC	Operating frequency	–	–	1	–	MHz
ACC1RC	Accuracy	–	–	1	6	%
CYC1RC	Output duty cycle	–	–	49–51	46.5–53.5	%
JIT1RC	Output jitter (peak to peak)	Period Jitter	–	10	36	ps
		Cycle-to-Cycle Jitter	–	10	50	ps
IDYN1RC	Operating current	–	–	0.1	–	mA
SU1RC	Startup time	–	–	–	20	μs

18. System Controller SPI Characteristics

Table 143 • System Controller SPI Characteristics
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Symbol	Description	Conditions	All Devices/Speed Grades			Units	Notes
			Min	Typ	Max		
sp1	SC_SPI_SCK minimum period	–	20	–	–	ns	–
sp2	SC_SPI_SCK minimum pulse width high	–	10	–	–	ns	–
sp3	SC_SPI_SCK minimum pulse width low	–	10	–	–	ns	–
sp4	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS rise time (10%-90%) 1	I/O Configuration: LVTTTL 3.3V- 20mA AC Loading: 35pF Test Conditions: Typical Voltage, 25C	–	1.239	–	ns	*
sp5	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS fall time (10%-90%) 1	I/O Configuration: LVTTTL 3.3V- 20mA AC Loading: 35pF Test Conditions: Typical Voltage, 25C	–	1.245	–	ns	*
sp6	Data from master (SC_SPI_SDO) setup time	–	160	–	–	ns	–
sp7	Data from master (SC_SPI_SDO) hold time	–	160	–	–	ns	–
sp8	SC_SPI_SDI setup time	–	20	–	–	ns	–
sp9	SC_SPI_SDI hold time	–	20	–	–	ns	–
Note: *For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models . Use the supported I/O Configurations for the System Controller SPI in Table 144.							

Table 144 • Supported I/O Configurations for System Controller SPI (for MSIO Bank Only)

Voltage Supply	I/O Drive Configuration	Units
3.3 V	20	mA
2.5 V	16	mA
1.8 V	12	mA
1.5 V	8	mA
1.2 V	4	mA

Table 149 • Flash*Freeze Entry and Exit Times (continued)

Military Worst-Case conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

TFF_EXIT	Exit Time with respect to MSS PLL Lock	eNVM and MSS/HPMS PLL = ON during F*F	100	μs	1
		eNVM=ON and MSS/HPMS PLL =OFF during F*F and MSS/HPMS PLL turned back on at exit	136	μs	1
		eNVM and MSS PLL=OFF during F*F and both are turned back on at exit	200	μs	1
		eNVM=OFF and MSS PLL = ON during F*F and eNVM turned back on at exit	200	μs	1
	Exit Time with respect to Fabric PLL Lock	eNVM and MSS/HPMS PLL = ON during F*F	1.5	ms	1,2
		eNVM and MSS PLL=OFF during F*F and both are turned back on at exit	1.5	ms	1,2
	Exit Time with respect to Fabric buffer output	eNVM and MSS/HPMS PLL = ON during F*F	21	μs	1,2
		eNVM and MSS PLL=OFF during F*F and both are turned back on at exit	65	μs	1

Notes:

1. F*F entry and exit times were measured with $F_{CLK} = 100\text{ MHz}$
2. PLL Lock Delay set to 1024 cycles (default)

Table 160 • SPI Characteristics

Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Symbol	Description	Conditions	All Devices/Speed Grades			Unit	Notes
			Min	Typ	Max		
sp4	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%-90%)	IO Configuration: LVCMOS 2.5 V - 8mA AC Loading: 35pF Test Conditions: Typical Voltage, 25°C	–	2.77	–	ns	1
sp5	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%-90%)	IO Configuration: LVCMOS 2.5 V - 8mA AC Loading: 35pF Test Conditions: Typical Voltage, 25°C	–	2.90 6	–	ns	1
SPI Master Configuration							
sp6m	SPI_[0 1]_DO setup time	–	(SPI_x_CLK_period/2) – 3.0	–	–	ns	2
sp7m	SPI_[0 1]_DO hold time	–	(SPI_x_CLK_period/2) – 2.5	–	–	ns	2
sp8m	SPI_[0 1]_DI setup time	–	8	–	–	ns	2
sp9m	SPI_[0 1]_DI hold time	–	2.5	–	–	ns	2
SPI Slave Configuration							
sp6s	SPI_[0 1]_DO setup time	–	(SPI_x_CLK_period/2) – 12.0	–	–	ns	2
sp7s	SPI_[0 1]_DO hold time	–	(SPI_x_CLK_period/2) + 3.0	–	–	ns	2
sp8s	SPI_[0 1]_DI setup time	–	2	–	–	ns	2
sp9s	SPI_[0 1]_DI hold time	–	3	–	–	ns	2
Notes: 1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models . 2. For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.							

25. CAN Controller Characteristics

Table 161 • CAN Controller Characteristics
 Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Min	Typ	Max	Units	Notes
FCANREFCLK	Internally Sourced CAN Reference Clock Frequency	–	–	128	MHz	*
BAUDCAN	CAN Performance Baud Rate	0.05	–	1	Mbps	–
<i>Note: PCLK to CAN controller must be a multiple of 8 MHz.</i>						