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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	12084
Total RAM Bits	933888
Number of I/O	233
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl010ts-1fgg484m

List of Tables

IGLOO2 and SmartFusion2 SoC FPGA Military Grade AC/DC Electrical Characteristics

1. Introduction

Microsemi®'s military grade SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) and IGLOO®2 FPGA families integrate an industry standard 4-input lookup table-based (LUT) FPGA fabric with integrated mathblocks, multiple embedded memory blocks, and high-performance SERDES communications interfaces on a single chip. Both families benefit from low power flash technology and are the most secure and reliable FPGAs in the industry. These next generation devices offer up to 150K Logic Elements, up to five MB of embedded RAM, up to 16 SERDES lanes, and up to four PCI Express Gen 1 endpoints, as well as integrated hard DDR3 memory controllers with error correction.

SmartFusion2 military grade devices integrate an entire low power real time Microcontroller Subsystem with a rich set of Industry standard peripherals including Ethernet, USB, and CAN, while the IGLOO2 military devices integrate a high-performance memory subsystem with on-chip flash, 32 Kbyte embedded SRAM, and multiple DMA controllers.

2. Device Status

For more information on device status, refer to the "Datasheet Categories".

Table 1 • **IGLOO2 FPGA and SmartFusion2 SoC FPGA Device Status**

Design Security Device Densities	**Status**
010T	Production
025T	Production
050T	Production
060T	Preliminary
090T	Production
150T	Production
Data Security Device Densities	**Status**
010TS	Production
025TS	Production
050TS	Production
060TS	Preliminary
090TS	Production
150TS	Production

Table 3 • **Recommended Operating Conditions (continued)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
VPPNVM	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–

Notes:

1. *Programming at this temperature range is available only with VPP in 3.3 V Range*
2. *Power supply ramps must all be strictly monotonic, without plateaus.*

Table 4 • **FPGA Operating Limits**

Product Grade	Element	Programming Temperature	Operating Temperature	Programming Cycles	Retention (Biased/Unbiased)	Note
Military	FPGA	Min T_J = 0°C Max T_J = 85°C	Min T_J = -55°C Max T_J = 125°C	500	10 Years	–
		Min T_J = -40°C Max T_J = 100°C	Min T_J = -55°C Max T_J = 125°C	500	10 Years	*

*Note: *: Programming at this temperature range is available only with VPP in 3.3 V Range*

Table 5 • **Embedded Flash Limits**

Product Grade	Element	Programming Temperature	Maximum Operating Temperature	Programming Cycles	Retention (Biased/Unbiased)
Military	Embedded flash	Min T_J = -55°C Max T_J = 125°C	Min T_J = -55°C Max T_J = 125°C	< 10,000 cycles per pages, up to one million cycles per eNVM array	10 Years

Table 6 • **Device Storage Temperature and Retention**

Product Grade	Storage Temperature (Tstg)	Retention
Military	Min T_J = -55°C Max T_J = 125°C	10 Years

4.2 Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to -1.0 V for no longer than 10% or the period. The current during the transition must not exceed 100mA.

For AC signals, the input signal may overshoot during transitions to VCCI + 1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100mA.

Note: The above specification does not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant to the PCI standard including the PCI overshoot/undershoot specifications.

4.3. Thermal Characteristics

4.3.1 Introduction

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures.

EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

where

θ_{JA} = Junction-to-air thermal resistance
θ_{JB} = Junction-to-board thermal resistance
θ_{JC} = Junction-to-case thermal resistance
T_J = Junction temperature
T_A = Ambient temperature
T_B = Board temperature (measured 1.0 mm away from the package edge)
T_C = Case temperature
P = Total power dissipated by the device

Table 7 • **Package Thermal Resistance**

Product M2GL/M2S	θ_{JA}			θ_{JB}	θ_{JC}	Units
	Still Air	1.0 m/s	2.5 m/s			
010						
FG484	18.22	14.83	13.62	8.83	4.92	°C/W
025						
FG484	17.03	13.66	12.45	7.66	4.18	°C/W
050						
FG484	15.29	12.19	10.99	6.27	3.24	°C/W
060						
FG484	15.40	12.06	10.85	6.14	3.15	°C/W
090						
FG484	14.64	11.37	10.16	5.43	2.77	°C/W
150						
FC1152	9.08	6.81	5.87	2.56	0.38	°C/W

4.3.2 Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It must be used with caution, but it is useful for comparing the thermal performance of one package to another.

The maximum power dissipation allowed is calculated using EQ 4.

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 100°C. EQ 5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL050-FG484 package at Military temperature and in still air, where:

θ_{JA} = 15.29°C/W (taken from Table 7 on page 15)

T_A = 85°C

$$\text{Maximum Power Allowed} = \frac{100°C - 85°C}{15.29°C/W} = 0.981\ W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

4.3.3 Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

4.3.4 Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition.

This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

Table 13 • **Inrush Currents at Power up, –55°C <= T_J <=125°C, Typical Process**

VDDI	2.62	141	161	187	283	404	mA
Number of banks		8	8	10	9	19	–

6. Average Fabric Temperature and Voltage Derating Factors

Table 14 • **Average Temperature and Voltage Derating Factors for Fabric Timing Delays**
(Normalized to T_J = 125°C, Worst-Case VDD = 1.14 V)

Core Voltage VDD (V)	Junction Temperature (°C)							
	–55°C	–40°C	0°C	25°C	70°C	85°C	100°C	125°C
1.14	0.91	0.91	0.93	0.94	0.96	0.97	0.98	1.00
1.2	0.82	0.83	0.84	0.85	0.87	0.87	0.88	0.90
1.26	0.75	0.75	0.77	0.77	0.79	0.80	0.81	0.75

Table 39 • **LVCMOS 1.8 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
Worst-case Military conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.71 V (continued)

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
12 mA	slow	3.795	3.096	3.773	6.773	6.067	ns
	medium	3.408	2.764	3.389	6.47	5.743	ns
	medium_fast	3.215	2.599	3.194	6.346	5.61	ns
	fast	3.196	2.584	3.175	6.335	5.604	ns
16 mA	slow	3.744	3.035	3.719	6.944	6.207	ns
	medium	3.358	2.712	3.339	6.657	5.868	ns
	medium_fast	3.175	2.546	3.153	6.547	5.751	ns
	fast	3.156	2.531	3.133	6.541	5.747	ns
LVCMOS 1.8 V (for MSIO I/O Bank)							
2 mA	slow	3.957	4.784	5.023	5.643	5.866	ns
4 mA	slow	3.668	4.162	4.485	6.543	6.382	ns
6 mA	slow	3.586	3.994	4.358	7.622	6.941	ns
8 mA	slow	3.616	3.782	4.162	7.988	7.161	ns
10 mA	slow	3.662	3.732	4.121	8.396	7.423	ns
12 mA	slow	3.75	3.615	4.006	8.576	7.543	ns
LVCMOS 1.8 V (for MSIOD I/O Bank)							
2 mA	slow	3.048	3.692	3.898	5.818	5.609	ns
4 mA	slow	2.5	3.088	3.288	6.421	6.121	ns
6 mA	slow	2.225	2.747	2.937	7.18	6.753	ns
8 mA	slow	2.233	2.72	2.904	7.49	6.992	ns
10 mA	slow	2.263	2.577	2.759	7.851	7.253	ns

8.6.5 1.5 V LVCMOS

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-11A.

8.6.5.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 40 • **LVCMOS 1.5 V Minimum and Maximum DC Input and Output Levels**

Symbols	Parameters	Min	Typ	Max	Units
LVCMOS 1.5 V Recommended DC Operating Conditions					
VDDI	Supply voltage	1.425	1.5	1.575	V
LVCMOS 1.5 V DC Input Voltage Specification					
VIH (DC)	DC input logic High for (MSIOD and DDRIO I/O banks)	0.65 × VDDI	–	1.575	V
VIH (DC)	DC input logic High (for MSIO I/O Bank)	0.65 × VDDI	–	2.75	V
VIL (DC)	DC input logic Low	–0.3	–	0.35 × VDDI	V
IIH (DC)	Input current High	–	–	10	µA
IIL (DC	Input current Low	–	–	10	µA
LVCMOS 1.5 V DC Output Voltage Specification					
VOH	DC output logic High	VDDI × 0.75	–	–	V
VOL	DC output logic Low	–	–	VDDI × 0.25	V

8.7.5.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 70 • DDR3/STTL15 AC Switching Characteristics for Receiver (Input Buffers)
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.425 V

		Speed Grade –1	
	ODT (On Die Termination)	t_{PY}	Units
DDR3/SSTL15 (for DDRIO I/O Bank) – Calibration Mode Only			
Pseudo-Differential	None	1.672	ns
True-Differential	None	1.694	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 71 • DDR3/SSTL15 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.425 V

	Speed Grade –1					
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	Units
DDR3 Reduced Drive/SSTL15 Class I (for DDRIO I/O Bank)						
Single Ended	2.832	2.766	2.767	2.658	2.659	ns
Differential	2.848	3.401	3.393	3.173	3.166	ns
DDR3 Full Drive/SSTL15 Class II (for DDRIO I/O Bank)						
Single Ended	2.832	2.76	2.759	2.655	2.655	ns
Differential	2.845	3.397	3.387	3.179	3.171	ns

8.7.6 Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer. This I/O standard is supported in DDRIO I/O Bank only.

8.7.6.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 72 • LPDDR AC/DC Specifications (for DDRIO IO Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.71	1.8	1.89	V	–
VTT	Termination voltage		0.838	0.900	0.964	V	–
VREF	Input reference voltage		0.838	0.900	0.964	V	–
LPDDR DC Input Voltage Specification							
VIH (DC)	DC input logic High		0.7 × VDDI	–	1.89	V	–
VIL (DC)	DC input logic Low		–0.3	–	0.3 × VDDI	V	–
IIH (DC)	Input current High		–	–	10	µA	–
IIL (DC)	Input current Low		–	–	10	µA	–
LPDDR DC Output Voltage Specification							

8.8.5 RSDS

Reduced Swing Differential Signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS devices and is only intended for point-to-point applications.

8.8.5.1 Minimum and Maximum Input and Output Levels

Table 101 • **RSDS DC Voltage Specification**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
VDDI	Supply voltage		2.375	2.5	2.625	V
RSDS DC Input Voltage Specification						
VI	DC input voltage		0	–	2.925	V
RSDS DC Output Voltage Specification						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
RSDS Differential Voltage Specification						
VOD	Differential output voltage swing		100	–	600	mV
VOCM	Output common mode voltage		0.5	–	1.5	V
VICM	Input common mode voltage		0.3	–	1.5	V
VID	Input differential voltage		100	–	600	mV

Table 102 • **RSDS AC Specifications**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
RSDS Maximum AC Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	460	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 10 pF / 100 Ω differential load	–	–	480	Mbps
RSDS Impedance Specification						
Rt	Termination resistance		–	100	–	Ω
RSDS AC Test Parameters Specifications						
VTrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF

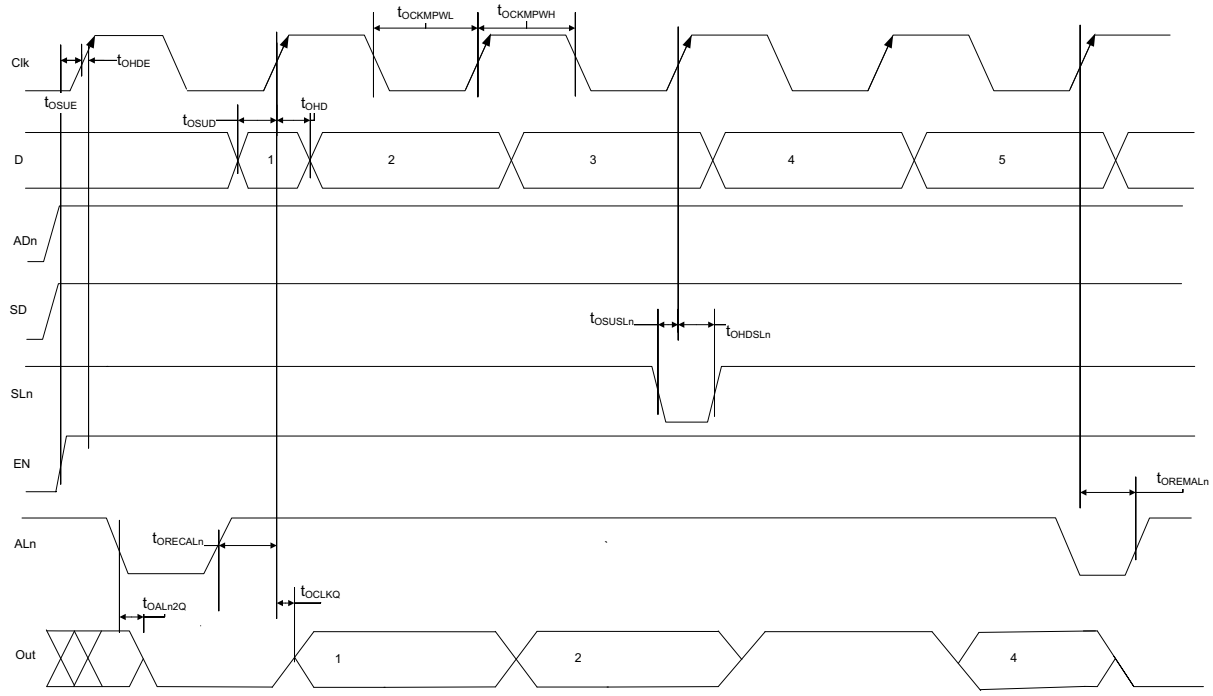

***Figure 8* • I/O Register Output Timing Diagram**

***Table 109* • Output/Enable Data Register Propagation Delays**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Measuring Nodes (from, to)*	Speed Grade –1	Units
tOBYP	Bypass Delay of the Output/Enable Register	F,G or H,I	0.364	ns
tOCLKQ	Clock-to-Q of the Output/Enable Register	E,G or E,I	0.272	ns
tOSUD	Data Setup Time for the Output/Enable Register	A,E or J,E	0.196	ns
tOHD	Data Hold Time for the Output/Enable Register	A,E or J,E	0	ns
tOSUE	Enable Setup Time for the Output/Enable Register	B,E	0.433	ns
tOHE	Enable Hold Time for the Output/Enable Register	B,E	0	ns
tOSUSL	Synchronous Load Setup Time for the Output/Enable Register	D,E	0.203	ns
tOHSL	Synchronous Load Hold Time for the Output/Enable Register	D,E	0	ns
tOALn2Q	Asynchronous Clear-to-Q of the Output/Enable Register (ADn=1)	C,G or C,I	0.523	ns
	Asynchronous Preset-to-Q of the Output/Enable Register (ADn=0)	C,G or C,I	0.545	ns
tOREMALn	Asynchronous Load Removal Time for the Output/Enable Register	C,E	0	ns

8.10.2 Input DDR Timing Diagram

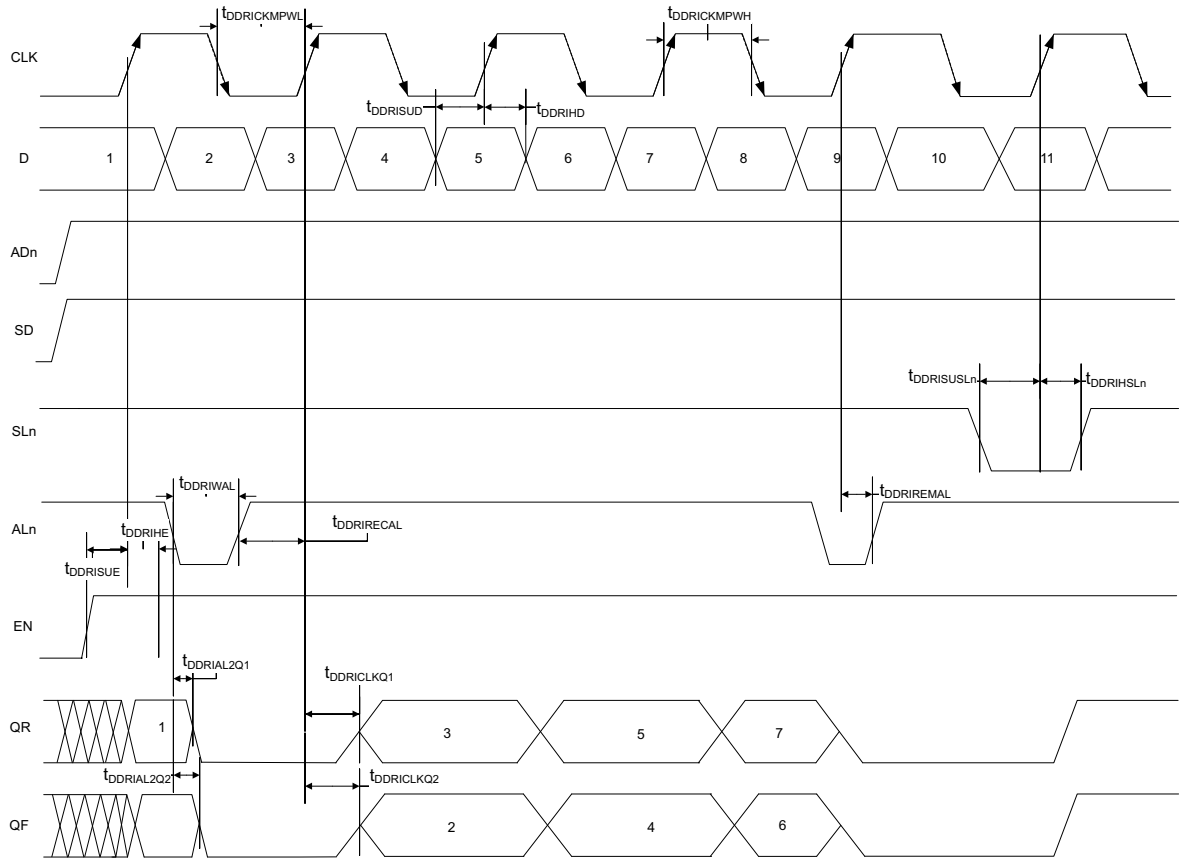

***Figure 10* • Input DDR Timing Diagram**

8.10.3 Timing Characteristics

Table 110 • Input DDR Propagation Delays
Worst-Case Military Conditions: T_J = 125°C, VDD=1.14 V

Parameter	Description	Measuring Nodes (from, to)	Speed Grade –1	Units
tDDRICLKQ1	Clock-to-Out Out_QR for Input DDR	B,C	0.165	ns
tDDRICLKQ2	Clock-to-Out Out_QF for Input DDR	B,D	0.172	ns
tDDRISUD	Data Setup for Input DDR	A,B	0.372	ns
tDDRIHD	Data Hold for Input DDR	A,B	0	ns
tDDRISUE	Enable Setup for Input DDR	E,B	0.475	ns
tDDRIHE	Enable Hold for Input DDR	E,B	0	ns
tDDRISUSLn	Synchronous Load Setup for Input DDR	G,B	0.475	ns
tDDRIHSLn	Synchronous Load Hold for Input DDR	G,B	0	ns
tDDRIAL2Q1	Asynchronous Load-to-Out QR for Input DDR	F,C	0.606	ns
tDDRIAL2Q2	Asynchronous Load-to-Out QF for Input DDR	F,D	0.558	ns
tDDRIREMAL	Asynchronous Load Removal time for Input DDR	F,B	0	ns
tDDRIRECAL	Asynchronous Load Recovery time for Input DDR	F,B	0.076	ns
tDDRIWAL	Asynchronous Load Minimum Pulse Width for Input DDR	F,F	0.313	ns
tDDRICKMPWH	Clock Minimum Pulse Width High for Input DDR	B,B	0.078	ns
tDDRICKMPWL	Clock Minimum Pulse Width Low for Input DDR	B,B	0.164	ns

9. Logic Element Specifications

9.1 4-input LUT (LUT-4)

The IGLOO2 and SmartFusion2 SoC FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *SmartFusion2 and IGLOO2 Macro Library Guide*.

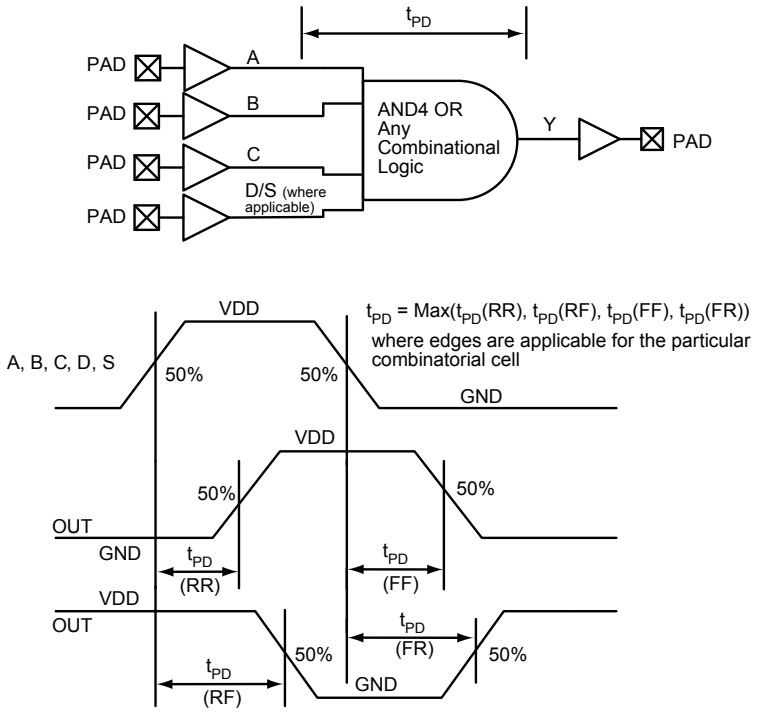

Figure 13 • **LUT-4**

Timing Characteristics

Table 112 • **Combinatorial Cell Propagation Delays**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Combinatorial Cell	Equation	Parameter	Speed Grade –1	Units
INV	Y = !A	t_{PD}	0.106	ns
AND2	Y = A · B	t_{PD}	0.17	ns
NAND2	Y = !(A · B)	t_{PD}	0.157	ns
OR2	Y = A + B	t_{PD}	0.17	ns
NOR2	Y = !(A + B)	t_{PD}	0.157	ns
XOR2	Y = A ⊕ B	t_{PD}	0.17	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.236	ns
AND3	Y = A · B · C	t_{PD}	0.217	ns
AND4	Y = A · B · C · D	t_{PD}	0.384	ns

11. FPGA Fabric SRAM

Refer to the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for more information.

11.1 FPGA Fabric Large SRAM (LSRAM)

Table 119 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1Kx18**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tcy	Clock Period	3.333	–	ns
tclkmpwh	Clock Minimum Pulse Width High	1.5	–	ns
tclkmpwl	Clock Minimum pulse Width Low	1.5	–	ns
tplcy	Pipelined Clock Period	3.333	–	ns
tplclkmpwh	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
tplclkmpwl	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.346	ns
	Read Access Time without Pipeline Register	–	2.346	ns
	Access Time with Feed-Through Write Timing	–	1.578	ns
taddrsu	Address Setup Time	0.455	–	ns
taddrhd	Address Hold Time	0.282	–	ns
tdsu	Data Setup Time	0.352	–	ns
tdhd	Data Hold Time	0.11	–	ns
tblksu	Block Select Setup Time	0.214	–	ns
tblkhd	Block Select Hold Time	0.223	–	ns
tblk2q	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	1.578	ns
tblkmpw	Block Select Minimum Pulse Width	0.218	–	ns
trdesu	Read Enable Setup Time	0.463	–	ns
trdehd	Read Enable Hold Time	0.173	–	ns
trdplesu	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
trdplehd	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
tr2q	Asynchronous Reset to Output Propagation Delay	–	1.561	ns
trstrem	Asynchronous Reset Removal Time	0.522	–	ns
trstrec	Asynchronous Reset Recovery Time	0.005	–	ns
trstmpw	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
tplrstrem	Pipelined Register Asynchronous Reset Removal Time	-0.288	–	ns
tplrstrec	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
tplrstmpw	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns

Table 120 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2Kx9**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
trstrem	Asynchronous Reset Removal Time	0.522	–	ns
trstrec	Asynchronous Reset Recovery Time	0.005	–	ns
trstmpw	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
tplrstrem	Pipelined Register Asynchronous Reset Removal Time	-0.288	–	ns
tplrstrec	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
tplrstmpw	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
tsrstsu	Synchronous Reset Setup Time	0.233	–	ns
tsrsthd	Synchronous Reset Hold Time	0.037	–	ns
twesu	Write Enable Setup Time	0.428	–	ns
twehd	Write Enable Hold Time	0.05	–	ns
Fmax	Maximum Frequency	–	300	MHz

Table 121 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4Kx4**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		
		Min	Max	Units
tcy	Clock Period	3.333	–	ns
tclkmpwh	Clock Minimum Pulse Width High	1.5	–	ns
tclkmpwl	Clock Minimum pulse Width Low	1.5	–	ns
tplcy	Pipelined Clock Period	3.333	–	ns
tplclkmpwh	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
tplclkmpwl	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.334	ns
	Read Access Time without Pipeline Register	–	2.346	ns
	Access Time with Feed-Through Write Timing	–	1.56	ns
taddrsu	Address Setup Time	0.56	–	ns
taddrhd	Address Hold Time	0.282	–	ns
tdsu	Data Setup Time	0.345	–	ns
tdhd	Data Hold Time	0.084	–	ns
tblksu	Block Select Setup Time	0.214	–	ns
tblkhd	Block Select Hold Time	0.223	–	ns
tblk2q	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	1.56	ns
tblkmpw	Block Select Minimum Pulse Width	0.218	–	ns

Table 126 • **uSRAM (RAM64x16) in 64x16 Mode**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
trdenhd	Read Enable Hold Time	0.059	–	ns
tblksu	Read Block Select Setup Time	1.898	–	ns
tblkhd	Read Block Select Hold Time	-0.671	–	ns
tblk2q	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.102	ns
trstrem	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
trstrec	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
tr2q	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.866	ns
tsrstsu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.062		ns
tccy	Write Clock Period	4	–	ns
tcclkmpwh	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclkmpwl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblkcsu	Write Block Setup Time	0.417	–	ns
tblkchd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.119	–	ns
tdinchd	Write Input Data hold Time	0.155	–	ns
taddrcsu	Write Address Setup Time	0.091	–	ns
taddrchd	Write Address Hold Time	0.132	–	ns
twecsu	Write Enable Setup Time	0.41	–	ns
twechd	Write Enable Hold Time	-0.027	–	ns
fmax	Maximum Frequency	–	250	MHz

Table 127 • **uSRAM (RAM128x9) in 128x9 Mode**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tcy	Read Clock Period	4	–	ns
tclkmpwh	Read Clock Minimum Pulse Width High	1.8	–	ns

Table 140 • **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Conditions/Package Combinations					Units	Notes
CCC Output Peak-to-Peak Period Jitter fOUT_CCC							
010, 050 FG484 Packages	SSO = 0	0 < SSO <= 2	SSO <= 4	SSO <= 8	SSO <= 16	–	*
20 MHz to 100 MHz	Max(110, ± 1% x (1/fOUT_CCC))	Max(150, ± 1% x (1/fOUT_CCC))				ps	–
100 MHz to 400 MHz	120	150			170	ps	–
025 FG484 Package	0 < SSO <=16						*
20 MHz to 74 MHz	± 1% x (1/fOUT_CCC)					ps	–
74 MHz to 400 MHz	210					ps	–
090 FG484 and 150 FC1152 Packages	0 < SSO <=16						*
20 MHz to 100 MHz	± 1% x (1/fOUT_CCC)					ps	–
100 MHz to 400 MHz	150					ps	–
*Note: *SSO Data is based on LVCMOS 2.5 V MSIO and/or MSIOD Bank I/Os.*							

16. JTAG

Table 141 • **JTAG 1532**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	-1 Speed Grade					Units
		010	025	050	090	150	
tTCK2Q	Clock to Q (data out)	7.91	7.95	8.15	9.21	8.85	ns
tRSTB2Q	Reset to Q (data out)	6.54	6.27	7.54	7.94	8.99	ns
tDISU	Test Data Input Setup Time	-0.70	-0.70	-0.31	-1.33	-1.02	ns
tDIHD	Test Data Input Hold Time	2.38	2.47	2.13	2.71	2.59	ns
tTMSSU	Test Mode Select Setup Time	-0.86	-1.13	0.26	-1.03	-0.56	ns
tTMDHD	Test Mode Select Hold Time	1.48	1.98	0.21	1.69	1.05	ns
tTRSTREM	ResetB Removal Time	-1.1	-1.38	-0.49	-0.8	-1.07	ns
tTRSTREC	ResetB Recovery Time	-1.1	-1.38	-0.47	-0.8	-1.07	ns
FTCKMAX	TCK Maximum frequency	25	25	25	25	25	MHz

24.3 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to Figure 17 on page 115.

Table 160 • **SPI Characteristics**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Symbol	Description	Conditions	All Devices/Speed Grades			Unit	Notes
			Min	Typ	Max		
sp1	**SPI_[0|1]_CLK minimum period**						
	SPI_[0|1]_CLK = PCLK/2	–	12	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/4	–	24.1	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/8	–	48.2	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/16	–	0.1	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/32	–	0.19	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/64	–	0.39	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/128	–	0.77	–	–	µs	–
sp2	**SPI_[0|1]_CLK minimum pulse width high**						
	SPI_[0|1]_CLK = PCLK/2	–	6	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/4	–	12.05	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/8	–	24.1	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/16	–	0.05	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/32	–	0.095	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/64	–	0.195	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/128	–	0.385	–	–	µs	–
sp3	**SPI_[0|1]_CLK minimum pulse width low**						
	SPI_[0|1]_CLK = PCLK/2	–	6	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/4	–	12.05	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/8	–	24.1	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/16	–	0.05	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/32	–	0.095	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/64	–	0.195	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/128	–	0.385	–	–	µs	–

Notes:

1. *For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.*

Datasheet Information

List of Changes

The following table shows important changes made in this document for each revision.

Revision	Changes	Page
Revision 4 (September 2015)	Updated Table 9: "SmartFusion2 and IGLOO2 Quiescent Supply Current – Typical Process" for typical process values (SAR 69218).	17
	Updated Table 10: "SmartFusion2 and IGLOO2 Quiescent Supply Current – Worst-Case Process" for worst process values (SAR 69218).	18
	Updated Table 140: "IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications" for FG484 package (SAR 69804).	101
Revision 3 (June 2015)	Updated Table 1: "IGLOO2 FPGA and SmartFusion2 SoC FPGA Device Status" (SAR 68620).	10
Revision 2 (June 2015)	Updated Table 1: "IGLOO2 FPGA and SmartFusion2 SoC FPGA Device Status"	10
	Updated Table 3: "Recommended Operating Conditions"	12
	Updated Table 4: "FPGA Operating Limits" (SAR 63109).	14
	Updated Table 7: "Package Thermal Resistance"	15
	Updated Table 65: "DDR2/SSTL18 AC Specifications (Applicable to DDRIO Bank Only)" and Table 69: "DDR3/SSTL15 AC Specifications" (SAR 67210).	49, 51
	Added "Embedded NVM (eNVM) Characteristics" (SAR 52509).	97
	Updated Table 139: "IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification" (SAR 65958, SAR 62012, and SAR 56666).	100
	Updated Table 141: "JTAG 1532"	101
	Added "DEVRST_N Characteristics " (SAR 64100).	102
	Added "DDR Memory Interface Characteristics" (SAR 66223).	107
	Added "SFP Transceiver Characteristics" (SAR 63105).	108
	Added "CAN Controller Characteristics" (SAR 50424).	116
	Added "USB Characteristics" (SAR 50424).	117
	Updated Table 157: "Maximum Frequency for MSS Main Clock" and Table 163: "Maximum Frequency for HPMS Main Clock" (SAR 66314).	110, 118
Revision 1 (December 2014)	Initial release.	NA