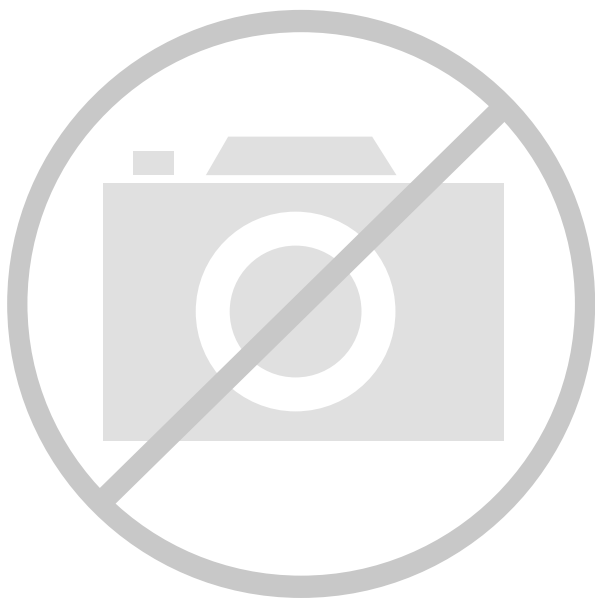




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	27696
Total RAM Bits	1130496
Number of I/O	267
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl025t-1fgg484m

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3. Product Briefs and Pin Descriptions

The product brief and pin descriptions are published separately:

- PB0121: IGLOO2 Product Brief
- DS0124: IGLOO2 Pin Descriptions
- PB0115: SmartFusion2 SoC FPGA Product Brief
- DS0115: SmartFusion2 Pin Descriptions

4. General Specifications

4.1 Operating Conditions

Stresses beyond those listed in Table 2 may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in Table 2 is not implied.

Table 2 • Absolute Maximum Ratings

Symbol	Parameter	Limits		Units	Notes
		Min	Max		
VDD	DC core supply voltage. Must always power this pin.	−0.3	1.32	V	–
VPP	Power supply for charge pumps (for normal operation and programming). Must always power this pin.	−0.3	3.63	V	–
MSS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	−0.3	3.63	V	–
HPMS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	−0.3	3.63	V	–
FDDR_PLL_VDDA	Analog power pad for FDDR PLL	−0.3	3.63	V	–
PLL0_PLL1_MSS_MDDR_VDDA	Analog power pad for MDDR PLL	−0.3	3.63	V	–
PLL0_PLL1_HPMS_MDDR_VDDA	Analog power pad for MDDR PLL	−0.3	3.63	V	–
CCC_XX[01]_PLL_VDDA	Analog power pad for PLL0–5	−0.3	3.63	V	–
SERDES_[01]_PLL_VDDA	High supply voltage for PLL SERDES[01]	−0.3	3.63	V	–
SERDES_[01]_L[0123]_VDDAPLL	Analog power for SERDES[01] PLL lane0 to lane3. This is a +2.5 V SERDES internal PLL supply.	−0.3	2.75	V	–
SERDES_[01]_L[0123]_VDDAIO	TX/RX analog I/O voltage. Low voltage power for the lanes of SERDESIF0. This is a +1.2 V SERDES PMA supply.	−0.3	1.32	V	–
SERDES_[01]_VDD	PCIe®/PCS power supply	−0.3	1.32	V	–
VDDIx	DC FPGA I/O buffer supply voltage for MSIO I/O Bank	−0.3	3.63	V	–
	DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O Banks	−0.3	2.75	V	–
VI	I/O Input voltage for MSIO I/O Bank	−0.3	3.63	V	–
	I/O Input voltage for MSIOD/DDRIO I/O Bank	−0.3	2.75	V	–
VPPNVM	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP.	−0.3	3.63	V	–

8.2. Output Buffer and AC Loading

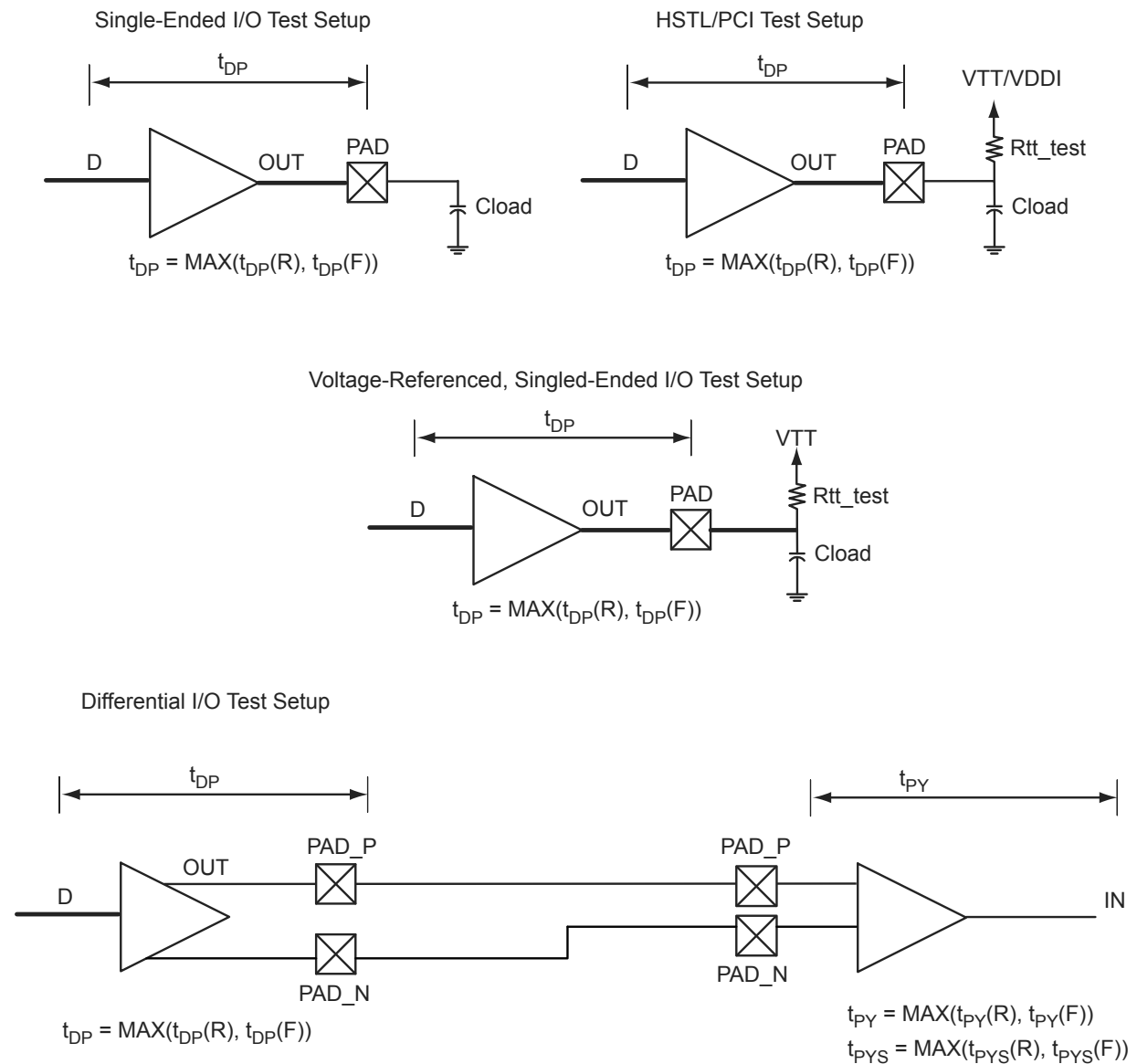


Figure 3 • Output Buffer AC Loading

8.6.3 2.5 V LVCMOS

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in IGLOO2 FPGA and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-5A.

8.6.3.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 27 • LVCMOS 2.5 V DC Voltage Specification

Symbol	Parameters	Conditions	Min	Typ	Max	Units	Notes
LVCMOS 2.5 V Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	–
LVCMOS 2.5 V DC Input Voltage Specification							
VIH (DC)	DC input logic High (for MSIOD and DDRIO I/O Bank)		1.7	–	2.625	V	–
VIH (DC)	DC input logic High (for MSIO I/O Bank)		1.7	–	2.75	V	–
VIL (DC)	DC input logic Low		–0.3	–	0.7	V	–
IIH (DC)	Input current High		–	–	10	μA	–
IIL (DC)	Input current Low		–	–	10	μA	–
LVCMOS 2.5 V DC Output Voltage Specification							
VOH	DC output logic High		1.7	–	–	V	*
VOL	DC output logic Low		–	–	0.7	V	*
Note: * The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.							

Table 28 • LVCMOS 2.5 V Maximum AC Switching Speeds

Symbol	Parameters	Conditions	Min	Typ	Max	Units
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	360	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	360	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	370	Mbps

Table 29 • LVCMOS 2.5 V AC Test Parameters and Driver Impedance Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 2.5 V Calibrated Impedance Option						
Rodt_cal	Supported output driver calibrated impedance (for DDRIO I/O Bank)	–	–	75, 60, 50, 33, 25, 20	–	Ω
LVCMOS 2.5 V AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path	–	–	1.2	–	V
Rent	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})	–	–	2k	–	Ω
Cent	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})	–	–	5	–	pF
Cload	Capacitive loading for data path (t _{DP})	–	–	5	–	pF

Table 32 • LVCMOS 2.5 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-case Military conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$ (continued)

Output Drive Selection	Slew Control	Speed Grade -1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
6 mA	slow	3.189	2.716	3.169	5.56	5.092	ns
	medium	2.886	2.473	2.876	5.273	4.752	ns
	medium_fast	2.749	2.355	2.738	5.127	4.167	ns
	fast	2.731	2.345	2.72	5.115	4.6	ns
8 mA	slow	3.132	2.646	3.109	5.686	5.207	ns
	medium	2.832	2.407	2.82	5.402	4.864	ns
	medium_fast	2.698	2.292	2.685	5.262	4.732	ns
	fast	2.684	2.282	2.671	5.252	4.724	ns
12 mA	slow	3.013	2.504	2.984	5.918	5.416	ns
	medium	2.72	2.284	2.707	5.657	5.074	ns
	medium_fast	2.592	2.176	2.578	5.537	4.949	ns
	fast	2.58	2.166	2.566	5.529	4.946	ns
16 mA	slow	2.936	2.415	2.902	6.136	5.577	ns
	medium	2.66	2.206	2.645	5.901	5.261	ns
	medium_fast	2.536	2.102	2.519	5.815	5.142	ns
	fast	2.523	2.093	2.506	5.81	5.137	ns
LVCMOS 2.5 V (for MSIO I/O Bank)							
2 mA	slow	3.933	4.352	4.22	2.358	3.838	ns
4 mA	slow	2.905	3.423	3.508	4.681	5.262	ns
6 mA	slow	2.687	2.995	3.155	5.561	5.73	ns
8 mA	slow	2.594	2.877	3.07	6.602	6.248	ns
12 mA	slow	2.623	2.732	2.944	6.974	6.478	ns
16 mA	slow	2.717	2.617	2.84	7.455	6.824	ns
LVCMOS 2.5 V (for MSIOD I/O Bank)							
2 mA	slow	2.403	2.922	2.89	5.397	5.202	ns
4 mA	slow	1.998	2.446	2.468	5.936	5.665	ns
6 mA	slow	1.861	2.329	2.375	6.391	6.068	ns
8 mA	slow	1.781	2.145	2.208	6.884	6.44	ns
12 mA	slow	1.804	2.039	2.108	7.23	6.685	ns

Table 36 • LVC MOS 1.8 V Transmitter Drive Strength Specifications

Output Drive Selection	VOH (V)	VOL (V)			
DDRIO Bank*	Min	Max	IOH (at VOH) mA	IOL (at VOL) mA	Notes
2 mA	VDDI – 0.45	0.45	2	2	–
4 mA	VDDI – 0.45	0.45	4	4	–
6 mA	VDDI – 0.45	0.45	6	6	**
8 mA	VDDI – 0.45	0.45	6	6	**
10 mA	VDDI – 0.45	0.45	8	8	–
12 mA	VDDI – 0.45	0.45	10	10	–
16 mA	VDDI – 0.45	0.45	12	12	–
Notes: * Software Configurator GUI will display the Commercial/Industrial numeric values. The actual drive capability at temperature is defined by Table 36. ** DDRIO has two 6mA drive strength settings. The setting that corresponds to Output Drive Selection value of 8mA has a shorter propagation delay.					

Table 37 • LVC MOS 1.8 V AC Test Parameters and Driver Impedance Specifications

LVC MOS 1.8 V AC Calibrated Impedance Option					
Symbols	Parameters	Min	Typ	Max	Units
Rodt_cal	Supported output driver calibrated impedance (for DDRIO I/O Bank)	–	75, 60, 50, 33, 25, 20	–	Ω
LVC MOS 1.8 V AC Test Parameters Specifications					
Vtrip	Measuring/trip point for data path	–	0.9	–	V
Rent	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})	–	2k	–	Ω
Cent	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})	–	5	–	pF
Cload	Capacitive loading for data path (t _{DP})	–	5	–	pF

8.6.5.2. AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 44 • LVCMOS 1.5 V AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Military Conditions: $T_J=125^{\circ}\text{C}$, $V_{DD}=1.14\text{ V}$, $V_{DDI}=1.425\text{ V}$

	ODT (On Die Termination)	Speed Grade -1		Units
		t_{PV}	t_{PVS}	
LVCMOS 1.5 V (for DDRIO I/O Bank with Fixed Codes)	none	2.19	2.216	ns
LVCMOS 1.5 V (for MSIO I/O Bank)	none	3.679	3.652	ns
	50	4.151	4.126	ns
	75	3.984	3.953	ns
	150	3.823	3.791	ns
LVCMOS 1.5 V (for MSIOD I/O Bank)	none	3.262	3.229	ns
	50	3.76	3.739	ns
	75	3.555	3.52	ns
	150	3.395	3.359	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 45 • LVCMOS 1.5 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-Case Military Conditions: $T_J=125^{\circ}\text{C}$, $V_{DD}=1.14\text{ V}$, $V_{DDI}=1.425\text{ V}$

Output Drive Selection	Slew Control	Speed Grade -1					Units
		t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
LVCMOS 1.5 V (for DDRIO I/O Bank with Fixed Codes)							
2 mA	slow	5.712	4.796	5.735	5.814	5.138	ns
	medium	5.094	4.274	5.114	5.484	4.779	ns
	medium_fast	4.793	4.013	4.81	5.288	4.625	ns
	fast	4.762	3.98	4.78	5.261	4.615	ns
4 mA	slow	4.966	4.133	4.956	6.763	6.05	ns
	medium	4.412	3.62	4.401	6.433	5.664	ns
	medium_fast	4.145	3.358	4.131	6.249	5.507	ns
	fast	4.116	3.338	4.103	6.238	5.498	ns
6 mA	slow	4.744	3.869	4.728	7.173	6.383	ns
	medium	4.212	3.382	4.195	6.837	6.004	ns
	medium_fast	3.951	3.135	3.93	6.668	5.861	ns
	fast	3.919	3.11	3.899	6.644	5.845	ns

Table 51 • LVCMOS 1.2 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Military Conditions: $T_J=125^{\circ}\text{C}$, $V_{DD}=1.14\text{ V}$, $V_{DDI}=1.14\text{ V}$ (continued)

Output Drive Selection	Slew Control	Speed Grade -1					Units
		t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
LVCMOS 1.2 V (for MSIOD I/O Bank)							
2 mA	slow	4.048	5.123	5.552	8.401	7.824	ns
4 mA	slow	3.941	4.406	4.814	9.422	8.656	ns

8.6.7 3.3 V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3 V standards specify support for 33 MHz and 66 MHz PCI bus applications.

8.6.7.1 Minimum and Maximum Input and Output Levels Specification

Table 52 • PCI/PCI-X DC Voltage Specification (Applicable to MSIO Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
PCI/PCIX Recommended DC Operating Conditions						
V_{DDI}	Supply voltage		3.15	3.3	3.45	V
PCI/PCIX DC Input Voltage Specification						
V_I	DC input voltage		0	—	3.45	V
$I_{IH}(\text{DC})$	Input current High		—	—	10	μA
$I_{IL}(\text{DC})$	Input current Low		—	—	10	μA
PCI/PCIX DC Output Voltage Specification						
V_{OH}	DC output logic High		Per PCI Specification			V
V_{OL}	DC output logic Low		Per PCI Specification			V

Table 53 • PCI/PCI-X AC Specifications (Applicable to MSIO Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
PCI/PCI-X AC Specifications						
D_{max}	Maximum data rate (MSIO I/O Bank)	AC Loading: per JEDEC specifications	—	—	560	Mbps
PCI/PCI-X AC Test Parameters Specifications						
V_{trip}	Measuring/trip point for data path (falling edge)		—	$0.615 \times V_{DDI}$	—	V
V_{trip}	Measuring/trip point for data path (rising edge)		—	$0.285 \times V_{DDI}$	—	V
R_{tt_test}	Resistance for data test path		—	25	—	Ω
R_{ent}	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		—	2k	—	Ω
C_{ent}	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		—	5	—	pF
C_{load}	Capacitive loading for data path (t_{DP})		—	10	—	pF

Table 68 • DDR3 SSTL15 DC Voltage Specification (for DDRIO I/O Bank Only) (continued)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
SSTL15 DC Output Voltage Specification						
DDR3/SSTL15 Class I (DDR3 Reduced Drive)						
VOH	DC output logic High		0.8 x VDDI	–	–	V
VOL	DC output logic Low		–	–	0.2 x VDDI	V
IOH at VOH	Output minimum source DC current		6.5	–	–	mA
IOL at VOL	Output minimum sink current		–6.5	–	–	mA
SSTL15 Class II (DDR3 Full Drive)						
VOH	DC output logic High		0.8 x VDDI	–	–	V
VOL	DC output logic Low		–	–	0.2 x VDDI	V
IOH at VOH	Output minimum source DC current		7.6	–	–	mA
IOL at VOL	Output minimum sink current		–7.6	–	–	mA
SSTL15 Differential Voltage Specification						
VID	DC input differential voltage		0.2	–	–	V
Note: *To meet JEDEC Electrical Compliance, use DDR3 Full Drive Transmitter.						

Table 69 • DDR3/SSTL15 AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
SSTL15 AC Differential Voltage Specification						
VDIFF	AC input differential voltage		0.3	–	–	V
Vx	AC differential cross point voltage		0.5 x VDDI – 0.150	–	0.5 x VDDI + 0.150	V
SSTL15 Maximum AC Switching Speed (for DDRIO I/O Banks Only)						
Dmax	Maximum data rate	AC loading: per JEDEC specifications	–	–	600	Mbps
SSTL15 AC Calibrated Impedance Option						
Rref	Supported output driver calibrated impedance	Reference resistor = 240 Ω	–	34, 40	–	Ω
RTT	Effective impedance value (ODT)	Reference resistor = 240 Ω	–	20, 30, 40, 60, 120	–	Ω
SSTL15 AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	0.75	–	V
Rent	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF
Rtt_test	Reference resistance for data test path for SSTL15 Class I (t _{DP})		–	50	–	Ω
Rtt_test	Reference resistance for data test path for SSTL15 Class II (t _{DP})		–	25	–	Ω
Cload	Capacitive loading for data path (t _{DP})		–	5	–	pF

8.8.1.2 LVDS25 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 85 • LVDS25 Receiver Characteristics

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	On-Die Termination (ODT)	Speed Grade -1	Units
		t_{PY}	
LVDS (for MSIO I/O Bank)	None	3.061	ns
	100	3.057	ns
LVDS (for MSIOD I/O Bank)	None	2.792	ns
	100	2.787	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 86 • LVDS25 Transmitter Characteristics

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	Speed Grade -1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVDS (for MSIO I/O Bank)	2.299	2.602	2.589	2.305	2.32	ns
LVDS (for MSIOD I/O Bank)						
No pre-emphasis	1.656	1.845	1.838	1.992	1.969	ns
Min pre-emphasis	1.583	1.868	1.866	2.018	1.998	ns
Med pre-emphasis	1.559	1.893	1.886	2.045	2.021	ns

8.8.1.3 LVDS33 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 87 • LVDS33 Receiver Characteristics

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 3.15\text{ V}$

	On Die Termination (ODT)	Speed Grade -1	Units
		t_{PY}	
LVDS33 (for MSIO I/O Bank)	None	2.763	ns
	100	2.76	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 88 • LVDS33 Transmitter Characteristics

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 3.15\text{ V}$

	Speed Grade -1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVDS33 (for MSIO I/O Bank)	2.069	2.112	2.106	2.078	2.09	ns

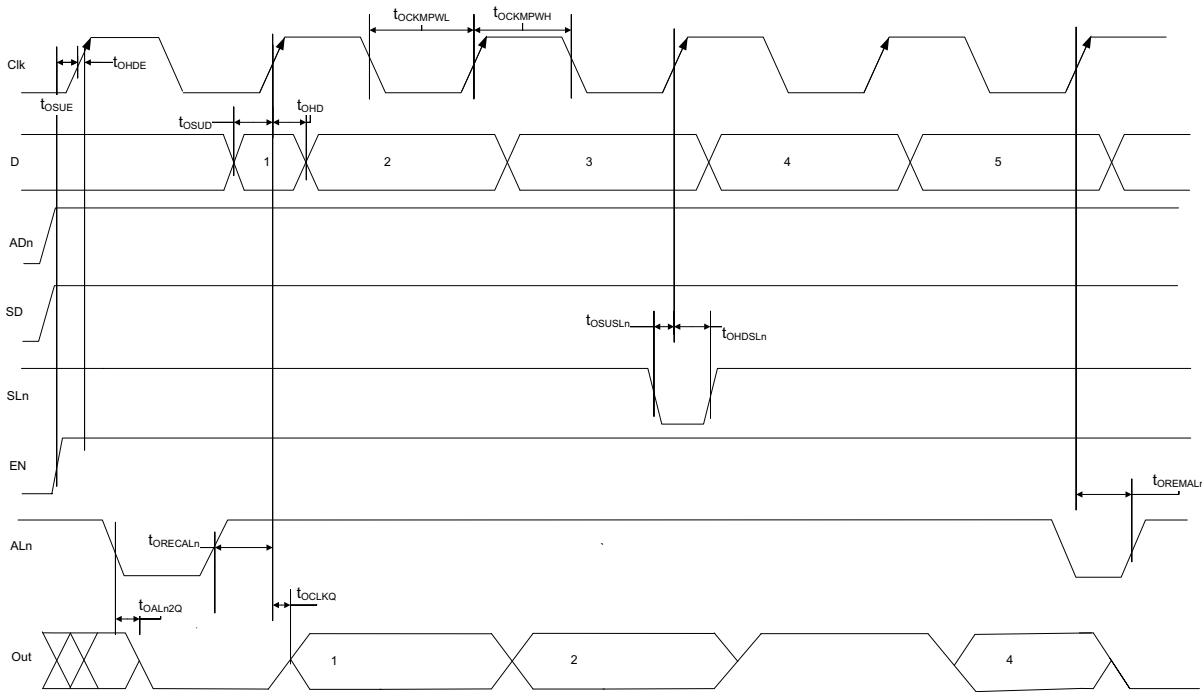


Figure 8 • I/O Register Output Timing Diagram

Table 109 • Output/Enable Data Register Propagation Delays
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Measuring Nodes (from, to)*	Speed Grade -1	Units
tOBYP	Bypass Delay of the Output/Enable Register	F,G or H,I	0.364	ns
tOCLKQ	Clock-to-Q of the Output/Enable Register	E,G or E,I	0.272	ns
tOSUD	Data Setup Time for the Output/Enable Register	A,E or J,E	0.196	ns
tOHD	Data Hold Time for the Output/Enable Register	A,E or J,E	0	ns
tOSUE	Enable Setup Time for the Output/Enable Register	B,E	0.433	ns
tOHE	Enable Hold Time for the Output/Enable Register	B,E	0	ns
tOSUSL	Synchronous Load Setup Time for the Output/Enable Register	D,E	0.203	ns
tOHSL	Synchronous Load Hold Time for the Output/Enable Register	D,E	0	ns
tOALn2Q	Asynchronous Clear-to-Q of the Output/Enable Register (ADn=1)	C,G or C,I	0.523	ns
	Asynchronous Preset-to-Q of the Output/Enable Register (ADn=0)	C,G or C,I	0.545	ns
tOREMALn	Asynchronous Load Removal Time for the Output/Enable Register	C,E	0	ns

9. Logic Element Specifications

9.1 4-input LUT (LUT-4)

The IGLOO2 and SmartFusion2 SoC FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *SmartFusion2 and IGLOO2 Macro Library Guide*.

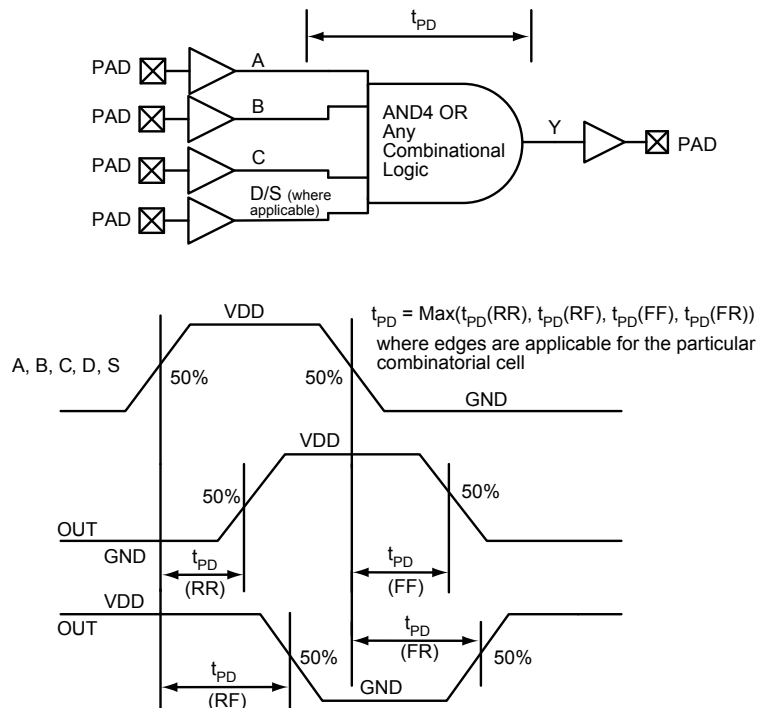


Figure 13 • LUT-4

Timing Characteristics

Table 112 • Combinatorial Cell Propagation Delays

Worst-Case Military Conditions: $T_j = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Combinatorial Cell	Equation	Parameter	Speed Grade -1	Units
INV	$Y = !A$	t_{PD}	0.106	ns
AND2	$Y = A \cdot B$	t_{PD}	0.17	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.157	ns
OR2	$Y = A + B$	t_{PD}	0.17	ns
NOR2	$Y = !(A + B)$	t_{PD}	0.157	ns
XOR2	$Y = A \oplus B$	t_{PD}	0.17	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	0.236	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	0.217	ns
AND4	$Y = A \cdot B \cdot C \cdot D$	t_{PD}	0.384	ns

9.2.1 Timing Characteristics

Table 113 • Register Delays

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade –1	Units
tCLKQ	Clock-to-Q of the Core Register	0.112	ns
tSUD	Data Setup Time for the Core Register	0.262	ns
tHD	Data Hold Time for the Core Register	0	ns
tSUE	Enable Setup Time for the Core Register	0.346	ns
tHE	Enable Hold Time for the Core Register	0	ns
tSUSL	Synchronous Load Setup Time for the Core Register	0.346	ns
tHSL	Synchronous Load Hold Time for the Core Register	0	ns
tALn2Q	Asynchronous Clear-to-Q of the Core Register (ADn=1)	0.49	ns
	Asynchronous Preset-to-Q of the Core Register (ADn=0)	0.466	ns
tREMAIn	Asynchronous Load Removal Time for the Core Register	0	ns
tRECAIn	Asynchronous Load Recovery Time for the Core Register	0.364	ns
tWALn	Asynchronous Load Minimum Pulse Width for the Core Register	0.266	ns
tCKMPWH	Clock Minimum Pulse Width High for the Core Register	0.065	ns
tCKMPWL	Clock Minimum Pulse Width Low for the Core Register	0.139	ns

10. Global Resource Characteristics

The IGLOO2 and SmartFusion2 SoC FPGA devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. Refer to the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for the positions of various global routing resources.

Table 114 • M2S150T Device Global Resource

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tRCKL	Input Low Delay for Global Clock	0.788	0.868	ns
tRCKH	Input High Delay for Global Clock	1.46	1.594	ns
tRCKSW	Maximum Skew for Global Clock	–	0.134	ns

Table 115 • M2S090T Device Global Resource

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tRCKL	Input Low Delay for Global Clock	0.793	0.847	ns

11. FPGA Fabric SRAM

Refer to the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for more information.

11.1 FPGA Fabric Large SRAM (LSRAM)

Table 119 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1Kx18
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t _{cy}	Clock Period	3.333	–	ns
t _{clkmpwh}	Clock Minimum Pulse Width High	1.5	–	ns
t _{clkmpwl}	Clock Minimum pulse Width Low	1.5	–	ns
t _{p_{cy}}	Pipelined Clock Period	3.333	–	ns
t _{p_{clkmpwh}}	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
t _{p_{clkmpwl}}	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
t _{clk2q}	Read Access Time with Pipeline Register	–	0.346	ns
	Read Access Time without Pipeline Register	–	2.346	ns
	Access Time with Feed-Through Write Timing	–	1.578	ns
t _{addr_{su}}	Address Setup Time	0.455	–	ns
t _{addr_{hd}}	Address Hold Time	0.282	–	ns
t _{dsu}	Data Setup Time	0.352	–	ns
t _{dhd}	Data Hold Time	0.11	–	ns
t _{blksu}	Block Select Setup Time	0.214	–	ns
t _{blkhd}	Block Select Hold Time	0.223	–	ns
t _{blk2q}	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	1.578	ns
t _{blkmpw}	Block Select Minimum Pulse Width	0.218	–	ns
t _{rdsu}	Read Enable Setup Time	0.463	–	ns
t _{rdehd}	Read Enable Hold Time	0.173	–	ns
t _{rdp_{lesu}}	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
t _{rdp_{lehd}}	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
t _{r2q}	Asynchronous Reset to Output Propagation Delay	–	1.561	ns
t _{rstrem}	Asynchronous Reset Removal Time	0.522	–	ns
t _{rstrec}	Asynchronous Reset Recovery Time	0.005	–	ns
t _{rstmpw}	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
t _{plrstrem}	Pipelined Register Asynchronous Reset Removal Time	–0.288	–	ns
t _{plrstrec}	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
t _{plrstmpw}	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns

Table 123 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16Kx1
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tpclkmpwl	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.332	ns
	Read Access Time without Pipeline Register	–	2.342	ns
	Access Time with Feed-Through Write Timing	–	1.559	ns
taddrsu	Address Setup Time	0.646	–	ns
taddrhd	Address Hold Time	0.282	–	ns
tdsu	Data Setup Time	0.332	–	ns
tdhd	Data Hold Time	0.084	–	ns
tblksu	Block Select Setup Time	0.214	–	ns
tblkhd	Block Select Hold Time	0.223	–	ns
tblk2q	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	1.559	ns
tblkmpw	Block Select Minimum Pulse Width	0.218	–	ns
trdesu	Read Enable Setup Time	0.547	–	ns
trdehd	Read Enable Hold Time	0.073	–	ns
trdple su	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
trdplehd	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
tr2q	Asynchronous Reset to Output Propagation Delay		1.603	ns
trstrem	Asynchronous Reset Removal Time	0.522	–	ns
trstrec	Asynchronous Reset Recovery Time	0.005	–	ns
trstmpw	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
tplrstrem	Pipelined Register Asynchronous Reset Removal Time	-0.288	–	ns
tplrstrec	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
tplrstmpw	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
tsrstsu	Synchronous Reset Setup Time	0.233	–	ns
tsrsthd	Synchronous Reset Hold Time	0.037	–	ns
twesu	Write Enable Setup Time	0.468	–	ns
twehd	Write Enable Hold Time	0.05	–	ns
Fmax	Maximum Frequency	–	300	MHz

Table 129 • uSRAM (RAM256x4) in 256x4 Mode
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
trdenhd	Read Enable Hold Time	0.059	–	ns
tblksu	Read Block Select Setup Time	1.898	–	ns
tblkhd	Read Block Select Hold Time	-0.671	–	ns
tblk2q	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.166	ns
trstrem	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
trstrec	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
tr2q	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.863	ns
tsrstsu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.062	–	ns
tccy	Write Clock Period	4	–	ns
tcclkmpwh	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclkmpwl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblkcsu	Write Block Setup Time	0.417	–	ns
tblkchd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.104	–	ns
tdinchd	Write Input Data hold Time	0.142	–	ns
taddrcsu	Write Address Setup Time	0.091	–	ns
taddrchd	Write Address Hold Time	0.253	–	ns
twecsu	Write Enable Setup Time	0.41	–	ns
twechd	Write Enable Hold Time	-0.027	–	ns
fmax	Maximum Frequency	–	250	MHz

Table 130 • uSRAM (RAM512x2) in 512x2 Mode
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
tcy	Read Clock Period	4	–	ns
tcclkmpwh	Read Clock Minimum Pulse Width High	1.8		ns

Table 130 • uSRAM (RAM512x2) in 512x2 Mode
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
tclcmpwl	Read Clock Minimum pulse Width Low	1.8	–	ns
tplcy	Read Pipe-line clock period	4	–	ns
tplclkmpwh	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
tplclkmpwl	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.824	ns
taddrsu	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	2.023	–	ns
taddrhd	Read Address Hold Time in Synchronous Mode	0.141	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.599	–	ns
trdensu	Read Enable Setup Time	0.287	–	ns
trdenhd	Read Enable Hold Time	0.059	–	ns
tblksu	Read Block Select Setup Time	1.898	–	ns
tblkhd	Read Block Select Hold Time	-0.671	–	ns
tblk2q	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.219	ns
trstrem	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
trstrec	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
tr2q	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.862	ns
tsrstsu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.062	–	ns
tccy	Write Clock Period	4	–	ns
tcclcmpwh	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclcmpwl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblkcsu	Write Block Setup Time	0.417	–	ns
tblkchd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.104	–	ns
tdinchd	Write Input Data hold Time	0.142	–	ns
taddrcsu	Write Address Setup Time	0.091	–	ns

24.3 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to Figure 17 on page 115.

Table 160 • SPI Characteristics

Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Symbol	Description	Conditions	All Devices/Speed Grades			Unit	Notes
			Min	Typ	Max		
sp1	SPI_[0 1]_CLK minimum period						
	SPI_[0 1]_CLK = PCLK/2	–	12	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/4	–	24.1	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/8	–	48.2	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/16	–	0.1	–	–	µs	–
	SPI_[0 1]_CLK = PCLK/32	–	0.19	–	–	µs	–
	SPI_[0 1]_CLK = PCLK/64	–	0.39	–	–	µs	–
	SPI_[0 1]_CLK = PCLK/128	–	0.77	–	–	µs	–
sp2	SPI_[0 1]_CLK minimum pulse width high						
	SPI_[0 1]_CLK = PCLK/2	–	6	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/4	–	12.05	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/8	–	24.1	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/16	–	0.05	–	–	µs	–
	SPI_[0 1]_CLK = PCLK/32	–	0.095	–	–	µs	–
	SPI_[0 1]_CLK = PCLK/64	–	0.195	–	–	µs	–
	SPI_[0 1]_CLK = PCLK/128	–	0.385	–	–	µs	–
sp3	SPI_[0 1]_CLK minimum pulse width low						
	SPI_[0 1]_CLK = PCLK/2	–	6	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/4	–	12.05	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/8	–	24.1	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/16	–	0.05	–	–	µs	–
	SPI_[0 1]_CLK = PCLK/32	–	0.095	–	–	µs	–
	SPI_[0 1]_CLK = PCLK/64	–	0.195	–	–	µs	–
	SPI_[0 1]_CLK = PCLK/128	–	0.385	–	–	µs	–

Notes:

- For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website:
<http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models>.
- For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.

Table 164 • SPI Characteristics

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Symbol	Description	Conditions	All Devices/Speed Grades			Unit	Notes
			Min	Typ	Max		
sp3	SPI_[0 1]_CLK minimum pulse width low						
	SPI_[0 1]_CLK = PCLK/2	–	6	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/4	–	12.05	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/8	–	24.1	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/16	–	0.05	–	–	µs	–
	SPI_[0 1]_CLK = PCLK/32	–	0.095	–	–	µs	–
	SPI_[0 1]_CLK = PCLK/64	–	0.195	–	–	µs	–
	SPI_[0 1]_CLK = PCLK/128	–	0.385	–	–	µs	–
sp4	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%-90%)	I/O Configuration: LVCMOS 2.5 V- 8mA AC Loading: 35pF Test Conditions: Typical Voltage, 25°C	–	2.77	–	ns	1
sp5	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%-90%)	I/O Configuration: LVCMOS 2.5 V- 8mA AC Loading: 35pF Test Conditions: Typical Voltage, 25°C	–	2.90 6	–	ns	1
SPI Master Configuration							
sp6m	SPI_[0 1]_DO setup time	–	(SPI_x_CLK_period/2) – 3.0	–	–	ns	2
sp7m	SPI_[0 1]_DO hold time	–	(SPI_x_CLK_period/2) – 2.5	–	–	ns	2
sp8m	SPI_[0 1]_DI setup time	–	8	–	–	ns	2
sp9m	SPI_[0 1]_DI hold time	–	2.5	–	–	ns	2
SPI Slave Configuration							
sp6s	SPI_[0 1]_DO setup time	–	(SPI_x_CLK_period/2) – 12.0	–	–	ns	2
sp7s	SPI_[0 1]_DO hold time	–	(SPI_x_CLK_period/2) + 3.0	–	–	ns	2
sp8s	SPI_[0 1]_DI setup time	–	2	–	–	ns	2