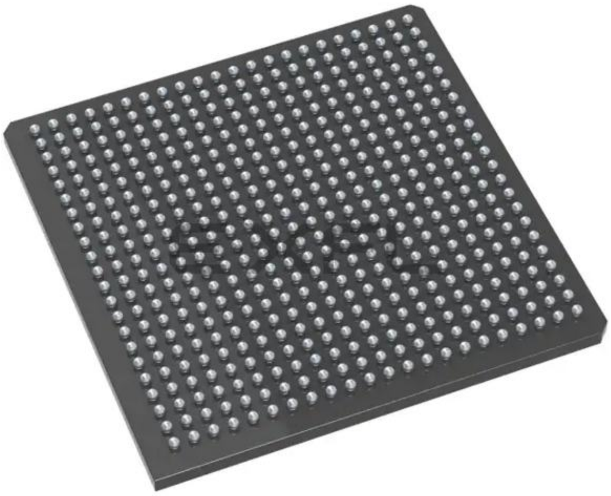
Microchip Technology - M2GL050TS-1FG484M Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	56340
Total RAM Bits	1869824
Number of I/O	267
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl050ts-1fg484m

Email: info@E-XFL.COM
Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

List of Figures

Table 3 • **Recommended Operating Conditions (continued)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
VPPNVM	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–

Notes:

1. *Programming at this temperature range is available only with VPP in 3.3 V Range*
2. *Power supply ramps must all be strictly monotonic, without plateaus.*

Table 4 • **FPGA Operating Limits**

Product Grade	Element	Programming Temperature	Operating Temperature	Programming Cycles	Retention (Biased/Unbiased)	Note
Military	FPGA	Min T_J = 0°C Max T_J = 85°C	Min T_J = -55°C Max T_J = 125°C	500	10 Years	–
		Min T_J = -40°C Max T_J = 100°C	Min T_J = -55°C Max T_J = 125°C	500	10 Years	*

*Note: *: Programming at this temperature range is available only with VPP in 3.3 V Range*

Table 5 • **Embedded Flash Limits**

Product Grade	Element	Programming Temperature	Maximum Operating Temperature	Programming Cycles	Retention (Biased/Unbiased)
Military	Embedded flash	Min T_J = -55°C Max T_J = 125°C	Min T_J = -55°C Max T_J = 125°C	< 10,000 cycles per pages, up to one million cycles per eNVM array	10 Years

Table 6 • **Device Storage Temperature and Retention**

Product Grade	Storage Temperature (Tstg)	Retention
Military	Min T_J = -55°C Max T_J = 125°C	10 Years

4.2 Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to -1.0 V for no longer than 10% or the period. The current during the transition must not exceed 100mA.

For AC signals, the input signal may overshoot during transitions to VCCI + 1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100mA.

Note: The above specification does not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant to the PCI standard including the PCI overshoot/undershoot specifications.

Table 24 • **LVTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications (Applicable to MSIO Bank* Only)**

Output Drive Selection	VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
2 mA	2.4	0.4	2	2
4 mA	2.4	0.4	4	4
8 mA	2.4	0.4	8	8
12 mA	2.4	0.4	12	12
16 mA	2.4	0.4	16	16
20 mA	2.4	0.4	18	18

Note: * *Software Configurator GUI displays the Commercial/Industrial numeric values. The actual drive capability at temperature is defined in Table 24.*

8.6.2.2 AC Switching Characteristics

Worst-case Military conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 3.15 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 25 • **LVTTL/LVCMOS 3.3 V Receiver Characteristics for MSIO I/O Banks (Input Buffers)**
Worst-case Military conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 3.15 V

	On-Die Termination (ODT)	Speed Grade –1		Units
		t_{PY}	t_{PYS}	
LVTTL/LVCMOS 3.3 V (for MSIO I/O Bank)	None	2.416	2.443	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 26 • **LVTTL/LVCMOS 3.3 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**
Worst-case Military conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 3.15 V

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
2mA	slow	3.515	3.826	3.242	2.024	3.636	ns
4mA	slow	2.565	2.948	2.774	3.339	4.896	ns
8mA	slow	2.349	2.568	2.528	5.013	5.329	ns
12mA	slow	2.261	2.324	2.386	6.389	6.05	ns
16mA	slow	2.274	2.287	2.369	6.671	6.256	ns
20mA	slow	2.372	2.206	2.306	6.976	6.541	ns

8.6.3 2.5 V LVCMOS

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in IGLOO2 FPGA and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-5A.

8.6.3.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 27 • **LVCMOS 2.5 V DC Voltage Specification**

Symbol	Parameters	Conditions	Min	Typ	Max	Units	Notes
LVCMOS 2.5 V Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	–
LVCMOS 2.5 V DC Input Voltage Specification							
VIH (DC)	DC input logic High (for MSIOD and DDRIO I/O Bank)		1.7	–	2.625	V	–
VIH (DC)	DC input logic High (for MSIO I/O Bank)		1.7	–	2.75	V	–
VIL (DC)	DC input logic Low		–0.3	–	0.7	V	–
IIH (DC)	Input current High		–	–	10	µA	–
IIL (DC)	Input current Low		–	–	10	µA	–
LVCMOS 2.5 V DC Output Voltage Specification							
VOH	DC output logic High		1.7	–	–	V	*
VOL	DC output logic Low		–	–	0.7	V	*
*Note: * The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.*							

Table 28 • **LVCMOS 2.5 V Maximum AC Switching Speeds**

Symbol	Parameters	Conditions	Min	Typ	Max	Units
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	360	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	360	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	370	Mbps

Table 29 • **LVCMOS 2.5 V AC Test Parameters and Driver Impedance Specifications**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 2.5 V Calibrated Impedance Option						
Rodt_cal	Supported output driver calibrated impedance (for DDRIO I/O Bank)	–	–	75, 60, 50, 33, 25, 20	–	Ω
LVCMOS 2.5 V AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path	–	–	1.2	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})	–	–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})	–	–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})	–	–	5	–	pF

Table 30 • **LVCMOS 2.5 V Transmitter Drive Strength Specifications**

Output Drive Selection			VOH (V) Min	VOL (V) Max	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (With Software Default Fixed Code)				
2 mA	2 mA	2 mA	1.7	0.7	2	2
4 mA	4 mA	4 mA	1.7	0.7	4	4
6 mA	6 mA	6 mA	1.7	0.7	6	6
8 mA	8 mA	8 mA	1.7	0.7	8	8
12 mA	12 mA	12 mA	1.7	0.7	12	12
16 mA	N/A	16 mA	1.7	0.7	16	16

Note: *For board design considerations, output slew rates extraction, detailed output buffer resistances and I/V Curve use the corresponding IBIS models located at: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models.*

8.6.3.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 31 • **LVCMOS 2.5 V AC Switching Characteristics for Receiver (Input Buffers)**
Worst-case Military conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 2.375 V

	On-Die Termination (ODT)	Speed Grade –1		Units
		t_{PY}	t_{PYS}	
LVCMOS 2.5 V (for DDRIO I/O Bank)	None	1.903	2.021	ns
LVCMOS 2.5 V (for MSIO I/O Bank)	None	2.689	2.698	ns
LVCMOS 2.5 V (for MSIOD I/O Bank)	None	2.447	2.46	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 32 • **LVCMOS 2.5 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
Worst-case Military conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 2.375 V

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVCMOS 2.5 V (for DDRIO I/O Bank with Fixed Code)							
2 mA	slow	3.967	3.664	3.986	4.172	3.811	ns
	medium	3.625	3.38	3.647	3.882	3.458	ns
	medium_fast	3.485	3.259	3.507	3.747	3.327	ns
	fast	3.458	3.253	3.48	3.74	3.31	ns
4 mA	slow	3.371	2.942	3.362	5.148	4.71	ns
	medium	3.063	2.701	3.059	4.874	4.381	ns
	medium_fast	2.925	2.566	2.92	4.686	4.248	ns
	fast	2.91	2.559	2.905	4.683	4.238	ns

8.6.4 1.8 V LVCMOS

LVCMOS 1.8 is a general standard for 1.8 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-7A.

8.6.4.1 Minimum and Maximum AC/DC Input and Output Levels

Table 33 • **LVCMOS 1.8 V DC Voltage Specification**

Symbols	Parameters	Min	Typ	Max	Units
Recommended DC Operating Conditions					
VDDI	Supply Voltage	1.710	1.8	1.89	V
LVCMOS 1.8 V DC Input Voltage Specification					
VIH(DC)	DC input Logic HIGH (for MSIOD and DDRIO I/O Banks)	0.65 x VDDI	–	1.89	V
VIH(DC)	DC input Logic HIGH (for MSIO I/O Bank)	0.65 x VDDI	–	2.75	V
VIL(DC)	DC input Logic LOW	-0.3	–	0.35 × VDDI	V
IIH(DC)	Input Current HIGH	–	–	10	uA
IIL(DC)	Input Current LOW	–	–	10	uA
LVCMOS 1.8 V DC Output Voltage Specification					
VOH	DC output Logic HIGH	VDDI - 0.45	–	–	V
VOL	DC output Logic LOW	–	–	0.45	V

Table 34 • **LVCMOS 1.8 V Maximum AC Switching Speeds**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 1.8 V Maximum AC Switching Speed						
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	360	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	260	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	360	Mbps
Note: ** Maximum data rate applies for drive strength 8mA and above, all slews*						

Table 35 • **LVCMOS 1.8 V Transmitter Drive Strength Specifications**

Output Drive Selection		VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	**MSIOD I/O Bank**	**Min**	**Max**		
2 mA	2 mA	VDDI – 0.45	0.45	2	2
4 mA	4 mA	VDDI – 0.45	0.45	4	4
6 mA	6 mA	VDDI – 0.45	0.45	6	6
8 mA	8 mA	VDDI – 0.45	0.45	8	8
10 mA	10 mA	VDDI – 0.45	0.45	10	10
12 mA	N/A	VDDI – 0.45	0.45	12	12

Table 56 • **HSTL DC Voltage Specification (Applicable to DDRIO I/O Bank Only) (continued)**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
VOL	DC output logic Low		–	–	0.4	V
IOH at VOH	Output minimum source DC current		–15.0	–	–	mA
IOL at VOL	Output minimum sink current		15.0	–	–	mA
HSTL DC Differential Voltage Specifications						
VID (DC)	DC input differential voltage		0.2	–	–	V

Table 57 • **HSTL AC Specifications (Applicable to DDRIO Bank Only)**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
HSTL AC Differential Voltage Specifications						
VDIFF	AC input differential voltage		0.4	–	–	V
Vx	AC differential cross point voltage		0.68	–	0.9	V
HSTL Maximum AC Switching Speed						
Dmax	Maximum data rate	AC loading: per JEDEC specifications	–	–	360	Mbps
HSTL Impedance Specification						
Rref	Supported output driver calibrated impedance (for DDRIO I/O Bank)	Reference resistance = 191 Ω	–	25.5, 47.8	–	Ω
RTT	Effective impedance value (ODT for DDRIO I/O Bank only)	Reference resistance = 191 Ω	–	47.8	–	Ω
HSTL AC Test Parameters Specification						
Vtrip	Measuring/trip point for data path		–	0.75	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF
Rtt_test	Reference resistance for data test path for HSTL15 Class I (t_{DP})		–	50	–	Ω
Rtt_test	Reference resistance for data test path for HSTL15 Class II (t_{DP})		–	25	–	Ω
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

8.7.1.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 58 • **HSTL15 AC Switching Characteristics for Receiver (Input Buffers)**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.425 V

		t_{PY}	
	ODT (On Die Termination)	**Speed Grade –1**	**Units**
HSTL (for DDRIO I/O Bank with Fixed Code)			
Pseudo-Differential	None	1.673	ns
True-Differential	None	1.693	ns

Table 72 • **LPDDR AC/DC Specifications (for DDRIO IO Bank Only)**

LPDDR Reduced Drive						
VOH	DC output logic High	0.9 × VDDI	–	–	V	–
VOL	DC output logic Low	–	–	0.1 × VDDI	V	–
IOH at VOH	Output minimum source DC current	0.1	–	–	mA	–
IOL at VOL	Output minimum sink current	–0.1	–	–	mA	–
LPDDR Full Drive						*
VOH	DC output logic High	0.9 × VDDI	–	–	V	–
VOL	DC output logic Low	–	–	0.1 × VDDI	V	–
IOH at VOH	Output minimum source DC current	0.1	–	–	mA	–
IOL at VOL	Output minimum sink current	–0.1	–	–	mA	–
LPDDR DC Differential Voltage Specification						
VID (DC)	DC input differential voltage	0.4 × VDDI	–	–	V	–
Note: **To meet JEDEC Electrical Compliance, use LPDDR Full Drive Transmitter.*						

Table 73 • **LPDDR Maximum AC Switching Speeds (for DDRIO I/O Bank Only)**

Symbols	**Parameters**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Dmax	Maximum data rate	AC loading: per JEDEC specifications	–	–	360	Mbps

Table 74 • **LPDDR AC Specifications (for DDRIO IO Bank Only)**

Symbols	**Parameters**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
LPDDR AC Differential Voltage Specification						
VDIFF (AC)	AC Input differential voltage	–	0.6 × VDDI	–	–	V
Vx (AC)	AC Differential Cross Point Voltage	–	0.4 × VDDI	–	0.6 × VDDI	V
LPDDR Impedance Specifications						
Rref	Supported Output Driver Calibrated Impedance	Reference Resistor = 150 Ω	–	20,42	–	Ω
RTT	Effective impedance Value - ODT	Reference Resistor = 150 Ω	–	50, 75, 150	–	Ω
LPDDR AC Test Parameters Specifications						
Vtrip	Measuring/Trip Point for Data Path	–	–	0.9	–	V
Rent	Resistance for Enable Path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})	–	–	2k	–	Ω
Cent	Capacitive Loading for Enable Path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})	–	–	5	–	pF
Rtt_test	Reference resistance for Data Test Path for LPDDR (t_{DP})	–	–	50	–	Ω
Cload	Capacitive Loading for Data Path (t_{DP})	–	–	5	–	pF

AC Switching Characteristics for Transmitter (Output and Tristate Buffers

Table 82 • LPDDR - LVCMOS 1.8 V AC Switching Characteristics for Transmitter DDRIO I/O Bank (Output and Tristate Buffers)

Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.71 V

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
2 mA	slow	4.681	4.017	4.69	5.388	4.852	ns
	medium	4.211	3.599	4.219	5.058	4.488	ns
	medium_fast	3.978	3.392	3.986	4.874	4.327	ns
	fast	3.953	3.373	3.961	4.858	4.316	ns
4 mA	slow	4.355	3.657	4.346	5.967	5.399	ns
	medium	3.886	3.246	3.879	5.628	5.01	ns
	medium_fast	3.656	3.05	3.647	5.461	4.845	ns
	fast	3.635	3.033	3.626	5.447	4.838	ns
6 mA	slow	4.105	3.422	4.092	6.221	5.599	ns
	medium	3.68	3.05	3.668	5.9	5.257	ns
	medium_fast	3.477	2.867	3.463	5.739	5.118	ns
	fast	3.451	2.849	3.437	5.72	5.104	ns
8 mA	slow	4.015	3.32	3.998	6.458	5.808	ns
	medium	3.59	2.947	3.574	6.129	5.449	ns
	medium_fast	3.383	2.761	3.366	5.963	5.304	ns
	fast	3.357	2.746	3.34	5.954	5.289	ns
10 mA	slow	3.888	3.18	3.864	6.739	6.045	ns
	medium	3.485	2.822	3.467	6.422	5.7	ns
	medium_fast	3.281	2.642	3.26	6.277	5.553	ns
	fast	3.258	2.627	3.238	6.27	5.546	ns
12 mA	slow	3.795	3.096	3.773	6.773	6.067	ns
	medium	3.408	2.764	3.389	6.47	5.743	ns
	medium_fast	3.215	2.599	3.194	6.346	5.61	ns
	fast	3.196	2.584	3.175	6.335	5.604	ns
16 mA	slow	3.744	3.035	3.719	6.944	6.207	ns
	medium	3.358	2.712	3.339	6.657	5.868	ns
	medium_fast	3.175	2.546	3.153	6.547	5.751	ns
	fast	3.156	2.531	3.133	6.541	5.747	ns

8.8. Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero® System-on-Chip (SoC) software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

8.8.1 LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

8.8.1.1 Minimum and Maximum Input and Output Levels

Table 83 • **LVDS DC Voltage Specification**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVDS Recommended DC Operating Conditions						
VDDI	Supply voltage	2.5 V range	2.375	2.5	2.625	V
VDDI	Supply voltage	3.3 V range	3.15	3.3	3.45	V
LVDS DC Input Voltage Specification						
VI	DC Input voltage	2.5 V range	0	–	2.925	V
VI	DC input voltage	3.3 V range	0	–	3.45	V
IIH (DC)	Input current High		–	–	10	µA
IIL (DC)	Input current Low		–	–	10	µA
LVDS DC Output Voltage Specification						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
LVDS Differential Voltage Specification						
VOD	Differential output voltage swing		250	350	450	mV
VOCM	Output common mode voltage		1.125	1.25	1.375	V
VICM	Input common mode voltage		0.05	1.25	2.35	V
VID	Input differential voltage		100	350	600	mV

Table 84 • **LVDS AC Specifications**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVDS Maximum AC Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 12 pF / 100 Ω differential load	–	–	480	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 10 pF / 100 Ω differential load	–	–	480	Mbps
LVDS Impedance Specification						
Rt	Termination resistance	–	–	100	–	Ω
LVDS AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF

Table 106 • **LVPECL Maximum AC Switching Speeds (Applicable to MSIO I/O Banks Only)**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVPECL AC Specifications						
Fmax	Maximum data rate (for MSIO I/O Bank)		–	–	810	Mbps

8.8.6.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 107 • **LVPECL Receiver Characteristics**

Worst-case Military conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 3.15 V

		t_{PY}	
	On-Die Termination (ODT)	**Speed Grade –1**	**Units**
LVPECL (for MSIO I/O Bank)	None	2.71	ns
	100	2.71	ns

8.9 I/O Register Specifications

8.9.1 Input Register

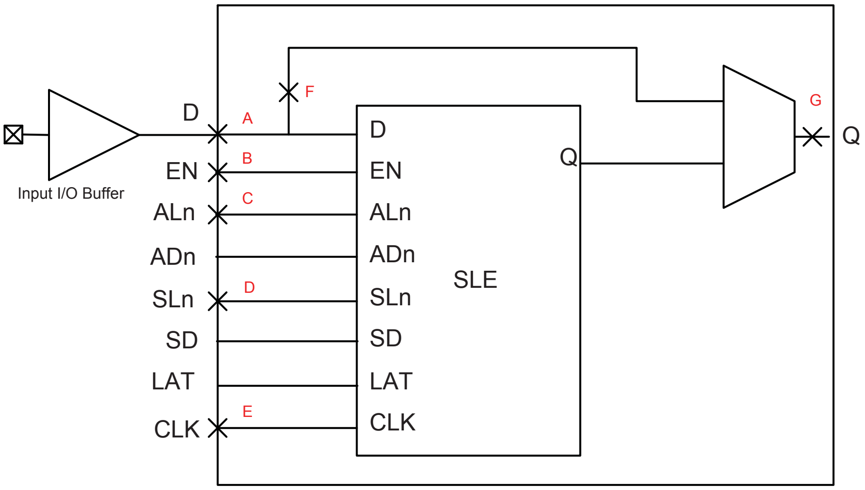


Figure 5 • **Timing Model for Input Register**

Table 109 • **Output/Enable Data Register Propagation Delays**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Measuring Nodes (from, to)*	Speed Grade –1	Units
tORECALn	Asynchronous Load Recovery Time for the Output/Enable Register	C,E	0.035	ns
tOWALn	Asynchronous Load Minimum Pulse Width for the Output/Enable Register	C,C	0.266	ns
tOCKMPWH	Clock Minimum Pulse Width High for the Output/Enable Register	E,E	0.065	ns
tOCKMPWL	Clock Minimum Pulse Width Low for the Output/Enable Register	E,E	0.139	ns

8.10 DDR Module Specification

8.10.1 Input DDR Module

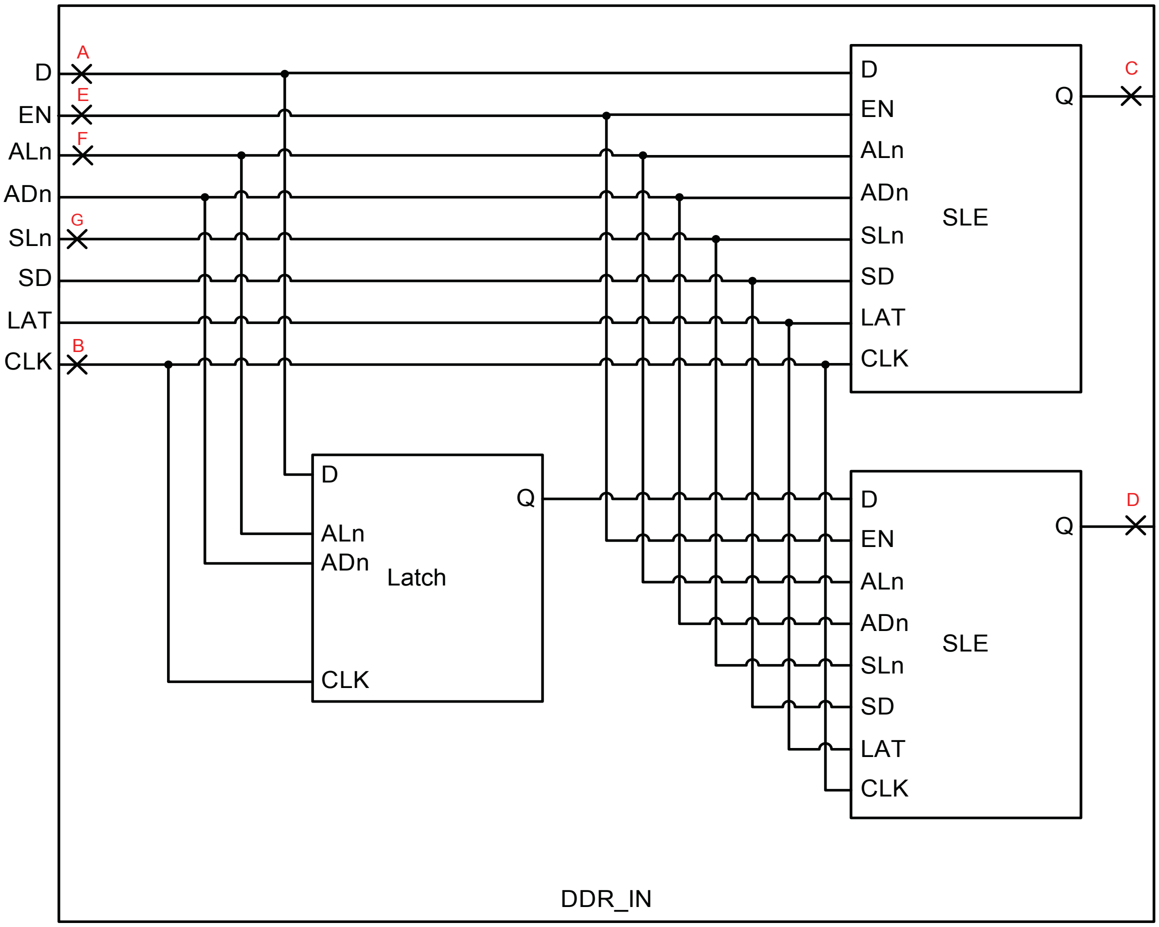


Figure 9 • **Input DDR Module**

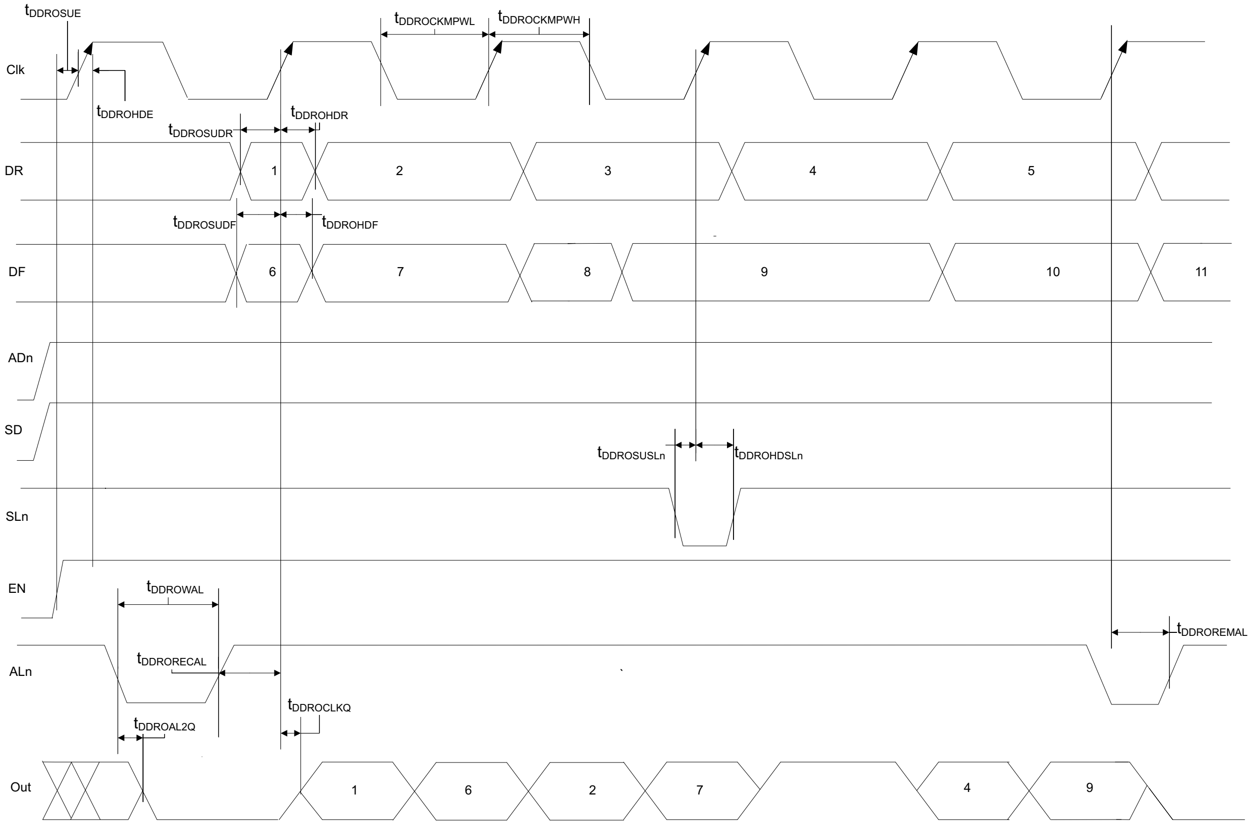


Figure 12 • **Output DDR Timing Diagram**

***Table 123* • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16Kx1**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tplclkmpwl	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.332	ns
	Read Access Time without Pipeline Register	–	2.342	ns
	Access Time with Feed-Through Write Timing	–	1.559	ns
taddrsu	Address Setup Time	0.646	–	ns
taddrhd	Address Hold Time	0.282	–	ns
tdsu	Data Setup Time	0.332	–	ns
tdhd	Data Hold Time	0.084	–	ns
tblksu	Block Select Setup Time	0.214	–	ns
tblkhd	Block Select Hold Time	0.223	–	ns
tblk2q	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	1.559	ns
tblkmpw	Block Select Minimum Pulse Width	0.218	–	ns
trdesu	Read Enable Setup Time	0.547	–	ns
trdehd	Read Enable Hold Time	0.073	–	ns
trdplesu	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
trdplehd	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
tr2q	Asynchronous Reset to Output Propagation Delay		1.603	ns
trstrem	Asynchronous Reset Removal Time	0.522	–	ns
trstrec	Asynchronous Reset Recovery Time	0.005	–	ns
trstmpw	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
tplrstrem	Pipelined Register Asynchronous Reset Removal Time	-0.288	–	ns
tplrstrec	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
tplrstmpw	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
tsrstsu	Synchronous Reset Setup Time	0.233	–	ns
tsrsthd	Synchronous Reset Hold Time	0.037	–	ns
twesu	Write Enable Setup Time	0.468	–	ns
twehd	Write Enable Hold Time	0.05	–	ns
Fmax	Maximum Frequency	–	300	MHz

***Table 130* • uSRAM (RAM512x2) in 512x2 Mode**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tclkmpwl	Read Clock Minimum pulse Width Low	1.8	–	ns
tplcy	Read Pipe-line clock period	4	–	ns
tplclkmpwh	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
tplclkmpwl	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.824	ns
taddrsu	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	2.023	–	ns
taddrhd	Read Address Hold Time in Synchronous Mode	0.141	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.599	–	ns
trdensu	Read Enable Setup Time	0.287	–	ns
trdenhd	Read Enable Hold Time	0.059	–	ns
tblksu	Read Block Select Setup Time	1.898	–	ns
tblkhd	Read Block Select Hold Time	-0.671	–	ns
tblk2q	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.219	ns
trstrem	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
trstrec	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
tr2q	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.862	ns
tsrstsu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.062	–	ns
tccy	Write Clock Period	4	–	ns
tcclkmpwh	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclkmpwl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblkcsu	Write Block Setup Time	0.417	–	ns
tblkchd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.104	–	ns
tdinchd	Write Input Data hold Time	0.142	–	ns
taddrcsu	Write Address Setup Time	0.091	–	ns

***Table 131* • uSRAM (RAM1024x1) in 1024x1 Mode**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tr2q	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.862	ns
tsrstsu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.062	–	ns
tccy	Write Clock Period	4	–	ns
tcclkmpwh	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclkmpwl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblkcsu	Write Block Setup Time	0.417	–	ns
tblkchd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.003	–	ns
tdinchd	Write Input Data hold Time	0.142	–	ns
taddrcsu	Write Address Setup Time	0.091	–	ns
taddrchd	Write Address Hold Time	0.255	–	ns
twecsu	Write Enable Setup Time	0.41	–	ns
twechd	Write Enable Hold Time	-0.027	–	ns
fmax	Maximum Frequency	–	250	MHz

17. DEVRST_N Characteristics

Table 142 • **DEVRST_N Characteristics**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

		All Devices/Speed Grades				
Symbol	**Description**	**Min**	**Typ**	**Max**	**Units**	**Notes**
TRAMPDEVRSTN	DEVRST_N ramp rate	–	–	10	ns	*

Note: ** Slower ramp rates are susceptible to board level noise.*

Table 147 • **Mathblock With Input Register Used and Output in Bypass Mode**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Mathblock With Input Register Used and Output in Bypass Mode		Speed Grade –1		
Parameter	**Description**	**Min**	**Max**	**Units**
TMISU	Input Register Setup time	0.149	–	ns
TMIHD	Input Register Hold time	0.08	–	ns
TMSRSTENSU	Synchronous Reset/Enable Setup time	0.185	–	ns
TMSRSTENHD	Synchronous Reset/Enable Hold time	-0.012	–	ns
TMARSTREM	Asynchronous Reset Removal time	-0.005	–	ns
TMARSTREC	Asynchronous Reset Recovery time	0.088	–	ns
TMICQ	Input Register Clock to Output delay	–	2.52	ns
TMCDIN2Q	CDIN to Output delay	–	1.951	ns

Table 148 • **Mathblock With Input and Output in Bypass Mode**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Mathblock With Input and Output in Bypass Mode		Speed Grade –1		
Parameter	**Description**	**Min**	**Max**	**Units**
TMIQ	Input to Output delay	–	2.568	ns
TMCDIN2Q	CDIN to Output delay	–	1.951	ns

20. Flash*Freeze Timing Characteristics

Table 149 • **Flash*Freeze Entry and Exit Times**
Military Worst-Case conditions: T_J = 125°C, VDD = 1.14 V

Symbols	Parameters	Conditions	Entry/Exit Timing	Units	Notes
TFF_ENTRY	Entry time	eNVM and MSS/HPMS PLL = ON	160	µs	1
		eNVM and MSS/HPMS PLL = OFF	215	µs	1

21. DDR Memory Interface Characteristics

***Table 150* • DDR Memory Interface Characteristics**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

	Supported Data Rate			
Standard	**Min**	**Typ**	**Max**	**Unit**
DDR3	667			Mbps
DDR2	667			Mbps
LPDDR	50	–	400	Mbps

24.3 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to Figure 17 on page 115.

***Table 160* • SPI Characteristics**

Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Symbol	Description	Conditions	All Devices/Speed Grades			Unit	Notes
			Min	Typ	Max		
sp1	**SPI_[0|1]_CLK minimum period**						
	SPI_[0|1]_CLK = PCLK/2	–	12	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/4	–	24.1	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/8	–	48.2	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/16	–	0.1	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/32	–	0.19	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/64	–	0.39	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/128	–	0.77	–	–	µs	–
sp2	**SPI_[0|1]_CLK minimum pulse width high**						
	SPI_[0|1]_CLK = PCLK/2	–	6	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/4	–	12.05	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/8	–	24.1	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/16	–	0.05	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/32	–	0.095	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/64	–	0.195	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/128	–	0.385	–	–	µs	–
sp3	**SPI_[0|1]_CLK minimum pulse width low**						
	SPI_[0|1]_CLK = PCLK/2	–	6	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/4	–	12.05	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/8	–	24.1	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/16	–	0.05	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/32	–	0.095	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/64	–	0.195	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/128	–	0.385	–	–	µs	–

Notes:

1. *For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.*