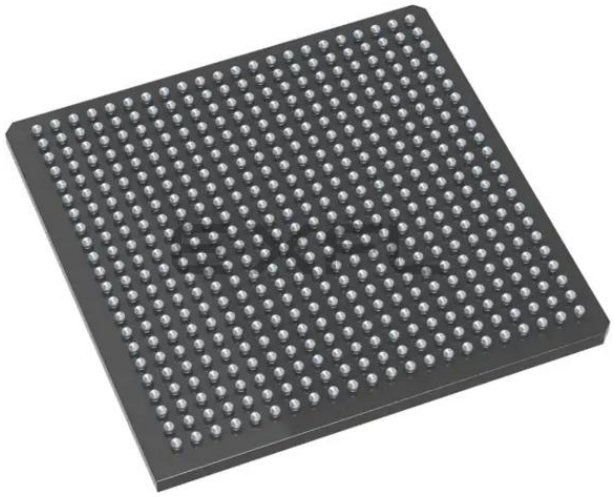

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 86184 |
| Total RAM Bits | 2648064 |
| Number of I/O | 267 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | -55°C ~ 125°C (TJ) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m2gl090t-1fg484m |

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***Table 2 •*** **Absolute Maximum Ratings (continued)**

| Symbol | Parameter | Limits | | Units | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $T_{STG}$ | Storage temperature | –65 | 150 | °C | * |
| $T_J$ | Junction temperature | – | 135 | °C | – |

*Note: * For flash programming and retention maximum limits, refer to Table 4 on page 14. For recommended operating conditions, refer to Table 3.*

***Table 3 •*** **Recommended Operating Conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Tj | Operating Junction Temperature | Military | -55 | 25 | 125 | °C | – |
| | Programming Junction Temperature | – | 0 | 25 | 85 | °C | – |
| | | – | -40 | 25 | 100 | °C | 1 |
| VDD | DC core supply voltage. Must always power this pin. | – | 1.14 | 1.2 | 1.26 | V | – |
| VPP | Power Supply for Charge Pumps (for Normal Operation and Programming) for 010, 025, 050 Devices | 2.5 V Range | 2.375 | 2.5 | 2.625 | V | – |
| | | 3.3 V Range | 3.15 | 3.3 | 3.45 | V | – |
| | Power Supply for Charge Pumps (for Normal Operation and Programming) for 090, and 150 devices | 3.3 V Range | 3.15 | 3.3 | 3.45 | V | – |
| MSS_MDDR_PLL_VDDA | Analog power pad for MDDR PLL | 2.5 V Range | 2.375 | 2.5 | 2.625 | V | – |
| | | 3.3 V Range | 3.15 | 3.3 | 3.45 | V | – |
| HPMS_MDDR_PLL_VDDA | Analog power pad for MDDR PLL | 2.5 V Range | 2.375 | 2.5 | 2.625 | V | – |
| | | 3.3 V Range | 3.15 | 3.3 | 3.45 | V | – |
| FDDR_PLL_VDDA | Analog power pad for FDDR PLL | 2.5 V Range | 2.375 | 2.5 | 2.625 | V | – |
| | | 3.3 V Range | 3.15 | 3.3 | 3.45 | V | – |
| PLL0_PLL1_MSS_MDDR_VDDA | Analog power pad for MDDR PLL | 2.5 V Range | 2.375 | 2.5 | 2.625 | V | – |
| | | 3.3 V Range | 3.15 | 3.3 | 3.45 | V | – |

# 5. Power Consumption

## 5.1 Quiescent Supply Current

***Table 8 •*** **Quiescent Supply Current Characteristics**

| Power Supplies/Blocks | Modes and Configurations | | Notes |
|---|---|---|---|
| | Non-Flash*Freeze Mode | Flash*Freeze Mode | |
| FPGA Core | On | Off | – |
| VDD / SERDES_[01]_VDD | On | On | 1 |
| VPP / VPPNVM | On | On | – |
| MDDR_PLL_VDDA<br>CCC_XX[01]_PLL_VDDA<br>PLL0_PLL1_MDDR_VDDA<br>FDDR_PLL_VDDA | 0 V | 0 V | – |
| SERDES_[01]_PLL_VDDA | 0 V | 0 V | 3 |
| SERDES_[01]_L[0123]_VDDAPLL / VDD_2V5 | On | On | 3 |
| SERDES_[01]_L[0123]_VDDAIIO | On | On | 3 |
| VDDIx | On | On | 2, 4 |
| VREFx | On | On | – |
| MSSDDR CLK | 32 kHz | 32 kHz | – |
| RAM | On | Sleep state | – |
| HPMS Controller | 50 MHz | 50 MHz | – |
| 50 MHz Oscillator (enable/disable) | Enabled | Disabled | – |
| 1 MHz Oscillator (enable/disable) | Disabled | Disabled | – |
| Crystal Oscillator (enable/disable) | Disabled | Disabled | – |

*Notes:*

1. *SERDES_[01]_VDD Power Supply is shorted to VDD.*
2. *VDDIx has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate VDDI Bank supplies. For details on bank power supplies, refer to the "Recommendation for Unused Bank Supplies" table in the AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note.*
3. *SERDES and DDR blocks to be unused.*
4. *No Differential (that is to say, LVDS) I/O's or ODT attributes to be used.*

***Table 9 •*** **SmartFusion2 and IGLOO2 Quiescent Supply Current – Typical Process**

| Parameter | Modes | Conditions | 010 | 025 | 050 | 090 | 150 | Units |
|---|---|---|---|---|---|---|---|---|
| | | | VDD=1.2 V | VDD=1.2 V | VDD=1.2 V | VDD=1.2 V | VDD=1.2 V | |
| IDC1 | Non-Flash*Freeze | Typical ($T_J$ = 25°C) | 6.9 | 8.9 | 13.1 | 15.4 | 27.5 | mA |
| | | Military ($T_J$ = 125°C) | 73.0 | 106.4 | 180.9 | 217.5 | 390.5 | mA |
| IDC2 | Flash*Freeze | Typical ($T_J$ = 25°C) | 2.6 | 3.7 | 5.1 | 5.1 | 8.9 | mA |
| | | Military ($T_J$ = 125°C) | 55.6 | 74.2 | 98.5 | 99.5 | 161.0 | mA |

## 8.3. Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The methodology of characterization is illustrated by the enable path test point shown in Figure 4.

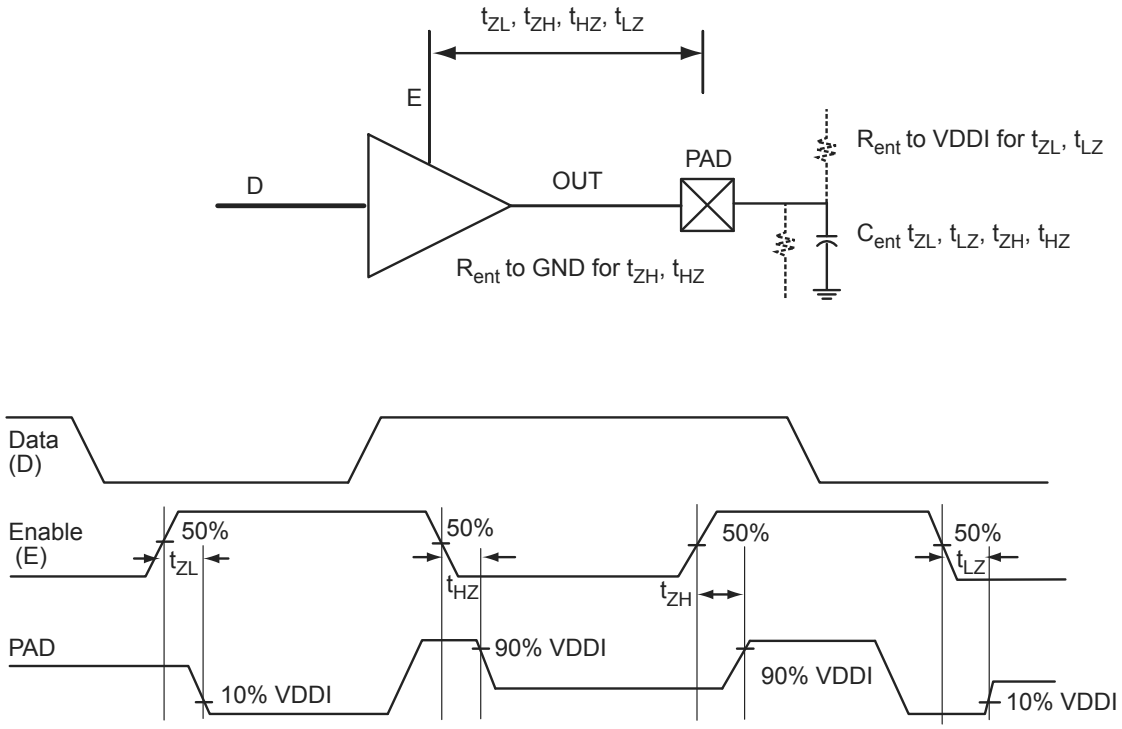


***Figure 4* • Tristate Buffer for Enable Path Test Point**

***Table 63 •*** **DDR1/SSTL2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V, VDDI= 2.375 V (continued)**

| | Speed Grade –1 | | | | | Units |
|---|---|---|---|---|---|---|
| | $t_{DP}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ | |
| **MSIO I/O Bank** | | | | | | |
| Single Ended | 2.563 | 2.208 | 2.19 | 2.205 | 2.187 | ns |
| Differential | 2.703 | 2.566 | 2.555 | 2.363 | 2.353 | ns |

## 8.7.4 Stub-Series Terminated Logic 1.8 V (SSTL18)

SSTL18 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double date rate (DDR2) standard. IGLOO2 and SmartFusion2 SoC FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

### 8.7.4.1 Minimum and Maximum Input and Output Levels Specification

***Table 64 •*** **DDR2/SSTL18 AC/DC Minimum and Maximum Input and Output Levels Specification**

| Symbols | Parameters | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| **Recommended DC Operating Conditions** | | | | | | | |
| VDDI | Supply voltage | | 1.71 | 1.8 | 1.89 | V | – |
| VTT | Termination voltage | | 0.838 | 0.900 | 0.964 | V | – |
| VREF | Input reference voltage | | 0.838 | 0.900 | 0.964 | V | – |
| **SSTL18 DC Input Voltage Specification** | | | | | | | |
| VIH (DC) | DC input logic High | | VREF + 0.125 | – | 1.89 | V | – |
| VIL (DC) | DC input logic Low | | –0.3 | – | VREF – 0.125 | V | – |
| IIH (DC) | Input current High | | – | – | 10 | µA | – |
| IIL (DC) | Input current Low | | – | – | 10 | µA | – |
| **SSTL18 DC Output Voltage Specification** | | | | | | | |
| **SSTL18 Class I (DDR2 Reduced Drive)** | | | | | | | |
| VOH | DC output logic High | | VTT + 0.603 | – | – | V | – |
| VOL | DC output logic Low | | – | – | VTT– 0.603 | V | – |
| IOH at VOH | Output minimum source DC current (DDRIO I/O Bank only) | | 6.0 | – | – | mA | – |
| IOL at VOL | Output minimum sink current (DDRIO I/O Bank only) | | –6.0 | – | – | mA | – |
| **SSTL18 Class II (DDR2 Full Drive)** | | | | | | | * |
| VOH | DC output logic High | | VTT + 0.603 | – | – | V | – |
| VOL | DC output logic Low | | – | – | VTT– 0.603 | V | – |
| IOH at VOH | Output minimum source DC current (DDRIO I/O Bank only) | | 12.0 | – | – | mA | – |

*Note: *To meet JEDEC Electrical Compliance, use DDR2 Full Drive Transmitter.*

***Table 78 •*** **LPDDR-LVCMOS 1.8 V Maximum AC Switching Speeds (Applicable to DDRIO I/O Bank Only)**

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Dmax | Maximum Data Rate (for DDRIO I/O Bank) | AC Loading: 17pF Load, 8mA Drive and Above/All Slew | – | – | 360 | Mbps |

***Table 79 •*** **LPDDR-LVCMOS 1.8 V AC Test Parameters and Driver Impedance Specifications (Applicable to DDRIO I/O Bank Only)**

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **LPDDR - LVCMOS 1.8 V Calibrated Impedance Option** | | | | | | |
| Rodt_cal | Supported Output Driver Calibrated Impedance (for DDRIO I/O Bank) | – | – | 75, 60, 50, 33, 25, 20 | – | Ω |
| **LPDDR- LVCMOS 1.8 V AC Test Parameters Specifications** | | | | | | |
| Vtrip | Measuring/Trip Point for Data Path | – | – | 0.9 | – | V |
| Rent | Resistance for Enable Path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | – | – | 2k | – | Ω |
| Cent | Capacitive Loading for Enable Path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | – | – | 5 | – | pF |
| Cload | Capacitive Loading for Data Path ($t_{DP)}$ | – | – | 5 | – | pF |

***Table 80 •*** **LPDDR-LVCMOS 1.8 V Mode Transmitter Drive Strength Specification (Applicable to DDRIO I/O Bank Only)**

| Output Drive Selection | VOH (V) Min | VOL (V) Max | IOH (at VOH) mA | IOL (at VOL) mA | Notes |
|---|---|---|---|---|---|
| 2 mA | VDDI – 0.45 | 0.45 | 2 | 2 | – |
| 4 mA | VDDI – 0.45 | 0.45 | 4 | 4 | – |
| 6 mA | VDDI – 0.45 | 0.45 | 6 | 6 | – |
| 8 mA | VDDI – 0.45 | 0.45 | 8 | 8 | – |
| 10 mA | VDDI – 0.45 | 0.45 | 10 | 10 | – |
| 12 mA | VDDI – 0.45 | 0.45 | 12 | 12 | – |
| 16 mA | VDDI – 0.45 | 0.45 | 16 | 16 | * |
| *Note: * 16mA Drive Strengths, All Slews, meet LPDDR JEDEC electrical compliance* | | | | | |

### *8.7.6.4 AC Switching Characteristics*

***Table 81 •*** **LPPDR - LVCMOS 1.8 V AC Switching Characteristics for Receiver (Input Buffers)**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V, VDDI = 1.71 V**

| | ODT (On Die Termination) | Speed Grade –1 | | Units |
|---|---|---|---|---|
| | | $t_{PY}$ | $t_{PYS}$ | |
| **LPDDR-LVCMOS 1.8 mode (for DDRIO I/O Bank with Fixed Codes)** | None | 2.071 | 2.213 | ns |

### 8.8.5.2. AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

**Table 103 • RSDS AC Switching Characteristics for Receiver (Input Buffers)**
**Worst-case Military conditions: $T_J$ = 125°C, VDD = 1.14 V, VDDI = 2.375 V**

| | On-Die Termination (ODT) | Speed Grade –1 | Units |
|---|---|---|---|
| | | $t_{PY}$ | |
| **RSDS (for MSIO I/O Bank)** | None | 3.112 | ns |
| | 100 | 3.108 | ns |
| **RSDS (for MSIOD I/O Bank)** | None | 2.832 | ns |
| | 100 | 2.821 | ns |

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 104 • RSDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
**Worst-case Military conditions: $T_J$ = 125°C, VDD = 1.14 V, VDDI = 2.375 V**

| | Speed Grade –1 | | | | | Units |
|---|---|---|---|---|---|---|
| | $t_{DP}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ | |
| **RSDS (for MSIO I/O Bank)** | 2.256 | 2.484 | 2.472 | 2.111 | 2.096 | ns |
| **RSDS (for MSIOD I/O Bank)** | | | | | | |
| No pre-emphasis | 1.661 | 1.648 | 1.645 | 1.675 | 1.665 | ns |
| Min pre-emphasis | 1.651 | 1.84 | 1.833 | 1.988 | 1.964 | ns |
| Med pre-emphasis | 1.577 | 1.868 | 1.859 | 2.019 | 1.993 | ns |
| Max pre-emphasis | 1.555 | 1.894 | 1.883 | 2.047 | 2.018 | ns |

## 8.8.6 LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO2 and SmartFusion2 SoC FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

### 8.8.6.1 Minimum and Maximum Input and Output Levels

**Table 105 • LVPECL DC Voltage Specification (Applicable to MSIO I/O Banks Only)**

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Recommended DC Operating Conditions** | | | | | | |
| VDDI | Supply voltage | | 3.15 | 3.3 | 3.45 | V |
| **LVPECL DC Input Voltage Specification** | | | | | | |
| VI | DC input voltage | | 0 | – | 3.45 | V |
| **LVPECL Differential Voltage Specification** | | | | | | |
| VICM | Input common mode voltage | | 0.3 | | 2.8 | V |
| VIDIFF | Input differential voltage | | 100 | 300 | 1,000 | mV |

**Table 122 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8Kx2**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V (continued)**

| Parameter | Description | Speed Grade –1 | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| tdsu | Data Setup Time | 0.34 | – | ns |
| tdhd | Data Hold Time | 0.084 | – | ns |
| tblksu | Block Select Setup Time | 0.214 | – | ns |
| tblkhd | Block Select Hold Time | 0.223 | – | ns |
| tblk2q | Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | – | 1.56 | ns |
| tblkmpw | Block Select Minimum Pulse Width | 0.218 | – | ns |
| trdesu | Read Enable Setup Time | 0.546 | – | ns |
| trdehd | Read Enable Hold Time | 0.073 | – | ns |
| trdplesu | Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN) | 0.256 | – | ns |
| trdplehd | Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN) | 0.106 | – | ns |
| tr2q | Asynchronous Reset to Output Propagation Delay | – | 1.583 | ns |
| trstrem | Asynchronous Reset Removal Time | 0.522 | – | ns |
| trstrec | Asynchronous Reset Recovery Time | 0.005 | – | ns |
| trstmpw | Asynchronous Reset Minimum Pulse Width | 0.352 | – | ns |
| tplrstrem | Pipelined Register Asynchronous Reset Removal Time | -0.288 | – | ns |
| tplrstrec | Pipelined Register Asynchronous Reset Recovery Time | 0.338 | – | ns |
| tplrstmpw | Pipelined Register Asynchronous Reset Minimum Pulse Width | 0.33 | – | ns |
| tsrstsu | Synchronous Reset Setup Time | 0.233 | – | ns |
| tsrsthd | Synchronous Reset Hold Time | 0.037 | – | ns |
| twesu | Write Enable Setup Time | 0.504 | – | ns |
| twehd | Write Enable Hold Time | 0.05 | – | ns |
| Fmax | Maximum Frequency | – | 300 | MHz |

**Table 123 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16Kx1**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V**

| Parameter | Description | Speed Grade –1 | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| tcy | Clock Period | 3.333 | – | ns |
| tclkmpwh | Clock Minimum Pulse Width High | 1.5 | – | ns |
| tclkmpwl | Clock Minimum pulse Width Low | 1.5 | – | ns |
| tplcy | Pipelined Clock Period | 3.333 | – | ns |
| tplclkmpwh | Pipelined Clock Minimum Pulse Width High | 1.5 | – | ns |

***Table 124 •*** **RAM1K18 – Two-Port Mode for Depth × Width Configuration 512x36**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V**

| Parameter | Description | Speed Grade –1 | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| tcy | Clock Period | 3.333 | – | ns |
| tclkmpwh | Clock Minimum Pulse Width High | 1.5 | – | ns |
| tclkmpwl | Clock Minimum pulse Width Low | 1.5 | – | ns |
| tplcy | Pipelined Clock Period | 3.333 | – | ns |
| tplclkmpwh | Pipelined Clock Minimum Pulse Width High | 1.5 | – | ns |
| tplclkmpwl | Pipelined Clock Minimum pulse Width Low | 1.5 | – | ns |
| tclk2q | Read Access Time with Pipeline Register | – | 0.346 | ns |
| | Read Access Time without Pipeline Register | – | 2.322 | ns |
| taddrsu | Address Setup Time | 0.323 | – | ns |
| taddrhd | Address Hold Time | 0.282 | – | ns |
| tdsu | Data Setup Time | 0.348 | – | ns |
| tdhd | Data Hold Time | 0.114 | – | ns |
| tblksu | Block Select Setup Time | 0.214 | – | ns |
| tblkhd | Block Select Hold Time | 0.208 | – | ns |
| tblk2q | Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | – | 2.322 | ns |
| tblkmpw | Block Select Minimum Pulse Width | 0.218 | – | ns |
| trdesu | Read Enable Setup Time | 0.463 | – | ns |
| trdehd | Read Enable Hold Time | 0.173 | – | ns |
| trdplesu | Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN) | 0.256 | – | ns |
| trdplehd | Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN) | 0.106 | – | ns |
| tr2q | Asynchronous Reset to Output Propagation Delay | – | 1.561 | ns |
| trstrem | Asynchronous Reset Removal Time | 0.522 | – | ns |
| trstrec | Asynchronous Reset Recovery Time | 0.005 | – | ns |
| trstmpw | Asynchronous Reset Minimum Pulse Width | 0.352 | – | ns |
| tplrstrem | Pipelined Register Asynchronous Reset Removal Time | -0.288 | – | ns |
| tplrstrec | Pipelined Register Asynchronous Reset Recovery Time | 0.338 | – | ns |
| tplrstmpw | Pipelined Register Asynchronous Reset Minimum Pulse Width | 0.33 | – | ns |
| tsrstsu | Synchronous Reset Setup Time | 0.233 | – | ns |
| tsrsthd | Synchronous Reset Hold Time | 0.037 | – | ns |
| twesu | Write Enable Setup Time | 0.402 | – | ns |

**Table 124 • RAM1K18 – Two-Port Mode for Depth × Width Configuration 512x36**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V (continued)**

| Parameter | Description | Speed Grade –1 | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| twehd | Write Enable Hold Time | 0.25 | – | ns |
| Fmax | Maximum Frequency | – | 300 | MHz |

## 11.2 FPGA Fabric Micro SRAM (uSRAM)

**Table 125 • uSRAM (RAM64x18) in 64x18 Mode**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V**

| Parameter | Description | Speed Grade –1 | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| tcy | Read Clock Period | 4 | – | ns |
| tclkmpwh | Read Clock Minimum Pulse Width High | 1.8 | – | ns |
| tclkmpwl | Read Clock Minimum pulse Width Low | 1.8 | – | ns |
| tplcy | Read Pipe-line clock period | 4 | – | ns |
| tplclkmpwh | Read Pipe-line clock Minimum Pulse Width High | 1.8 | – | ns |
| tplclkmpwl | Read Pipe-line clock Minimum Pulse Width Low | 1.8 | – | ns |
| tclk2q | Read Access Time with Pipeline Register | – | 0.276 | ns |
| | Read Access Time without Pipeline Register | – | 1.738 | ns |
| taddrsu | Read Address Setup Time in Synchronous Mode | 0.311 | – | ns |
| | Read Address Setup Time in Asynchronous Mode | 1.916 | – | ns |
| taddrhd | Read Address Hold Time in Synchronous Mode | 0.094 | – | ns |
| | Read Address Hold Time in Asynchronous Mode | -0.803 | – | ns |
| trdensu | Read Enable Setup Time | 0.287 | – | ns |
| trdenhd | Read Enable Hold Time | 0.059 | – | ns |
| tblksu | Read Block Select Setup Time | 1.898 | – | ns |
| tblkhd | Read Block Select Hold Time | -0.671 | – | ns |
| tblk2q | Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | – | 2.102 | ns |
| trstrem | Read Asynchronous Reset Removal Time (Pipelined Clock) | -0.15 | – | ns |
| | Read Asynchronous Reset Removal Time (Non-Pipelined Clock) | 0.047 | – | ns |
| trstrec | Read Asynchronous Reset Recovery Time (Pipelined Clock) | 0.524 | – | ns |
| | Read Asynchronous Reset Recovery Time (Non-Pipelined Clock) | 0.244 | – | ns |
| tr2q | Read Asynchronous Reset to Output Propagation Delay (with Pipe-Line Register Enabled) | – | 0.869 | ns |

***Table 130 •*** **uSRAM (RAM512x2) in 512x2 Mode**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V (continued)**

| Parameter | Description | Speed Grade –1 | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| tclkmpwl | Read Clock Minimum pulse Width Low | 1.8 | – | ns |
| tplcy | Read Pipe-line clock period | 4 | – | ns |
| tplclkmpwh | Read Pipe-line clock Minimum Pulse Width High | 1.8 | – | ns |
| tplclkmpwl | Read Pipe-line clock Minimum Pulse Width Low | 1.8 | – | ns |
| tclk2q | Read Access Time with Pipeline Register | – | 0.276 | ns |
| | Read Access Time without Pipeline Register | – | 1.824 | ns |
| taddrsu | Read Address Setup Time in Synchronous Mode | 0.311 | – | ns |
| | Read Address Setup Time in Asynchronous Mode | 2.023 | – | ns |
| taddrhd | Read Address Hold Time in Synchronous Mode | 0.141 | – | ns |
| | Read Address Hold Time in Asynchronous Mode | -0.599 | – | ns |
| trdensu | Read Enable Setup Time | 0.287 | – | ns |
| trdenhd | Read Enable Hold Time | 0.059 | – | ns |
| tblksu | Read Block Select Setup Time | 1.898 | – | ns |
| tblkhd | Read Block Select Hold Time | -0.671 | – | ns |
| tblk2q | Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | – | 2.219 | ns |
| trstrem | Read Asynchronous Reset Removal Time (Pipelined Clock) | -0.15 | – | ns |
| | Read Asynchronous Reset Removal Time (Non-Pipelined Clock) | 0.047 | – | ns |
| trstrec | Read Asynchronous Reset Recovery Time (Pipelined Clock) | 0.524 | – | ns |
| | Read Asynchronous Reset Recovery Time (Non-Pipelined Clock) | 0.244 | – | ns |
| tr2q | Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled) | – | 0.862 | ns |
| tsrstsu | Read Synchronous Reset Setup Time | 0.279 | – | ns |
| tsrsthd | Read Synchronous Reset Hold Time | 0.062 | – | ns |
| tccy | Write Clock Period | 4 | – | ns |
| tcclkmpwh | Write Clock Minimum Pulse Width High | 1.8 | – | ns |
| tcclkmpwl | Write Clock Minimum Pulse Width Low | 1.8 | – | ns |
| tblkcsu | Write Block Setup Time | 0.417 | – | ns |
| tblkchd | Write Block Hold Time | 0.007 | – | ns |
| tdincsu | Write Input Data setup Time | 0.104 | – | ns |
| tdinchd | Write Input Data hold Time | 0.142 | – | ns |
| taddrcsu | Write Address Setup Time | 0.091 | – | ns |

# 12. Embedded NVM (eNVM) Characteristics

***Table 132 •*** **eNVM Read Performance**
**Worst-Case Conditions: VDD = 1.14 V, VPPNVM = VPP = 2.375 V**

| Symbol | Description | Operating Temperature Range | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| $T_j$ | Junction Temperature Range | -55°C to 125°C | | -40°C to 100°C | | 0°C to 85°C | | °C |
| Speed grade | | -1 | Std | -1 | Std | -1 | Std | – |
| $F_{MAXREAD}$ | eNVM Maximum Read Frequency | 25 | 25 | 25 | 25 | 25 | 25 | MHz |

***Table 133 •*** **eNVM Page Programming**
**Worst-Case Conditions: VDD = 1.14 V, VPPNVM = VPP = 2.375 V**

| Symbol | Description | Operating Temperature Range | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| $T_j$ | Junction Temperature Range | -55°C to 125°C | | -40°C to 100°C | | 0°C to 85°C | | °C |
| Speed grade | | -1 | Std | -1 | Std | -1 | Std | – |
| $t_{PAGEPGM}$ | eNVM Page Programming Time | 40 | 40 | 40 | 40 | 40 | 40 | ms |

# 13. Crystal Oscillator

Table 134 describes the electrical characteristics of the crystal oscillator in the IGLOO2 FPGA and SmartFusion2 SoC FPGAs.

***Table 134 •*** **Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V**

| Parameter | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| FXTAL | Operating frequency | – | 20 | – | MHz |
| ACCXTAL | Accuracy | – | – | 0.006 | % |
| CYCXTAL | Output duty cycle | – | 49-51 | 47-53 | % |
| JITPERXTAL | Output Period Jitter (peak to peak) | – | 200 | 300 | ps |
| JITCYCXTAL | Output Cycle to Cycle Jitter (peak to peak) | – | 200 | 550 | ps |
| IDYNXTAL | Operating current | – | 1.5 | – | mA |
| VIHXTAL | Input logic level High | 0.9 × VPP | – | – | V |
| VILXTAL | Input logic level Low | – | – | 0.1 × VPP | V |
| SUXTAL | Startup time (with regard to stable oscillator output) | – | – | 1 | ms |

***Table 135 •*** **Electrical Characteristics of the Crystal Oscillator – Medium Gain Mode (2 MHz)**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V**

| Parameter | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| FXTAL | Operating frequency | – | 2 | – | MHz |
| ACCXTAL | Accuracy | – | – | 0.003 | % |
| CYCXTAL | Output duty cycle | – | 49–51 | 47–53 | % |
| JITPERXTAL | Output Period Jitter (peak to peak) | – | 1 | 5 | ns |
| JITCYCXTAL | Output Cycle to Cycle Jitter (peak to peak) | – | 1 | 5 | ns |
| IDYNXTAL | Operating current | – | 0.3 | – | mA |
| VIHXTAL | Input logic level High | 0.9 × VPP | – | – | V |
| VILXTAL | Input logic level Low | – | – | 0.1 × VPP | V |
| SUXTAL | Startup time (with regard to stable oscillator output) | – | – | 4.5 | ms |

***Table 136 •*** **Electrical Characteristics of the Crystal Oscillator – Low Gain Mode (32 kHz)**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V**

| Parameter | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| FXTAL | Operating frequency | – | 32 | – | kHz |
| ACCXTAL | Accuracy | – | – | 0.006 | % |
| CYCXTAL | Output duty cycle | – | 49–51 | 45.5–54.5 | % |
| JITPERXTAL | Output Period Jitter (peak to peak) | – | 150 | 300 | ns |
| JITCYCXTAL | Output Cycle to Cycle Jitter (peak to peak) | – | 150 | 300 | ns |

# 15. Clock Conditioning Circuits (CCC)

***Table 139 •*** **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification**
**Military Worst-Case Conditions: $T_J$ = 125°C, VDD = 1.14 V**

| Parameter | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Clock conditioning circuitry input frequency $f_{IN\_CCC}$ | All CCC | 1 | – | 200 | MHz | – |
| | 32 kHz Capable CCC | 0.032 | | 200 | MHz | – |
| Clock conditioning circuitry output frequency $f_{OUT\_CCC}$ | – | 0.078 | – | 400 | MHz | 1 |
| PLL VCO frequency | – | 500 | – | 1000 | MHz | 2 |
| Delay increments in programmable delay blocks | – | – | 75 | 100 | ps | – |
| Number of programmable values in each programmable delay block | – | – | – | 64 | – | – |
| Acquisition time | – | – | 70 | 100 | µs | – |
| Input Duty Cycle (Reference Clock) | Internal Feedback | | | | | |
| | 1 MHz ≤ $f_{IN\_CCC}$ ≤ 25 MHz | 10 | – | 90 | % | – |
| | 25 MHz ≤ $f_{IN\_CCC}$ ≤ 100 MHz | 25 | – | 75 | % | – |
| | 100 MHz ≤ $f_{IN\_CCC}$ ≤ 150 MHz | 35 | – | 65 | % | – |
| | 150 MHz ≤ $f_{IN\_CCC}$ ≤ 200 MHz | 45 | – | 55 | % | – |
| | External Feedback (CCC, FPGA, Off-chip) | | | | | |
| | 1 MHz ≤ $f_{IN\_CCC}$ ≤ 25 MHz | 25 | – | 75 | % | – |
| | 25 MHz ≤ $f_{IN\_CCC}$ ≤ 35 MHz | 35 | – | 65 | % | – |
| | 35 MHz ≤ $f_{IN\_CCC}$ ≤ 50 MHz | 45 | – | 55 | % | – |
| Output duty cycle | 010, 025, and 050 Devices | 46 | – | 52 | % | – |
| | 090 and 150 Devices | 44 | – | 52 | % | – |
| **Spread Spectrum Characteristics** | | | | | | |
| Modulation frequency range | – | 25 | 35 | 50 | kHz | – |
| Modulation depth range | – | 0 | – | 1.5 | % | – |
| Modulation depth control | – | – | 0.5 | – | % | – |

*Notes:*

1. *The minimum output clock frequency is limited by the PLL. For more information refer to the UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide.*
2. *The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance will be limited by the CCC output frequency.*

## 24.3 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to Figure 17 on page 115.

***Table 160 •*** **SPI Characteristics**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V**

| Symbol | Description | Conditions | All Devices/Speed Grades | | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| sp1 | **SPI_[0\|1]_CLK minimum period** | | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | – | 12 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/4 | – | 24.1 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/8 | – | 48.2 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/16 | – | 0.1 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/32 | – | 0.19 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/64 | – | 0.39 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/128 | – | 0.77 | – | – | µs | – |
| sp2 | **SPI_[0\|1]_CLK minimum pulse width high** | | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | – | 6 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/4 | – | 12.05 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/8 | – | 24.1 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/16 | – | 0.05 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/32 | – | 0.095 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/64 | – | 0.195 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/128 | – | 0.385 | – | – | µs | – |
| sp3 | **SPI_[0\|1]_CLK minimum pulse width low** | | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | – | 6 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/4 | – | 12.05 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/8 | – | 24.1 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/16 | – | 0.05 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/32 | – | 0.095 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/64 | – | 0.195 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/128 | – | 0.385 | – | – | µs | – |

*Notes:*

1. *For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.*

***Table 160 •*** **SPI Characteristics**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V (continued)**

| Symbol | Description | Conditions | All Devices/Speed Grades | | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| sp4 | SPI_[0\|1]_CLK, SPI_[0\|1]_DO, SPI_[0\|1]_SS rise time (10%-90%) | IO Configuration: LVCMOS 2.5 V - 8mA<br>AC Loading: 35pF<br>Test Conditions: Typical Voltage, 25°C | – | 2.77 | – | ns | 1 |
| sp5 | SPI_[0\|1]_CLK, SPI_[0\|1]_DO, SPI_[0\|1]_SS fall time (10%-90%) | IO Configuration: LVCMOS 2.5 V - 8mA<br>AC Loading: 35pF<br>Test Conditions: Typical Voltage, 25°C | – | 2.906 | – | ns | 1 |
| **SPI Master Configuration** | | | | | | | |
| sp6m | SPI_[0\|1]_DO setup time | – | (SPI_x_CLK_period/2) – 3.0 | – | – | ns | 2 |
| sp7m | SPI_[0\|1]_DO hold time | – | (SPI_x_CLK_period/2) – 2.5 | – | – | ns | 2 |
| sp8m | SPI_[0\|1]_DI setup time | – | 8 | – | – | ns | 2 |
| sp9m | SPI_[0\|1]_DI hold time | – | 2.5 | – | – | ns | 2 |
| **SPI Slave Configuration** | | | | | | | |
| sp6s | SPI_[0\|1]_DO setup time | – | (SPI_x_CLK_period/2) – 12.0 | – | – | ns | 2 |
| sp7s | SPI_[0\|1]_DO hold time | – | (SPI_x_CLK_period/2) + 3.0 | – | – | ns | 2 |
| sp8s | SPI_[0\|1]_DI setup time | – | 2 | – | – | ns | 2 |
| sp9s | SPI_[0\|1]_DI hold time | – | 3 | – | – | ns | 2 |

*Notes:*

1. *For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.*

# 27. IGLOO2 Specifications

## 27.1 HPMS Clock Frequency

***Table 163 •*** **Maximum Frequency for HPMS Main Clock**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V**

| Symbol | Description | Speed Grade –1 | Units |
|---|---|---|---|
| HPMS_CLK | Maximum Frequency for the HPMS Main Clock (FCLK) | 133 | MHz |

## 27.2 IGLOO2 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_0_CLK. For timing parameter definitions, refer to Figure 18 on page 120.

***Table 164 •*** **SPI Characteristics**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V**

| Symbol | Description | Conditions | All Devices/Speed Grades | | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| sp1 | **SPI_[0\|1]_CLK minimum period** | | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | – | 12 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/4 | – | 24.1 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/8 | – | 48.2 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/16 | – | 0.1 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/32 | – | 0.19 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/64 | – | 0.39 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/128 | – | 0.77 | – | – | µs | – |
| sp2 | **SPI_[0\|1]_CLK minimum pulse width high** | | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | – | 6 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/4 | – | 12.05 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/8 | – | 24.1 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/16 | – | 0.05 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/32 | – | 0.095 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/64 | – | 0.195 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/128 | – | 0.385 | – | – | µs | – |

***Table 164 •*** **SPI Characteristics**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V (continued)**

| Symbol | Description | Conditions | All Devices/Speed Grades | | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| sp9s | SPI_[0\|1]_DI hold time | – | 3 | – | – | ns | 2 |

*Notes:*

1. *For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.*

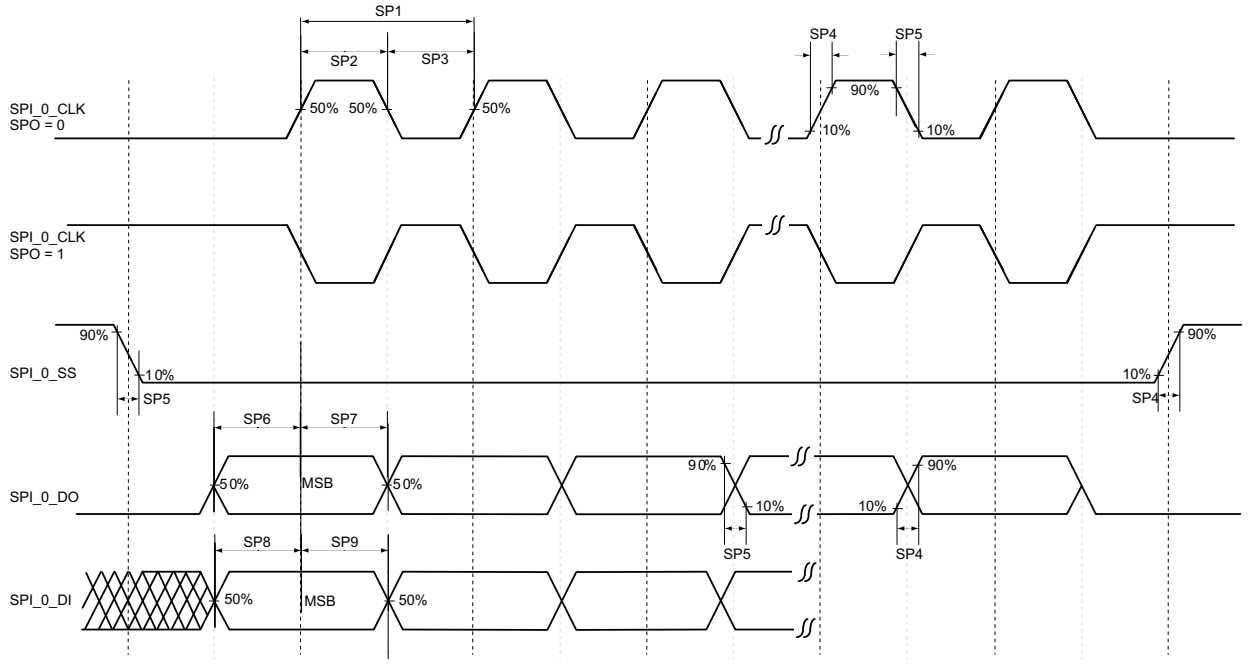


***Figure 18 •*** **SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**

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