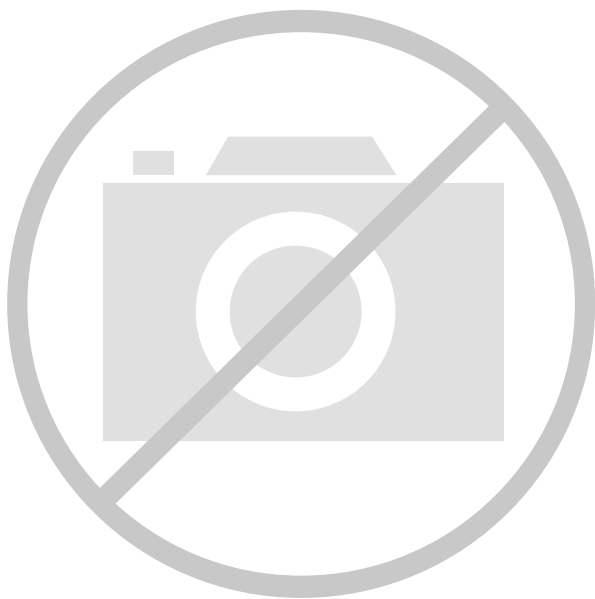




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	86184
Total RAM Bits	2648064
Number of I/O	267
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl090t-1fgg484m

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Table 10 • SmartFusion2 and IGLOO2 Quiescent Supply Current – Worst-Case Process

Parameter	Modes	Conditions	010	025	050	090	150	Units
			VDD=1.26 V	VDD=1.26 V	VDD=1.26 V	VDD=1.26 V	VDD=1.26 V	
IDC1	Non-Flash*Freeze	Military (T _J = 125°C)	151.5	227.4	358.9	443.1	660.4	mA
IDC2	Flash*Freeze	Military (T _J = 125°C)	127.2	144.2	174.6	195.0	236.3	mA

5.2 Programming Currents

The tables below represent programming, verify and Inrush currents for SmartFusion2 SoC and IGLOO2 FPGA devices.

Table 11 • Currents During Program Cycle, 0°C ≤ T_J ≤ 85°C, Typical Process

Power Supplies	Voltage (V)	010	025	050	090	150	Units	Notes
VDD	1.26	53	55	58	42	52	mA	–
VPP	3.46	11	6	10	12	12	mA	–
VPPNVM	3.46	2	2	3	3	–	mA	*
VDDI	2.62	16	17	1	12	81	mA	**
	3.46	31	36	1	17	84	mA	**
Number of banks		8	8	10	9	19	–	–
Notes: * VPP and VPPNVM are internally shorted. ** The current for 050 represents JTAG I/O Bank only.								

Table 12 • Currents During Verify Cycle, 0°C ≤ T_J ≤ 85°C, Typical Process

Power Supplies	Voltage (V)	010	025	050	090	150	Units	Notes
VDD	1.26	53	55	58	41	51	mA	–
VPP	3.46	5	3	15	11	12	mA	–
VPPNVM	3.46	0	0	1	1	–	mA	*
VDDI	2.62	16	17	1	11	81	mA	**
	3.46	32	36	1	17	84	mA	**
Number of banks		8	8	10	9	19	–	–
Notes: * VPP and VPPNVM are internally shorted. ** The current for 050 represents JTAG I/O Bank only.								

Table 13 • Inrush Currents at Power up, –55°C ≤ T_J ≤ 125°C, Typical Process

Power Supplies	Voltage (V)	010	025	050	090	150	Units
VDD	1.26	53	78	57	98	140	mA
VPP	3.46	57	50	180	36	51	mA

Table 13 • Inrush Currents at Power up, $-55^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$, Typical Process

VDDI	2.62	141	161	187	283	404	mA
Number of banks		8	8	10	9	19	–

6. Average Fabric Temperature and Voltage Derating Factors

Table 14 • Average Temperature and Voltage Derating Factors for Fabric Timing Delays
(Normalized to $T_J = 125^{\circ}\text{C}$, Worst-Case VDD = 1.14 V)

Core Voltage VDD (V)	Junction Temperature ($^{\circ}\text{C}$)							
	-55°C	-40°C	0°C	25°C	70°C	85°C	100°C	125°C
1.14	0.91	0.91	0.93	0.94	0.96	0.97	0.98	1.00
1.2	0.82	0.83	0.84	0.85	0.87	0.87	0.88	0.90
1.26	0.75	0.75	0.77	0.77	0.79	0.80	0.81	0.75

8.4 I/O Speeds

Table 16 • Maximum Data Rate Summary for Worst-Case Military Conditions

Single-Ended I/O	MSIO	MSIOD	DDRIO	Units
PCI 3.3 V	560	–	–	Mbps
LVTTL 3.3 V	540	–	–	Mbps
LVC MOS 3.3 V	540	–	–	Mbps
LVC MOS 2.5 V	360	370	360	Mbps
LVC MOS 1.8 V	260	360	360	Mbps
LVC MOS 1.5 V	140	190	210	Mbps
LVC MOS 1.2 V	100	140	180	Mbps
LPDDR – LVC MOS 1.8 V Mode	–	–	360	Mbps
Voltage-Referenced I/O	MSIO	MSIOD	DDRIO	Units
LPDDR	–	–	360	Mbps
HSTL 1.5 V	–	–	360	Mbps
SSTL 2.5 V	450	480	360	Mbps
SSTL 1.8 V	–	–	600	Mbps
Voltage-Referenced I/O	MSIO	MSIOD	DDRIO	Units
SSTL 1.5 V	–	–	600	Mbps
Differential I/O	MSIO	MSIOD	DDRIO	Units
LVPECL (input only)	810	–	–	Mbps
LVDS 3.3 V	480	480	–	Mbps
LVDS 2.5 V	480	480	–	Mbps
RSDS	460	480	–	Mbps
BLVDS	450	–	–	Mbps
MLVDS	450	–	–	Mbps
Mini-LVDS	460	480	–	Mbps

8.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

8.6.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 21 • LVTTL/LVCMOS 3.3 V DC Voltage Specification (Applicable to MSIO I/O Bank Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units	Notes
LVTTL/LVCMOS 3.3 V Recommended DC Operating Conditions							
VDDI	Supply voltage		3.15	3.3	3.45	V	–
LVTTL/LVCMOS 3.3 V DC Input Voltage Specification							
VIH (DC)	DC input logic High		2.0	–	3.45	V	–
VIL (DC)	DC input logic Low		–0.3	–	0.8	V	–
IIH (DC)	Input current High		–	–	10	μA	–
IIL (DC)	Input current Low		–	–	10	μA	–
LVCMOS 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		2.4	–	–	V	*
VOL	DC output logic Low		–	–	0.4	V	*
LVTTL 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		2.4	–	–	V	–
VOL	DC output logic Low		–	–	0.4	V	–
Note: * The VOH/VOL test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.							

Table 22 • LVTTL/LVCMOS 3.3 V Maximum Switching Speeds (Applicable to MSIO I/O Bank Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
LVTTL/LVCMOS 3.3 V Maximum Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	540	Mbps

Table 23 • LVTTL/LVCMOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO Bank Only)

LVTTL/LVCMOS 3.3 V AC Test Parameter Specifications						
Symbol	Parameters	Conditions	Min	Typ	Max	Units
Vtrip	Measuring/trip point for data path		–	1.4	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

8.6.5.2. AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 44 • LVCMOS 1.5 V AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Military Conditions: $T_J=125^{\circ}\text{C}$, $V_{DD}=1.14\text{ V}$, $V_{DDI}=1.425\text{ V}$

	ODT (On Die Termination)	Speed Grade -1		Units
		t_{PV}	t_{PVS}	
LVCMOS 1.5 V (for DDRIO I/O Bank with Fixed Codes)	none	2.19	2.216	ns
LVCMOS 1.5 V (for MSIO I/O Bank)	none	3.679	3.652	ns
	50	4.151	4.126	ns
	75	3.984	3.953	ns
	150	3.823	3.791	ns
LVCMOS 1.5 V (for MSIOD I/O Bank)	none	3.262	3.229	ns
	50	3.76	3.739	ns
	75	3.555	3.52	ns
	150	3.395	3.359	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 45 • LVCMOS 1.5 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-Case Military Conditions: $T_J=125^{\circ}\text{C}$, $V_{DD}=1.14\text{ V}$, $V_{DDI}=1.425\text{ V}$

Output Drive Selection	Slew Control	Speed Grade -1					Units
		t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
LVCMOS 1.5 V (for DDRIO I/O Bank with Fixed Codes)							
2 mA	slow	5.712	4.796	5.735	5.814	5.138	ns
	medium	5.094	4.274	5.114	5.484	4.779	ns
	medium_fast	4.793	4.013	4.81	5.288	4.625	ns
	fast	4.762	3.98	4.78	5.261	4.615	ns
4 mA	slow	4.966	4.133	4.956	6.763	6.05	ns
	medium	4.412	3.62	4.401	6.433	5.664	ns
	medium_fast	4.145	3.358	4.131	6.249	5.507	ns
	fast	4.116	3.338	4.103	6.238	5.498	ns
6 mA	slow	4.744	3.869	4.728	7.173	6.383	ns
	medium	4.212	3.382	4.195	6.837	6.004	ns
	medium_fast	3.951	3.135	3.93	6.668	5.861	ns
	fast	3.919	3.11	3.899	6.644	5.845	ns

Table 46 • LVCMOS 1.2 V Minimum and Maximum DC Input and Output Levels

IIL (DC)	Input current Low	–	–	10	μA
LVCMOS 1.2 V DC Output Voltage Specification					
VOH	DC output logic High	–	VDDI × 0.75	–	V
VOL	DC output logic Low	–	–	VDDI × 0.25	V

Table 47 • LVCMOS 1.2 V Maximum AC Switching Speeds

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 1.2 V Maximum AC Switching Speed						
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	180	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	100	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	140	Mbps

Table 48 • LVCMOS 1.2 V AC Calibrated Impedance and Test Parameters Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 1.2 V AC Calibrated Impedance Option						
Rodt_cal	Supported output driver calibrated impedance (for DDRIO I/O Bank)		–	75, 60, 50, 40	–	Ω
LVCMOS 1.2 V AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	0.6	–	V
Rent	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF
Cload	Capacitive loading for data path (t _{DP})		–	5	–	pF

Table 49 • LVCMOS 1.2 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (with Fixed Code)	Min	Max		
2 mA	2 mA	2 mA	VDDI × 0.75	VDDI × 0.25	2	2
4 mA	4 mA	4 mA	VDDI × 0.75	VDDI × 0.25	4	4
N/A	N/A	6 mA	VDDI × 0.75	VDDI × 0.25	6	6

8.7.3.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 62 • DDR1/SSTL2 AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	ODT (On Die Termination)	Speed Grade -1	Units
		t _{py}	
SSTL2 (DDRIO I/O Bank)			
Pseudo-Differential	None	1.613	ns
True-Differential	None	1.647	ns
SSTL2 (MSIO I/O Bank)			
Pseudo-Differential	None	3.083	ns
True-Differential	None	3.028	ns
SSTL2 (MSIOD I/O Bank)			
Pseudo-Differential	None	2.721	ns
True-Differential	None	2.71	ns

Table 63 • DDR1/SSTL2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	Speed Grade -1					Units
	t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
SSTL2 Class I						
DDRIO I/O Bank						
Single Ended	2.457	2.145	2.137	2.302	2.293	ns
Differential	2.454	2.38	2.375	2.589	2.584	ns
MSIO I/O Bank						
Single Ended	2.283	2.255	2.243	2.286	2.273	ns
Differential	2.434	2.702	2.691	2.39	2.381	ns
MSIOD I/O Bank						
Single Ended	1.646	1.59	1.589	1.82	1.818	ns
Differential	1.774	1.93	1.926	2.012	2.007	ns
SSTL2 Class II						
DDRIO I/O Bank						
Single Ended	2.317	2.06	2.053	2.229	2.221	ns
Differential	2.32	2.213	2.21	2.57	2.565	ns

Table 63 • DDR1/SSTL2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$ (continued)

	Speed Grade -1					Units
	t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
MSIO I/O Bank						
Single Ended	2.563	2.208	2.19	2.205	2.187	ns
Differential	2.703	2.566	2.555	2.363	2.353	ns

8.7.4 Stub-Series Terminated Logic 1.8 V (SSTL18)

SSTL18 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR2) standard. IGLOO2 and SmartFusion2 SoC FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

8.7.4.1 Minimum and Maximum Input and Output Levels Specification

Table 64 • DDR2/SSTL18 AC/DC Minimum and Maximum Input and Output Levels Specification

Symbols	Parameters	Conditions	Min	Typ	Max	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.71	1.8	1.89	V	–
VTT	Termination voltage		0.838	0.900	0.964	V	–
VREF	Input reference voltage		0.838	0.900	0.964	V	–
SSTL18 DC Input Voltage Specification							
VIH (DC)	DC input logic High		$V_{REF} + 0.125$	–	1.89	V	–
VIL (DC)	DC input logic Low		–0.3	–	$V_{REF} - 0.125$	V	–
IIH (DC)	Input current High		–	–	10	μA	–
IIL (DC)	Input current Low		–	–	10	μA	–
SSTL18 DC Output Voltage Specification							
SSTL18 Class I (DDR2 Reduced Drive)							
VOH	DC output logic High		$V_{TT} + 0.603$	–	–	V	–
VOL	DC output logic Low		–	–	$V_{TT} - 0.603$	V	–
IOH at VOH	Output minimum source DC current (DDRIO I/O Bank only)		6.0	–	–	mA	–
IOL at VOL	Output minimum sink current (DDRIO I/O Bank only)		–6.0	–	–	mA	–
SSTL18 Class II (DDR2 Full Drive)							
VOH	DC output logic High		$V_{TT} + 0.603$	–	–	V	–
VOL	DC output logic Low		–	–	$V_{TT} - 0.603$	V	–
IOH at VOH	Output minimum source DC current (DDRIO I/O Bank only)		12.0	–	–	mA	–
Note: *To meet JEDEC Electrical Compliance, use DDR2 Full Drive Transmitter.							*

8.7.5.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 70 • DDR3/SSTL15 AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.425\text{ V}$

	ODT (On Die Termination)	Speed Grade -1	Units
		t _{py}	
DDR3/SSTL15 (for DDRIO I/O Bank) – Calibration Mode Only			
Pseudo-Differential	None	1.672	ns
True-Differential	None	1.694	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 71 • DDR3/SSTL15 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.425\text{ V}$

	Speed Grade –1					Units
	t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
DDR3 Reduced Drive/SSTL15 Class I (for DDRIO I/O Bank)						
Single Ended	2.832	2.766	2.767	2.658	2.659	ns
Differential	2.848	3.401	3.393	3.173	3.166	ns
DDR3 Full Drive/SSTL15 Class II (for DDRIO I/O Bank)						
Single Ended	2.832	2.76	2.759	2.655	2.655	ns
Differential	2.845	3.397	3.387	3.179	3.171	ns

8.7.6 Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer. This I/O standard is supported in DDRIO I/O Bank only.

8.7.6.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 72 • LPDDR AC/DC Specifications (for DDRIO IO Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.71	1.8	1.89	V	–
VTT	Termination voltage		0.838	0.900	0.964	V	–
VREF	Input reference voltage		0.838	0.900	0.964	V	–
LPDDR DC Input Voltage Specification							
VIH (DC)	DC input logic High		$0.7 \times V_{DDI}$	–	1.89	V	–
VIL (DC)	DC input logic Low		–0.3	–	$0.3 \times V_{DDI}$	V	–
IIH (DC)	Input current High		–	–	10	μA	–
IIL (DC)	Input current Low		–	–	10	μA	–
LPDDR DC Output Voltage Specification							

8.8.2 B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

8.8.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 89 • B-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Bus-LVDS Recommended DC Operating Conditions						
VDDI	Supply voltage		2.375	2.5	2.625	V
Bus-LVDS DC Input Voltage Specification						
VI	DC input voltage		0	–	2.925	V
IIH (DC)	Input current High		–	–	10	μA
IIL (DC)	Input current Low		–	–	10	μA
Bus-LVDS DC Output Voltage Specification (for MSIO I/O Bank only)						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
Bus-LVDS Differential Voltage Specification						
VOD	Differential output voltage swing (for MSIO I/O Bank only)		65	–	460	mV
VOCM	Output common mode voltage (for MSIO I/O Bank only)		1.1	–	1.5	V
VICM	Input common mode voltage		0.05	–	2.4	V
VID	Input differential voltage		0.1	–	VDDI	V

Table 90 • B-LVDS AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Bus-LVDS Maximum AC Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	450	Mbps
Bus-LVDS Impedance Specifications						
Rt	Termination resistance		–	27	–	Ω
Bus-LVDS AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF

8.8.5.2. AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 103 • RSDS AC Switching Characteristics for Receiver (Input Buffers)

Worst-case Military conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	On-Die Termination (ODT)	Speed Grade -1	Units
		t_{PY}	
RSDS (for MSIO I/O Bank)	None	3.112	ns
	100	3.108	ns
RSDS (for MSIOD I/O Bank)	None	2.832	ns
	100	2.821	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 104 • RSDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-case Military conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	Speed Grade -1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
RSDS (for MSIO I/O Bank)	2.256	2.484	2.472	2.111	2.096	ns
RSDS (for MSIOD I/O Bank)						
No pre-emphasis	1.661	1.648	1.645	1.675	1.665	ns
Min pre-emphasis	1.651	1.84	1.833	1.988	1.964	ns
Med pre-emphasis	1.577	1.868	1.859	2.019	1.993	ns
Max pre-emphasis	1.555	1.894	1.883	2.047	2.018	ns

8.8.6 LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO2 and SmartFusion2 SoC FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

8.8.6.1 Minimum and Maximum Input and Output Levels

Table 105 • LVPECL DC Voltage Specification (Applicable to MSIO I/O Banks Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
V_{DDI}	Supply voltage		3.15	3.3	3.45	V
LVPECL DC Input Voltage Specification						
V_I	DC input voltage		0	—	3.45	V
LVPECL Differential Voltage Specification						
V_{ICM}	Input common mode voltage		0.3		2.8	V
V_{DIFF}	Input differential voltage		100	300	1,000	mV

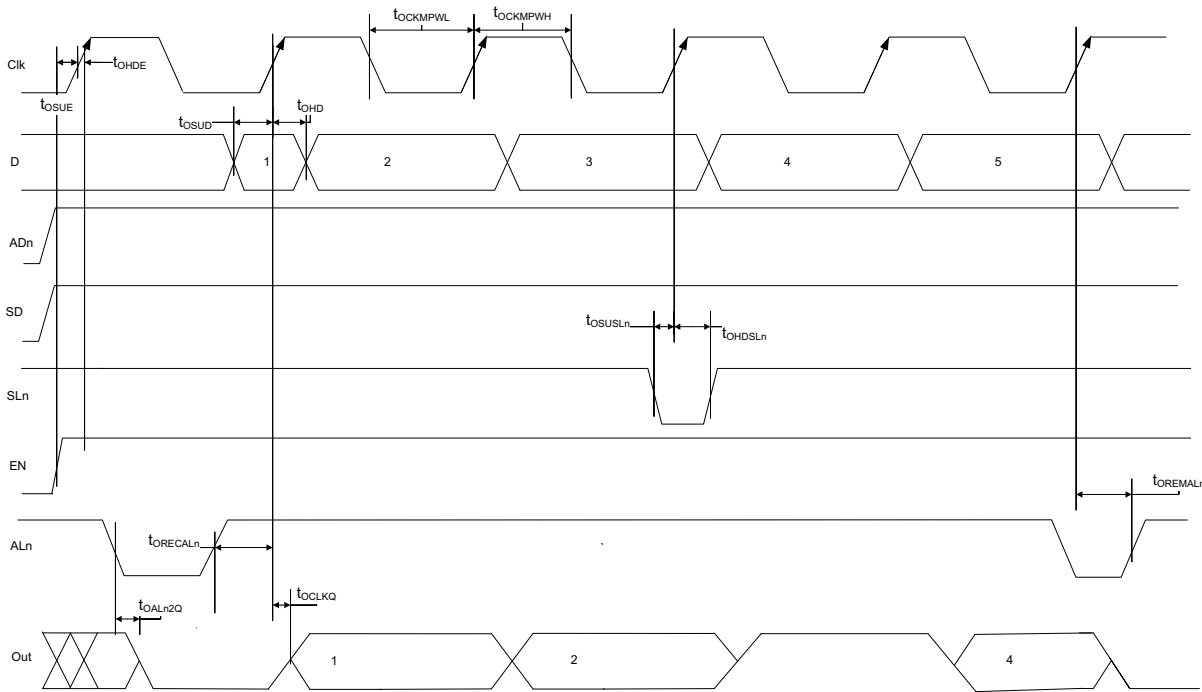


Figure 8 • I/O Register Output Timing Diagram

Table 109 • Output/Enable Data Register Propagation Delays
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Measuring Nodes (from, to)*	Speed Grade -1	Units
tOBYP	Bypass Delay of the Output/Enable Register	F,G or H,I	0.364	ns
tOCLKQ	Clock-to-Q of the Output/Enable Register	E,G or E,I	0.272	ns
tOSUD	Data Setup Time for the Output/Enable Register	A,E or J,E	0.196	ns
tOHD	Data Hold Time for the Output/Enable Register	A,E or J,E	0	ns
tOSUE	Enable Setup Time for the Output/Enable Register	B,E	0.433	ns
tOHE	Enable Hold Time for the Output/Enable Register	B,E	0	ns
tOSUSL	Synchronous Load Setup Time for the Output/Enable Register	D,E	0.203	ns
tOHSL	Synchronous Load Hold Time for the Output/Enable Register	D,E	0	ns
tOALn2Q	Asynchronous Clear-to-Q of the Output/Enable Register (ADn=1)	C,G or C,I	0.523	ns
	Asynchronous Preset-to-Q of the Output/Enable Register (ADn=0)	C,G or C,I	0.545	ns
tOREMALn	Asynchronous Load Removal Time for the Output/Enable Register	C,E	0	ns

Table 121 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4Kx4
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade –1		
		Min	Max	Units
trdesu	Read Enable Setup Time	0.532	–	ns
trdehd	Read Enable Hold Time	0.073	–	ns
trdple su	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
trdplehd	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
tr2q	Asynchronous Reset to Output Propagation Delay	–	1.562	ns
trstrem	Asynchronous Reset Removal Time	0.522	–	ns
trstrec	Asynchronous Reset Recovery Time	0.005	–	ns
trstmpw	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
tplrstrem	Pipelined Register Asynchronous Reset Removal Time	-0.288	–	ns
tplrstrec	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
tplrstmpw	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
tsrst su	Synchronous Reset Setup Time	0.233	–	ns
tsrsthd	Synchronous Reset Hold Time	0.037	–	ns
twesu	Write Enable Setup Time	0.473	–	ns
twehd	Write Enable Hold Time	0.05	–	ns
Fmax	Maximum Frequency	–	300	MHz

Table 122 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8Kx2
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tcy	Clock Period	3.333	–	ns
tclkmpwh	Clock Minimum Pulse Width High	1.5	–	ns
tclkmpwl	Clock Minimum pulse Width Low	1.5	–	ns
tpcy	Pipelined Clock Period	3.333	–	ns
tpclkmpwh	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
tpclkmpwl	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.332	ns
	Read Access Time without Pipeline Register	–	2.346	ns
	Access Time with Feed-Through Write Timing	–	1.56	ns
taddr su	Address Setup Time	0.631	–	ns
taddrhd	Address Hold Time	0.282	–	ns

Table 125 • uSRAM (RAM64x18) in 64x18 Mode
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
tsrstu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsth	Read Synchronous Reset Hold Time	0.062	–	ns
tccy	Write Clock Period	4	–	ns
tcclkmpwh	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclkmpwl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblkcsu	Write Block Setup Time	0.417	–	ns
tblkchd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.119	–	ns
tdinchd	Write Input Data hold Time	0.155	–	ns
taddrcsu	Write Address Setup Time	0.091	–	ns
taddrchd	Write Address Hold Time	0.132	–	ns
twecsu	Write Enable Setup Time	0.41	–	ns
twechd	Write Enable Hold Time	-0.027	–	ns
fmax	Maximum Frequency	–	250	MHz

Table 126 • uSRAM (RAM64x16) in 64x16 Mode
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
tcy	Read Clock Period	4	–	ns
tclcmpwh	Read Clock Minimum Pulse Width High	1.8	–	ns
tclcmpwl	Read Clock Minimum pulse Width Low	1.8	–	ns
tpcy	Read Pipe-line clock period	4	–	ns
tpclcmpwh	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
tpclcmpwl	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.738	ns
taddrsu	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	1.916	–	ns
taddrhd	Read Address Hold Time in Synchronous Mode	0.094	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.803	–	ns
trdensu	Read Enable Setup Time	0.287	–	ns

Table 126 • uSRAM (RAM64x16) in 64x16 Mode
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
trdenhd	Read Enable Hold Time	0.059	–	ns
tblksu	Read Block Select Setup Time	1.898	–	ns
tblkhd	Read Block Select Hold Time	-0.671	–	ns
tblk2q	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.102	ns
trstrem	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
trstrec	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
tr2q	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.866	ns
tsrstsu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.062		ns
tccy	Write Clock Period	4	–	ns
tcclkmpwh	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclkmpwl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblkcsu	Write Block Setup Time	0.417	–	ns
tblkchd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.119	–	ns
tdinchd	Write Input Data hold Time	0.155	–	ns
taddrcsu	Write Address Setup Time	0.091	–	ns
taddrchd	Write Address Hold Time	0.132	–	ns
twecsu	Write Enable Setup Time	0.41	–	ns
twechd	Write Enable Hold Time	-0.027	–	ns
fmax	Maximum Frequency	–	250	MHz

Table 127 • uSRAM (RAM128x9) in 128x9 Mode
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
tcy	Read Clock Period	4	–	ns
tcclkmpwh	Read Clock Minimum Pulse Width High	1.8	–	ns

15. Clock Conditioning Circuits (CCC)

Table 139 • IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification
Military Worst-Case Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Conditions	Min	Typ	Max	Units	Notes
Clock conditioning circuitry input frequency f_{IN_CCC}	All CCC	1	–	200	MHz	–
	32 kHz Capable CCC	0.032		200	MHz	–
Clock conditioning circuitry output frequency f_{OUT_CCC}	–	0.078	–	400	MHz	1
PLL VCO frequency	–	500	–	1000	MHz	2
Delay increments in programmable delay blocks	–	–	75	100	ps	–
Number of programmable values in each programmable delay block	–	–	–	64	–	–
Acquisition time	–	–	70	100	μs	–
Input Duty Cycle (Reference Clock)	Internal Feedback					
	$1\text{ MHz} \leq f_{IN_CCC} \leq 25\text{ MHz}$	10	–	90	%	–
	$25\text{ MHz} \leq f_{IN_CCC} \leq 100\text{ MHz}$	25	–	75	%	–
	$100\text{ MHz} \leq f_{IN_CCC} \leq 150\text{ MHz}$	35	–	65	%	–
	$150\text{ MHz} \leq f_{IN_CCC} \leq 200\text{ MHz}$	45	–	55	%	–
	External Feedback (CCC, FPGA, Off-chip)					
	$1\text{ MHz} \leq f_{IN_CCC} \leq 25\text{ MHz}$	25	–	75	%	–
	$25\text{ MHz} \leq f_{IN_CCC} \leq 35\text{ MHz}$	35	–	65	%	–
	$35\text{ MHz} \leq f_{IN_CCC} \leq 50\text{ MHz}$	45	–	55	%	–
Output duty cycle	010, 025, and 050 Devices	46	–	52	%	–
	090 and 150 Devices	44	–	52	%	–
Spread Spectrum Characteristics						
Modulation frequency range	–	25	35	50	kHz	–
Modulation depth range	–	0	–	1.5	%	–
Modulation depth control	–	–	0.5	–	%	–
Notes:						
1. The minimum output clock frequency is limited by the PLL. For more information refer to the UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide.						
2. The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance will be limited by the CCC output frequency.						

21. DDR Memory Interface Characteristics

Table 150 • DDR Memory Interface Characteristics

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Standard	Supported Data Rate			Unit
	Min	Typ	Max	
DDR3	667			Mbps
DDR2	667			Mbps
LPDDR	50	–	400	Mbps

Table 164 • SPI Characteristics

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Symbol	Description	Conditions	All Devices/Speed Grades			Unit	Notes
			Min	Typ	Max		
sp9s	SPI_[0 1]_DI hold time	—	3	—	—	ns	2

Notes:

- For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website:
<http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models>.
- For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.

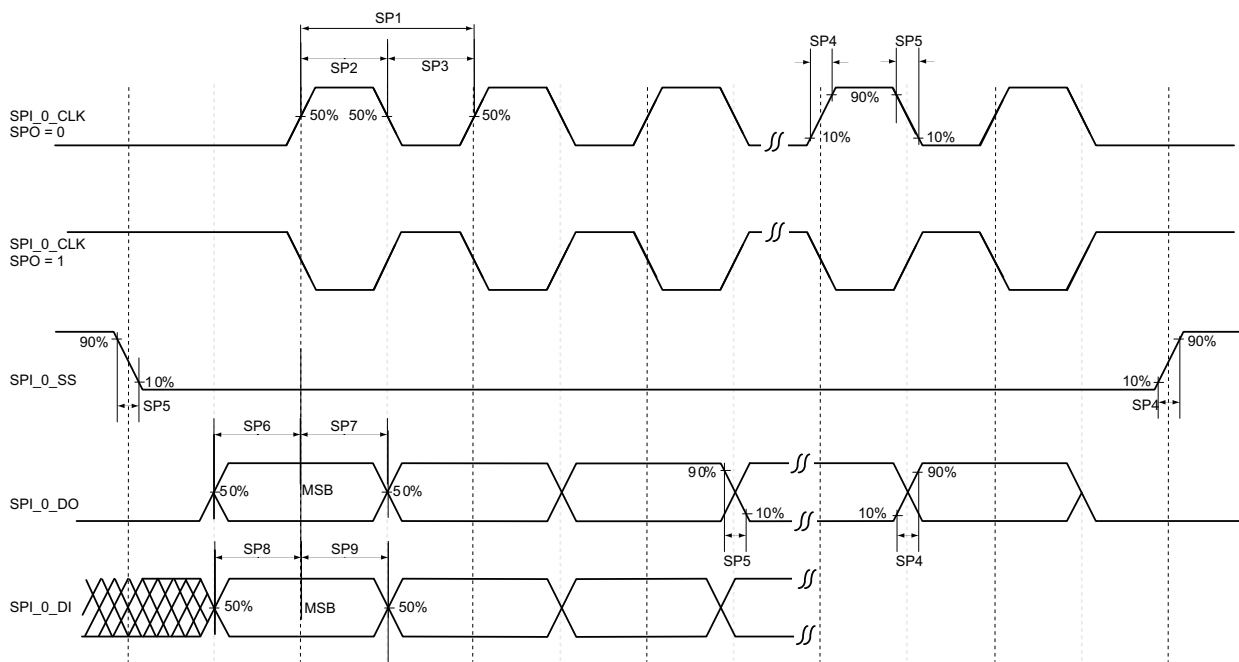


Figure 18 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)