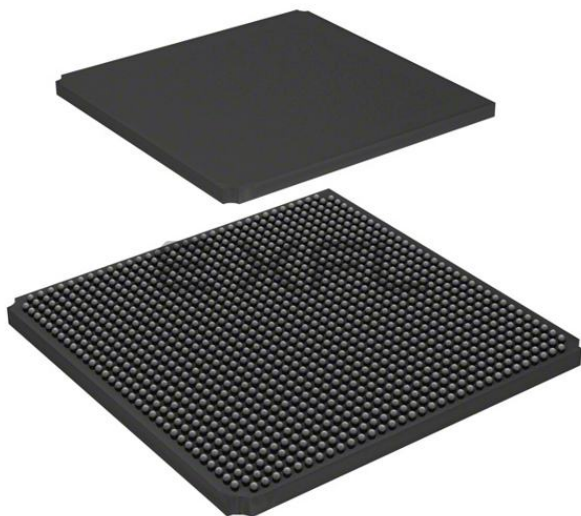




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	146124
Total RAM Bits	5120000
Number of I/O	574
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl150t-1fc1152m

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8.4 I/O Speeds

Table 16 • Maximum Data Rate Summary for Worst-Case Military Conditions

Single-Ended I/O	MSIO	MSIOD	DDRIO	Units
PCI 3.3 V	560	–	–	Mbps
LVTTL 3.3 V	540	–	–	Mbps
LVC MOS 3.3 V	540	–	–	Mbps
LVC MOS 2.5 V	360	370	360	Mbps
LVC MOS 1.8 V	260	360	360	Mbps
LVC MOS 1.5 V	140	190	210	Mbps
LVC MOS 1.2 V	100	140	180	Mbps
LPDDR – LVC MOS 1.8 V Mode	–	–	360	Mbps
Voltage-Referenced I/O	MSIO	MSIOD	DDRIO	Units
LPDDR	–	–	360	Mbps
HSTL1.5 V	–	–	360	Mbps
SSTL 2.5 V	450	480	360	Mbps
SSTL 1.8 V	–	–	600	Mbps
Voltage-Referenced I/O	MSIO	MSIOD	DDRIO	Units
SSTL 1.5 V	–	–	600	Mbps
Differential I/O	MSIO	MSIOD	DDRIO	Units
LVPECL (input only)	810	–	–	Mbps
LVDS 3.3 V	480	480	–	Mbps
LVDS 2.5 V	480	480	–	Mbps
RS DS	460	480	–	Mbps
BLVDS	450	–	–	Mbps
MLVDS	450	–	–	Mbps
Mini-LVDS	460	480	–	Mbps

8.7.4.2. AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 66 • DDR2/SSTL18 AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Military Conditions: $T_j = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.71\text{ V}$

	On-Die Termination (ODT)	Speed Grade –1	Units
		t _{PY}	
SSTL18 (for DDRIO I/O Bank with Fixed Codes)			
Pseudo differential	None	1.633	ns
True differential	None	1.65	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 67 • DDR2/SSTL18 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-Case Military Conditions: $T_j = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.71\text{ V}$

	Speed Grade –1					Units
	t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
SSTL18 Class I (for DDRIO I/O Bank)						
Single Ended	2.67	3.078	3.072	2.489	2.484	ns
Differential	2.645	2.431	2.434	2.396	2.398	ns
SSTL18 Class II (for DDRIO I/O Bank)						
Single Ended	2.564	2.973	2.965	2.45	2.444	ns
Differential	2.532	2.401	2.398	2.368	2.365	ns

8.7.5 Stub-Series Terminated Logic 1.5 V (SSTL15)

SSTL15 Class I and Class II are supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR3) standard. IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

8.7.5.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 68 • DDR3 SSTL15 DC Voltage Specification (for DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
VDDI	Supply voltage		1.425	1.5	1.575	V
VTT	Termination voltage		0.698	0.750	0.803	V
VREF	Input reference voltage		0.698	0.750	0.803	V
SSTL15 DC Input Voltage Specification						
VIH(DC)	DC input logic High		$V_{REF} + 0.1$	–	1.575	V
VIL(DC)	DC input logic Low		–0.3	–	$V_{REF} - 0.1$	V
IIH (DC)	Input current High		–	–	10	μA
IIL (DC)	Input current Low		–	–	10	μA

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 82 • LPDDR - LVCMOS 1.8 V AC Switching Characteristics for Transmitter DDRIO I/O Bank (Output and Tristate Buffers)

Worst-Case Military Conditions: $T_j = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.71\text{ V}$

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
2 mA	slow	4.681	4.017	4.69	5.388	4.852	ns
	medium	4.211	3.599	4.219	5.058	4.488	ns
	medium_fast	3.978	3.392	3.986	4.874	4.327	ns
	fast	3.953	3.373	3.961	4.858	4.316	ns
4 mA	slow	4.355	3.657	4.346	5.967	5.399	ns
	medium	3.886	3.246	3.879	5.628	5.01	ns
	medium_fast	3.656	3.05	3.647	5.461	4.845	ns
	fast	3.635	3.033	3.626	5.447	4.838	ns
6 mA	slow	4.105	3.422	4.092	6.221	5.599	ns
	medium	3.68	3.05	3.668	5.9	5.257	ns
	medium_fast	3.477	2.867	3.463	5.739	5.118	ns
	fast	3.451	2.849	3.437	5.72	5.104	ns
8 mA	slow	4.015	3.32	3.998	6.458	5.808	ns
	medium	3.59	2.947	3.574	6.129	5.449	ns
	medium_fast	3.383	2.761	3.366	5.963	5.304	ns
	fast	3.357	2.746	3.34	5.954	5.289	ns
10 mA	slow	3.888	3.18	3.864	6.739	6.045	ns
	medium	3.485	2.822	3.467	6.422	5.7	ns
	medium_fast	3.281	2.642	3.26	6.277	5.553	ns
	fast	3.258	2.627	3.238	6.27	5.546	ns
12 mA	slow	3.795	3.096	3.773	6.773	6.067	ns
	medium	3.408	2.764	3.389	6.47	5.743	ns
	medium_fast	3.215	2.599	3.194	6.346	5.61	ns
	fast	3.196	2.584	3.175	6.335	5.604	ns
16 mA	slow	3.744	3.035	3.719	6.944	6.207	ns
	medium	3.358	2.712	3.339	6.657	5.868	ns
	medium_fast	3.175	2.546	3.153	6.547	5.751	ns
	fast	3.156	2.531	3.133	6.541	5.747	ns

8.8. Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero® System-on-Chip (SoC) software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

8.8.1 LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

8.8.1.1 Minimum and Maximum Input and Output Levels

Table 83 • LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVDS Recommended DC Operating Conditions						
VDDI	Supply voltage	2.5 V range	2.375	2.5	2.625	V
VDDI	Supply voltage	3.3 V range	3.15	3.3	3.45	V
LVDS DC Input Voltage Specification						
VI	DC Input voltage	2.5 V range	0	–	2.925	V
VI	DC input voltage	3.3 V range	0	–	3.45	V
IIH (DC)	Input current High		–	–	10	μA
IIL (DC)	Input current Low		–	–	10	μA
LVDS DC Output Voltage Specification						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
LVDS Differential Voltage Specification						
VOD	Differential output voltage swing		250	350	450	mV
VOCM	Output common mode voltage		1.125	1.25	1.375	V
VICM	Input common mode voltage		0.05	1.25	2.35	V
VID	Input differential voltage		100	350	600	mV

Table 84 • LVDS AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVDS Maximum AC Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 12 pF / 100 Ω differential load	–	–	480	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 10 pF / 100 Ω differential load	–	–	480	Mbps
LVDS Impedance Specification						
Rt	Termination resistance	–	–	100	–	Ω
LVDS AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF

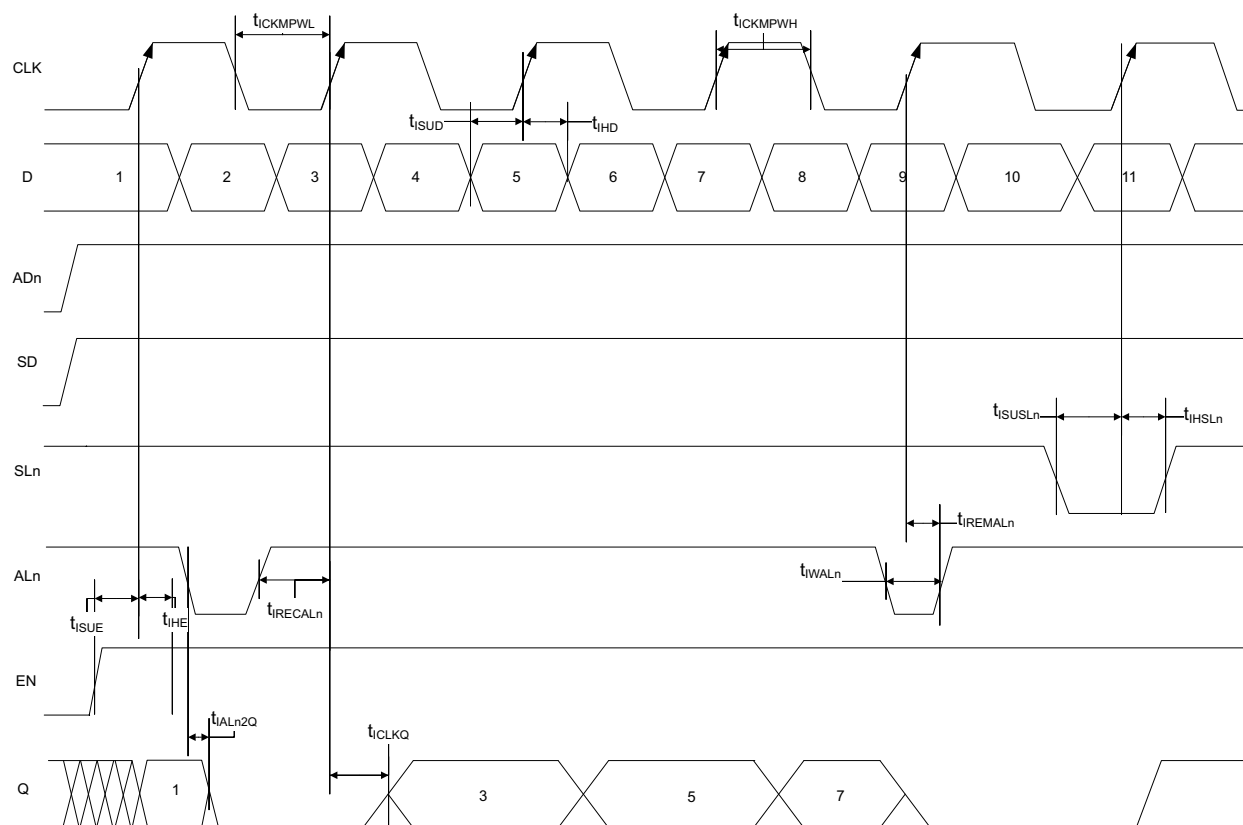


Figure 6 • I/O Register Input Timing Diagram

Table 108 • Input Data Register Propagation Delays
Worst-Case Military Conditions: T_j = 125°C, VDD = 1.14 V

Parameter	Description	Measuring Nodes (from, to)*	Speed Grade –1	Units
t _{IBYP}	Bypass Delay of the Input Register	F,G	0.364	ns
t _{CLKQ}	Clock-to-Q of the Input Register	E,G	0.165	ns
t _{ISUD}	Data Setup Time for the Input Register	A,E	0.369	ns
t _{IHD}	Data Hold Time for the Input Register	A,E	0	ns
t _{ISUE}	Enable Setup Time for the Input Register	B,E	0.475	ns
t _{IHE}	Enable Hold Time for the Input Register	B,E	0	ns
t _{ISUSL}	Synchronous Load Setup Time for the Input Register	D,E	0.475	ns
t _{IHSL}	Synchronous Load Hold Time for the Input Register	D,E	0	ns
t _{IALn2Q}	Asynchronous Clear-to-Q of the Input Register (ADn=1)	C,G	0.648	ns
	Asynchronous Preset-to-Q of the Input Register (ADn=0)	C,G	0.606	ns

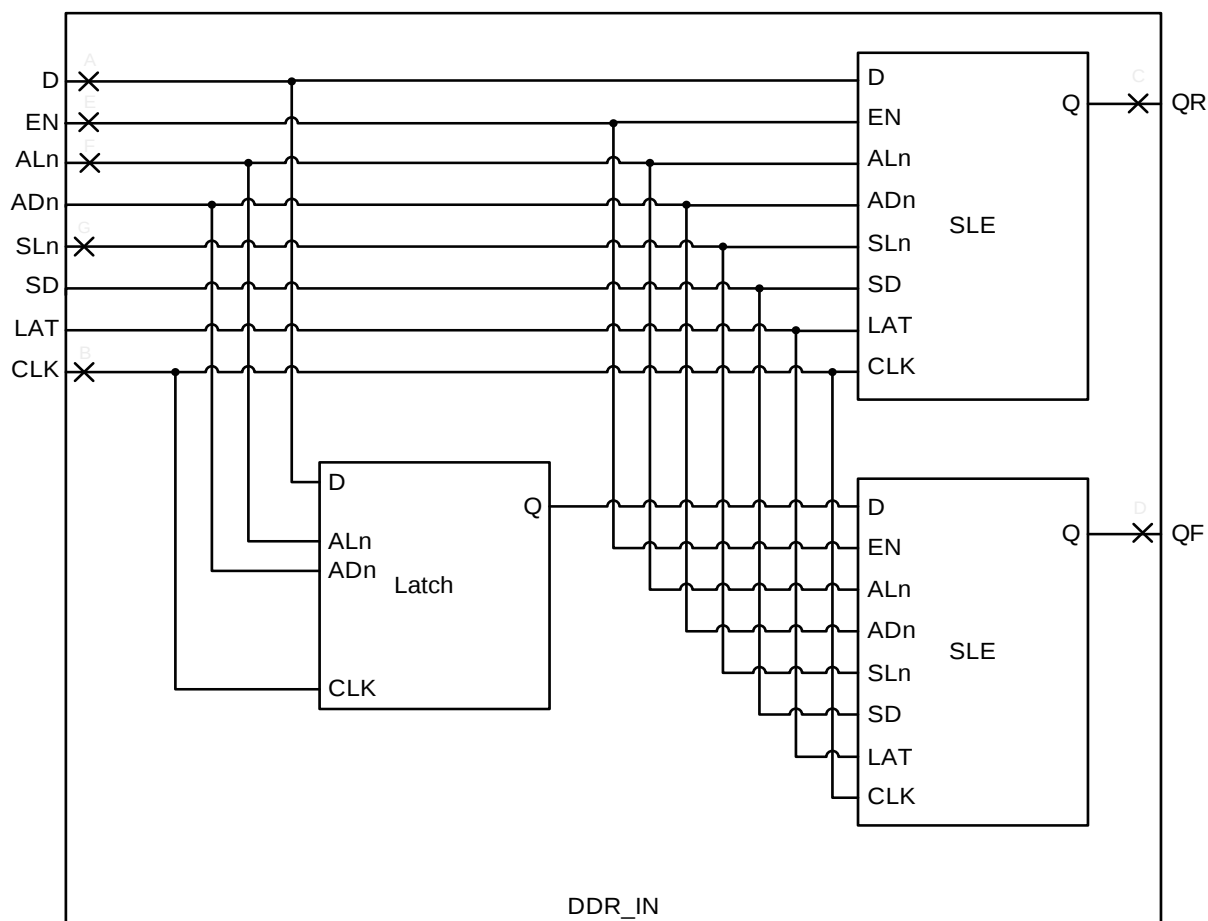
Table 109 • Output/Enable Data Register Propagation Delays

Worst-Case Military Conditions: $T_j = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Measuring Nodes (from, to)*	Speed Grade -1	Units
tORECALn	Asynchronous Load Recovery Time for the Output/Enable Register	C,E	0.035	ns
tOWALn	Asynchronous Load Minimum Pulse Width for the Output/Enable Register	C,C	0.266	ns
tOCKMPWH	Clock Minimum Pulse Width High for the Output/Enable Register	E,E	0.065	ns
tOCKMPWL	Clock Minimum Pulse Width Low for the Output/Enable Register	E,E	0.139	ns

8.10 DDR Module Specification

8.10.1 Input DDR Module


Figure 9 • Input DDR Module

8.10.2 Input DDR Timing Diagram

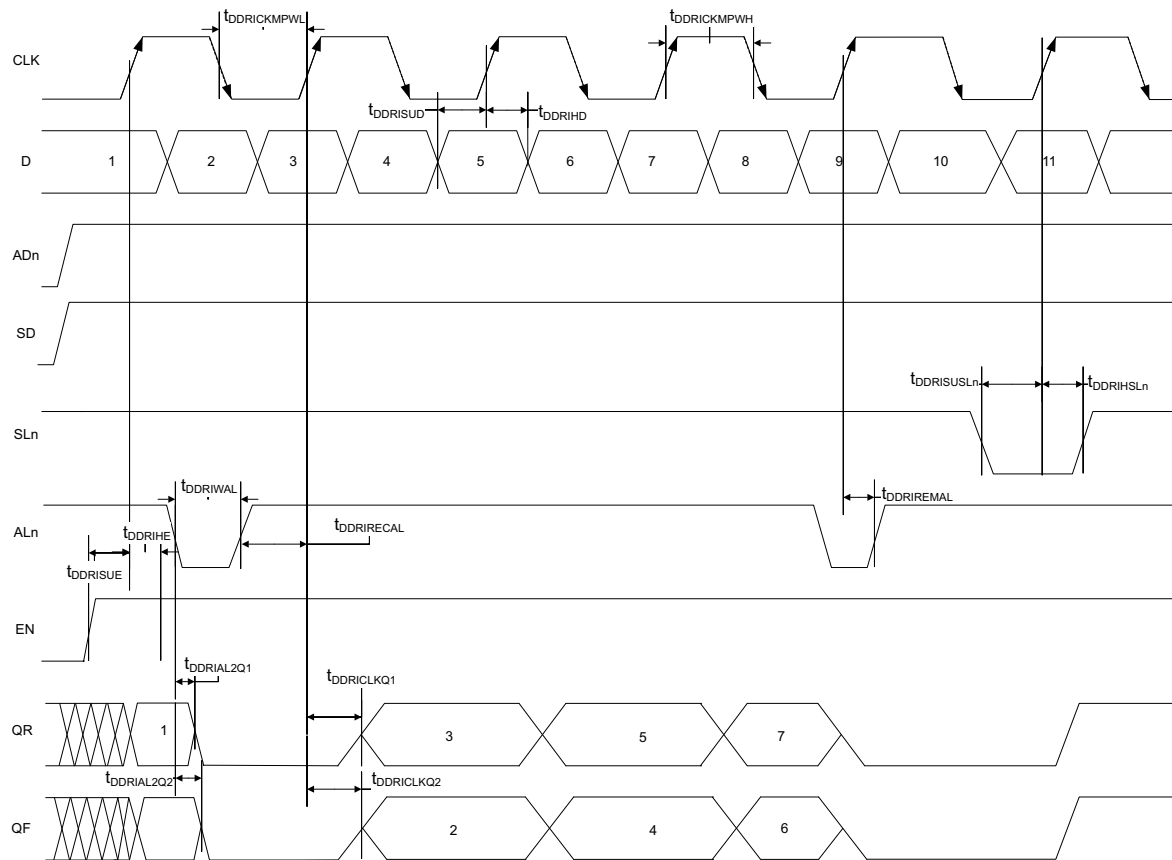


Figure 10 • Input DDR Timing Diagram

Table 121 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4Kx4

Worst-Case Military Conditions: T_j = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		
		Min	Max	Units
trdesu	Read Enable Setup Time	0.532	–	ns
trdehd	Read Enable Hold Time	0.073	–	ns
trdplesu	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
trdpleshd	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
tr2q	Asynchronous Reset to Output Propagation Delay	–	1.562	ns
trstrem	Asynchronous Reset Removal Time	0.522	–	ns
trstrec	Asynchronous Reset Recovery Time	0.005	–	ns
trstmpw	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
tplrstrem	Pipelined Register Asynchronous Reset Removal Time	-0.288	–	ns
tplrstrec	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
tplrstmpw	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
tsrstsu	Synchronous Reset Setup Time	0.233	–	ns
tsrsthd	Synchronous Reset Hold Time	0.037	–	ns
twesu	Write Enable Setup Time	0.473	–	ns
twehd	Write Enable Hold Time	0.05	–	ns
Fmax	Maximum Frequency	–	300	MHz

Table 122 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8Kx2

Worst-Case Military Conditions: T_j = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tcy	Clock Period	3.333	–	ns
tclkmpwh	Clock Minimum Pulse Width High	1.5	–	ns
tclkmpwl	Clock Minimum pulse Width Low	1.5	–	ns
tpcy	Pipelined Clock Period	3.333	–	ns
tpclkmpwh	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
tpclkmpwl	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.332	ns
	Read Access Time without Pipeline Register	–	2.346	ns
	Access Time with Feed-Through Write Timing	–	1.56	ns
taddrsu	Address Setup Time	0.631	–	ns
taddrhd	Address Hold Time	0.282	–	ns

Table 129 • uSRAM (RAM256x4) in 256x4 Mode

Worst-Case Military Conditions: T_j = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
trdenhd	Read Enable Hold Time	0.059	–	ns
tblksu	Read Block Select Setup Time	1.898	–	ns
tblkhd	Read Block Select Hold Time	-0.671	–	ns
tblk2q	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.166	ns
trstrem	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
trstrec	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
tr2q	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.863	ns
tsrstsu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.062	–	ns
tcy	Write Clock Period	4	–	ns
tcclmpwh	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclmpwl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblkcsu	Write Block Setup Time	0.417	–	ns
tblkchd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.104	–	ns
tdinchd	Write Input Data hold Time	0.142	–	ns
taddrcsu	Write Address Setup Time	0.091	–	ns
taddrchd	Write Address Hold Time	0.253	–	ns
twecsu	Write Enable Setup Time	0.41	–	ns
twechd	Write Enable Hold Time	-0.027	–	ns
fmax	Maximum Frequency	–	250	MHz

Table 130 • uSRAM (RAM512x2) in 512x2 Mode

Worst-Case Military Conditions: T_j = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tcy	Read Clock Period	4	–	ns
tcclmpwh	Read Clock Minimum Pulse Width High	1.8		ns

Table 136 • Electrical Characteristics of the Crystal Oscillator – Low Gain Mode (32 kHz)

Worst-Case Military Conditions: $T_j = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Min	Typ	Max	Units
IDYNXTAL	Operating current	–	0.044	–	mA
VIHXTAL	Input logic level High	$0.9 \times V_{PP}$	–	–	V
VILXTAL	Input logic level Low	–	–	$0.1 \times V_{PP}$	V
SUXTAL	Startup time (with regard to stable oscillator output)	–	–	120	ms

14. On-Chip Oscillator

Table 137 and Table 138 describe the electrical characteristics of the available on-chip oscillators in the IGLOO2 FPGAs and SmartFusion2 SoC FPGAs.

Table 137 • Electrical Characteristics of the 50 MHz RC Oscillator

Worst-Case Military Conditions: $T_j = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Condition	Min	Typ	Max	Units
F50RC	Operating frequency	–	–	50	–	MHz
ACC50RC	Accuracy	–	–	1	8	%
CYC50RC	Output duty cycle	–	–	49–51	46–54	%
JIT50RC	Output jitter (peak to peak)	Period Jitter	–	200	500	ps
		Cycle-to-Cycle Jitter	–	320	900	ps
IDYN50RC	Operating current	–	–	8.5	–	mA

Table 138 • Electrical Characteristics of the 1 MHz RC Oscillator

Worst-Case Military Conditions: $T_j = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Condition	Min	Typ	Max	Units
F1RC	Operating frequency	–	–	1	–	MHz
ACC1RC	Accuracy	–	–	1	6	%
CYC1RC	Output duty cycle	–	–	49–51	46.5–53.5	%
JIT1RC	Output jitter (peak to peak)	Period Jitter	–	10	36	ps
		Cycle-to-Cycle Jitter	–	10	50	ps
IDYN1RC	Operating current	–	–	0.1	–	mA
SU1RC	Startup time	–	–	–	20	μs

23. PCIe Electrical and Timing AC and DC Characteristics

PCIe® is a high speed, packet-based, point-to-point, low pin count, serial interconnect bus. The IGLOO2 and SmartFusion2 SoC FPGAs has up to four hard high-speed serial interface blocks. Each SERDES block contains a PCIe system block. The PCIe system is connected to the SERDES block.

Table 152 • Transmitter Parameters

Worst-Case Military Conditions: $T_j = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Min	Typ	Max	Units
VTX-DIFF-PP	Differential swing PCIe Gen1	0.8	–	1.2	V
VTX-CM-AC-P	Output common mode voltage PCIe Gen1	–	–	20	mV
VTX-RISE-FALL	Rise and fall time (20% to 80%) PCIe Gen1	0.125	–	–	UI
ZTX-DIFF-DC	Output impedance – differential	80	–	120	Ω
LTX-SKEW	Lane-to-lane TX skew within a SERDES block PCIe Gen1	–	–	500 ps + 2 UI	ps
RLTX-DIFF	Return loss differential mode PCIe Gen1	–10	–	–	dB
RLTX-CM	Return loss common mode PCIe Gen1	–6	–	–	dB
TX-LOCK-RST	Transmit PLL lock time from reset	–	–	10	μs

Table 153 • Receiver Parameters

Worst-Case Military Conditions: $T_j = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Min	Typ	Max	Units
VRX-DIFF-PP-CC	Input levels PCIe Gen1	0.175	–	1.2	V
VRX-CM-DC-P	Input common mode range (DC coupled) Note: PCIe standard mandates AC coupling	NA	NA	NA	–
VRX-CM-AC-P	Input common mode range (AC coupled)	–	–	150	mV
VRX-DIFF-PP-CC	Differential input sensitivity Gen1	0.175	–	–	mV
ZRX-DIFF-DC	Differential input termination	80	100	120	Ω
REXT	External calibration resistor	1,188	1,200	1,212	Ω
CDR-LOCK-RST	CDR relock time from reset	–	–	15	μs
RLRX-DIFF	Return loss differential mode PCIe Gen1	–10	–	–	dB
RLRX-CM	Return loss common mode PCIe Gen1	–6	–	–	dB
	CID limit (set by 8B/10B coding, not the receiver PLL)	–	–	4	UI
VRX-IDLE-DET-DIFF-PP	Signal detect limit	65	–	175	mV

Table 154 • SERDES Reference Clock AC Specifications

Worst-Case Military Conditions: $T_j = 125^{\circ}\text{C}$, Worst-Case $V_{DD} = 1.14\text{ V}$

Symbols	Description	Min	Typ	Max	Units
FREFCLK	Reference Clock Frequency	100	–	160	MHz
TRISE	Reference Clock Rise Time	0.6	–	4	V/ns
TFALL	Reference Clock Fall Time	0.6	–	4	V/ns
TCYC	Reference Clock Duty Cycle	40	–	60	%
Mmrefclk	Reference Clock Mismatch	–300	–	300	ppm
SSCref	Reference Spread Spectrum Clock	0	–	5000	ppm

Table 155 • HCSL Minimum and Maximum DC Input Levels (Applicable to SERDES REFCLK Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
VDDI	Supply Voltage	–	2.375	2.5	2.625	V
HCSL DC Input Voltage Specification						
VI	DC Input voltage	–	0	–	2.625	V
HCSL Differential Voltage Specification						
VICM	Input common mode voltage	–	0.05	–	2.4	V
VIDIFF	Input differential voltage	–	100	–	1100	mV

Table 156 • HCSL Maximum AC Switching Speeds (Applicable to SERDES REFCLK Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
HCSL AC Specifications						
Fmax	Maximum Data Rate (for MSIO IO Bank)	–	–	–	350	Mbps
HCSL Impedance Specifications						
Rt	Termination Resistance	–	–	100	–	Ω

24. SmartFusion2 Specifications

24.1 MSS Clock Frequency

Table 157 • Maximum Frequency for MSS Main Clock

Worst-Case Military Conditions: T_j = 125°C, VDD = 1.14 V

Symbol	Description	Speed Grade –1	Units
M3_CLK	Maximum frequency for the MSS Main Clock (FCLK)	133	MHz

24.2 SmartFusion2 Inter-Integrated Circuit (I²C) Characteristics

This section describes the DC and switching of the I²C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, refer to Figure 16 on page 112.

Table 158 • I2C Characteristics

Worst-Case Military Conditions: T_j = 125°C, VDD = 1.14 V

Parameter	Definition	Conditions	Min	Typ	Max	Units	Notes
VIL	Input low voltage	Refer to the "Single-Ended I/O Standards" section on page 27 for more information. I/O standard used for illustration: MSIO bank– LVTTTL 8 mA low drive.	–0.3	–	0.8	V	–
VIH	Input high voltage	Refer to the "Single-Ended I/O Standards" section on page 27 for more information. I/O standard used for illustration: MSIO bank – LVTTTL 8 mA low drive.	2	–	3.45	V	–

Table 158 • I2C Characteristics

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Definition	Conditions	Min	Typ	Max	Units	Notes
VHYS	Hysteresis of Schmitt triggered inputs for $V_{DDI} > 2\text{ V}$	Refer to Table 20 on page 27 for more information.	$0.05 \times V_{DDI}$	–	–	V	–
IIL	Input current high	Refer to the "Single-Ended I/O Standards" section on page 27 for more information.	–	–	10	μA	–
IIH	Input current low	Refer to the "Single-Ended I/O Standards" section on page 27 for more information.	–	–	10	μA	–
Tir	Input rise time	Standard Mode	–	–	1000	ns	–
–	–	Fast Mode	–	–	300	ns	–
Tif	Input fall time	Standard Mode	–	–	300	ns	–
–	–	Fast Mode	–	–	300	ns	–
VOL	Maximum output voltage low (open drain) at 3 mA sink current for $V_{DDI} > 2\text{ V}$	Refer to the "Single-Ended I/O Standards" section on page 27 for more information. I/O standard used for illustration: MSIO bank – LVTTTL 8 mA low drive.	–	–	0.4	V	–
Cin	Pin capacitance	$V_{IN} = 0$, $f = 1.0\text{ MHz}$	–	–	10	pF	–
t_{OF}	Output fall time from V_{IHmin} to V_{ILMax}	V_{IHmin} to V_{ILMax} , $C_{load} = 400\text{ pF}$	–	21.04	–	ns	1
		V_{IHmin} to V_{ILMax} , $C_{load} = 100\text{ pF}$	–	5.556	–	ns	
t_{OR}	Output rise time from V_{ILMax} to V_{IHmin}	V_{ILMax} to V_{IHmin} , $C_{load} = 400\text{ pF}$	–	19.887	–	ns	1
		V_{ILMax} to V_{IHmin} , $C_{load} = 100\text{ pF}$	–	5.218	–	ns	
Rpull-up	Output maximum buffer pull-down resistance	–	–	–	50	Ω	2, 3
Rpull-down	Output maximum buffer pull-up resistance	–	–	–	131.25	Ω	2, 4
Dmax	Maximum data rate	Fast mode	–	–	400	Kbps	–
		Standard mode	–	–	100	Kbps	–
t_{FILT}	Pulse width of spikes which must be suppressed by the input filter	Fast mode	–	50	–	ns	–

Notes:

1. These values are provided for MSIO Bank - LVTTTL 8 mA Low Drive at 25°C , typical conditions. For Board Design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models>.
2. These maximum values are provided for information only. Minimum output buffer resistance values depend on V_{DDI} , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models>.
3. $R(\text{PULL-DOWN-MAX}) = (V_{OLspec}) / I_{OLspec}$
4. $R(\text{PULL-UP-MAX}) = (V_{DDImax} - V_{OHspec}) / I_{OHspec}$

Table 159 • I²C Switching Characteristics

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Definition	Conditions	Speed Grade -1		Units
			Min	Max	
t_{LOW}	Low period of I2C_x_SCL	—	1	—	pclk cycles
t_{HIGH}	High period of I2C_x_SCL	—	1	—	pclk cycles
$t_{\text{HD;STA}}$	START hold time	—	1	—	pclk cycles
$t_{\text{SU;STA}}$	START setup time	—	1	—	pclk cycles
$t_{\text{HD;DAT}}$	DATA hold time	—	1	—	pclk cycles
$t_{\text{SU;DAT}}$	DATA setup time	—	1	—	pclk cycles
$t_{\text{SU;STO}}$	STOP setup time	—	1	—	pclk cycles

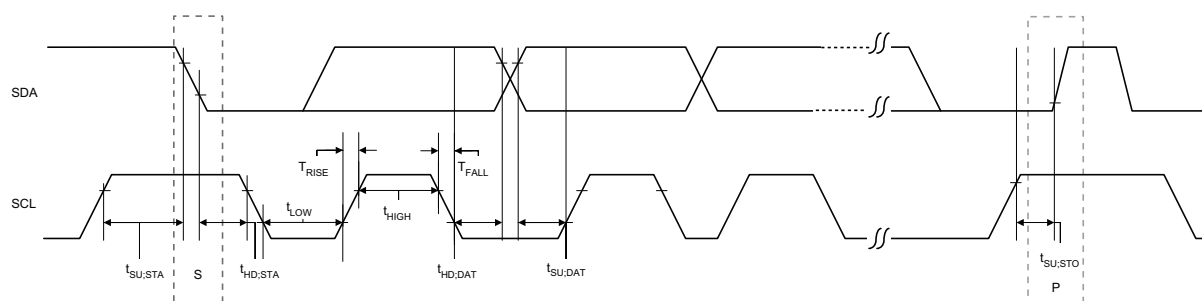

Figure 16 • I²C Timing Parameter Definition

Table 164 • SPI Characteristics

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Symbol	Description	Conditions	All Devices/Speed Grades			Unit	Notes
			Min	Typ	Max		
sp9s	SPI_[0]1_DI hold time	—	3	—	—	ns	2

Notes:

- For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website:
<http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models>.
- For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.

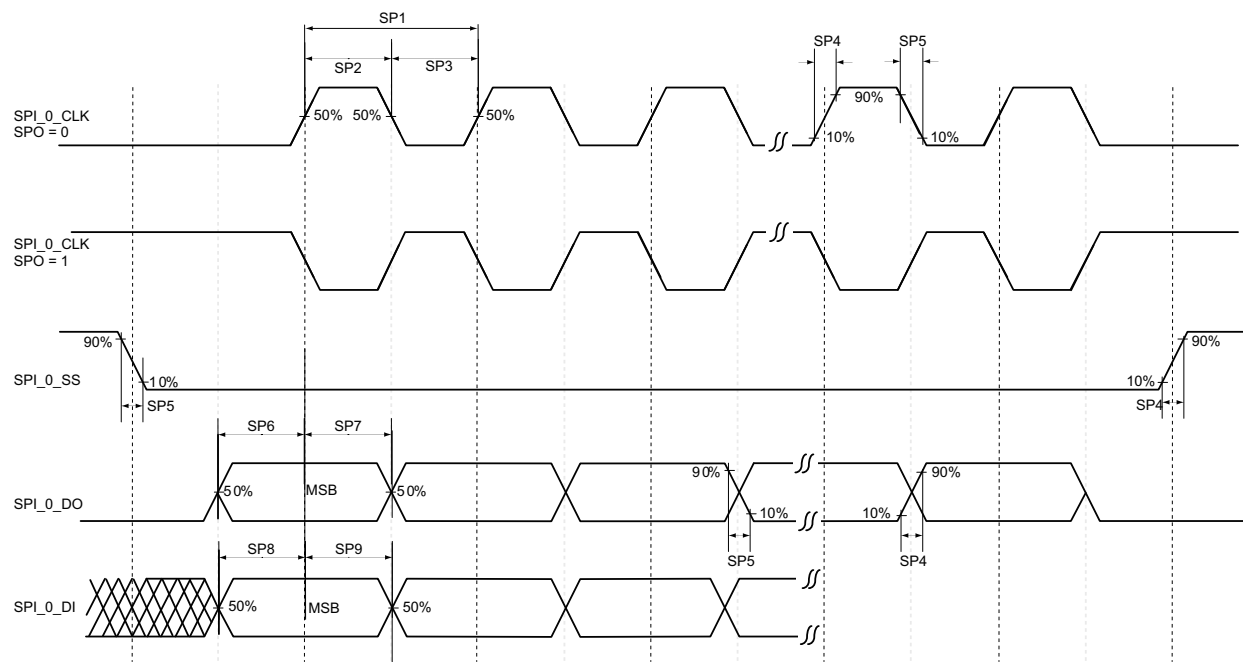


Figure 18 • SPI Timing for a Single Frame Transfer in Motorola Mode ($SPH = 1$)

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in Table 1 on page 10 is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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