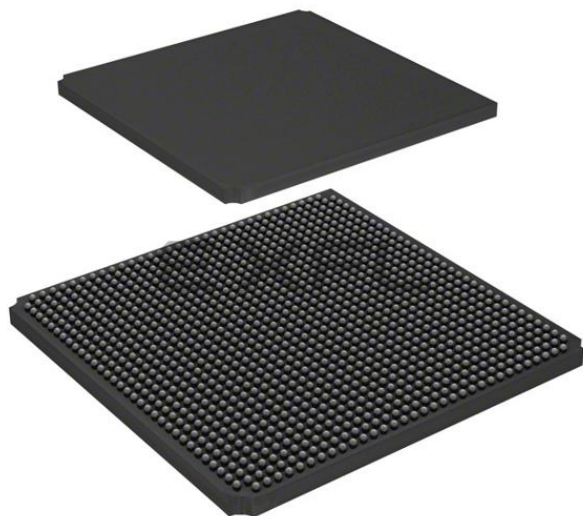




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	146124
Total RAM Bits	5120000
Number of I/O	574
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl150t-1fcg1152m

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8.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

8.6.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 21 • LVTTL/LVCMOS 3.3 V DC Voltage Specification (Applicable to MSIO I/O Bank Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units	Notes
LVTTL/LVCMOS 3.3 V Recommended DC Operating Conditions							
VDDI	Supply voltage		3.15	3.3	3.45	V	–
LVTTL/LVCMOS 3.3 V DC Input Voltage Specification							
VIH (DC)	DC input logic High		2.0	–	3.45	V	–
VIL (DC)	DC input logic Low		–0.3	–	0.8	V	–
IIH (DC)	Input current High		–	–	10	μA	–
IIL (DC)	Input current Low		–	–	10	μA	–
LVCMOS 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		2.4	–	–	V	*
VOL	DC output logic Low		–	–	0.4	V	*
LVTTL 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		2.4	–	–	V	–
VOL	DC output logic Low		–	–	0.4	V	–
Note: * The VOH/VOL test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.							

Table 22 • LVTTL/LVCMOS 3.3 V Maximum Switching Speeds (Applicable to MSIO I/O Bank Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
LVTTL/LVCMOS 3.3 V Maximum Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	540	Mbps

Table 23 • LVTTL/LVCMOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO Bank Only)

LVTTL/LVCMOS 3.3 V AC Test Parameter Specifications						
Symbol	Parameters	Conditions	Min	Typ	Max	Units
Vtrip	Measuring/trip point for data path		–	1.4	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

8.6.3 2.5 V LVCMOS

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in IGLOO2 FPGA and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-5A.

8.6.3.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 27 • LVCMOS 2.5 V DC Voltage Specification

Symbol	Parameters	Conditions	Min	Typ	Max	Units	Notes
LVCMOS 2.5 V Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	–
LVCMOS 2.5 V DC Input Voltage Specification							
VIH (DC)	DC input logic High (for MSIOD and DDRIO I/O Bank)		1.7	–	2.625	V	–
VIH (DC)	DC input logic High (for MSIO I/O Bank)		1.7	–	2.75	V	–
VIL (DC)	DC input logic Low		–0.3	–	0.7	V	–
IIH (DC)	Input current High		–	–	10	μA	–
IIL (DC)	Input current Low		–	–	10	μA	–
LVCMOS 2.5 V DC Output Voltage Specification							
VOH	DC output logic High		1.7	–	–	V	*
VOL	DC output logic Low		–	–	0.7	V	*
Note: * The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.							

Table 28 • LVCMOS 2.5 V Maximum AC Switching Speeds

Symbol	Parameters	Conditions	Min	Typ	Max	Units
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	360	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	360	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	370	Mbps

Table 29 • LVCMOS 2.5 V AC Test Parameters and Driver Impedance Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 2.5 V Calibrated Impedance Option						
Rodt_cal	Supported output driver calibrated impedance (for DDRIO I/O Bank)	–	–	75, 60, 50, 33, 25, 20	–	Ω
LVCMOS 2.5 V AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path	–	–	1.2	–	V
Rent	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})	–	–	2k	–	Ω
Cent	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})	–	–	5	–	pF
Cload	Capacitive loading for data path (t _{DP})	–	–	5	–	pF

Table 45 • LVCMOS 1.5 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Military Conditions: $T_J=125^{\circ}\text{C}$, $V_{DD}=1.14\text{ V}$, $V_{DDI}=1.425\text{ V}$ (continued)

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
8 mA	slow	4.603	3.691	4.585	7.397	6.553	ns
	medium	4.081	3.242	4.062	7.064	6.189	ns
	medium_fast	3.827	3.015	3.804	6.912	6.051	ns
	fast	3.804	2.994	3.781	6.903	6.051	ns
10 mA	slow	4.519	3.612	4.499	7.578	6.676	ns
	medium	4.026	3.177	4.005	7.264	6.335	ns
	medium_fast	3.775	2.948	3.75	7.11	6.198	ns
	fast	3.747	2.929	3.721	7.103	6.19	ns
12 mA	slow	4.456	3.562	4.433	7.704	6.795	ns
	medium	3.965	3.13	3.943	7.388	6.425	ns
	medium_fast	3.731	2.912	3.704	7.278	6.303	ns
	fast	3.703	2.893	3.676	7.275	6.294	ns
LVCMOS 1.5 V (for MSIO I/O Bank)							
2 mA	slow	5.118	6.263	6.53	6.524	6.388	ns
4 mA	slow	4.657	5.178	5.65	8.57	7.55	ns
6 mA	slow	4.693	4.89	5.389	8.928	7.766	ns
8 mA	slow	4.876	4.663	5.183	9.59	8.173	ns
LVCMOS 1.5 V (for MSIOD I/O Bank)							
2 mA	slow	3.085	3.795	4.086	6.838	6.477	ns
4 mA	slow	2.731	3.365	3.631	7.663	7.165	ns
6 mA	slow	2.742	3.162	3.417	8.126	7.52	ns

8.6.6 1.2 V LVCMOS

LVCMOS 1.2 is a general standard for 1.2 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-12A.

8.6.6.1 Minimum and Maximum Input and Output Levels Specification

Table 46 • LVCMOS 1.2 V Minimum and Maximum DC Input and Output Levels

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 1.2 V Recommended DC Operating Conditions						
VDDI	Supply voltage		1.140	1.2	1.26	V
LVCMOS 1.2 V DC Input Voltage Specification						
VIH (DC)	DC input logic High (for MSIOD and DDRIO I/O Banks)	$0.65 \times V_{DDI}$	–		1.26	V
VIH (DC)	DC input logic High (for MSIO I/O Bank)	$0.65 \times V_{DDI}$	–		2.75	V
VIL (DC)	DC input logic Low	–0.3	–		$0.35 \times V_{DDI}$	V
IIH (DC)	Input current High		–	–	10	μA

Table 51 • LVCMOS 1.2 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Military Conditions: $T_J=125^{\circ}\text{C}$, $V_{DD}=1.14\text{ V}$, $V_{DDI}=1.14\text{ V}$ (continued)

Output Drive Selection	Slew Control	Speed Grade -1					Units
		t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
LVCMOS 1.2 V (for MSIOD I/O Bank)							
2 mA	slow	4.048	5.123	5.552	8.401	7.824	ns
4 mA	slow	3.941	4.406	4.814	9.422	8.656	ns

8.6.7 3.3 V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3 V standards specify support for 33 MHz and 66 MHz PCI bus applications.

8.6.7.1 Minimum and Maximum Input and Output Levels Specification

Table 52 • PCI/PCI-X DC Voltage Specification (Applicable to MSIO Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
PCI/PCIX Recommended DC Operating Conditions						
V_{DDI}	Supply voltage		3.15	3.3	3.45	V
PCI/PCIX DC Input Voltage Specification						
V_I	DC input voltage		0	–	3.45	V
$I_{IH}(\text{DC})$	Input current High		–	–	10	μA
$I_{IL}(\text{DC})$	Input current Low		–	–	10	μA
PCI/PCIX DC Output Voltage Specification						
V_{OH}	DC output logic High		Per PCI Specification			V
V_{OL}	DC output logic Low		Per PCI Specification			V

Table 53 • PCI/PCI-X AC Specifications (Applicable to MSIO Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
PCI/PCI-X AC Specifications						
D_{max}	Maximum data rate (MSIO I/O Bank)	AC Loading: per JEDEC specifications	–	–	560	Mbps
PCI/PCI-X AC Test Parameters Specifications						
V_{trip}	Measuring/trip point for data path (falling edge)		–	$0.615 \times V_{DDI}$	–	V
V_{trip}	Measuring/trip point for data path (rising edge)		–	$0.285 \times V_{DDI}$	–	V
$R_{\text{tt_test}}$	Resistance for data test path		–	25	–	Ω
R_{ent}	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
C_{ent}	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF
C_{load}	Capacitive loading for data path (t_{DP})		–	10	–	pF

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 82 • LPDDR - LVCMOS 1.8 V AC Switching Characteristics for Transmitter DDRIO I/O Bank (Output and Tristate Buffers)

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.71\text{ V}$

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
2 mA	slow	4.681	4.017	4.69	5.388	4.852	ns
	medium	4.211	3.599	4.219	5.058	4.488	ns
	medium_fast	3.978	3.392	3.986	4.874	4.327	ns
	fast	3.953	3.373	3.961	4.858	4.316	ns
4 mA	slow	4.355	3.657	4.346	5.967	5.399	ns
	medium	3.886	3.246	3.879	5.628	5.01	ns
	medium_fast	3.656	3.05	3.647	5.461	4.845	ns
	fast	3.635	3.033	3.626	5.447	4.838	ns
6 mA	slow	4.105	3.422	4.092	6.221	5.599	ns
	medium	3.68	3.05	3.668	5.9	5.257	ns
	medium_fast	3.477	2.867	3.463	5.739	5.118	ns
	fast	3.451	2.849	3.437	5.72	5.104	ns
8 mA	slow	4.015	3.32	3.998	6.458	5.808	ns
	medium	3.59	2.947	3.574	6.129	5.449	ns
	medium_fast	3.383	2.761	3.366	5.963	5.304	ns
	fast	3.357	2.746	3.34	5.954	5.289	ns
10 mA	slow	3.888	3.18	3.864	6.739	6.045	ns
	medium	3.485	2.822	3.467	6.422	5.7	ns
	medium_fast	3.281	2.642	3.26	6.277	5.553	ns
	fast	3.258	2.627	3.238	6.27	5.546	ns
12 mA	slow	3.795	3.096	3.773	6.773	6.067	ns
	medium	3.408	2.764	3.389	6.47	5.743	ns
	medium_fast	3.215	2.599	3.194	6.346	5.61	ns
	fast	3.196	2.584	3.175	6.335	5.604	ns
16 mA	slow	3.744	3.035	3.719	6.944	6.207	ns
	medium	3.358	2.712	3.339	6.657	5.868	ns
	medium_fast	3.175	2.546	3.153	6.547	5.751	ns
	fast	3.156	2.531	3.133	6.541	5.747	ns

Table 106 • LVPECL Maximum AC Switching Speeds (Applicable to MSIO I/O Banks Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVPECL AC Specifications						
Fmax	Maximum data rate (for MSIO I/O Bank)		–	–	810	Mbps

8.8.6.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 107 • LVPECL Receiver Characteristics

Worst-case Military conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 3.15\text{ V}$

	On-Die Termination (ODT)	t _{py}	Units
		Speed Grade –1	
LVPECL (for MSIO I/O Bank)	None	2.71	ns
	100	2.71	ns

8.9 I/O Register Specifications

8.9.1 Input Register

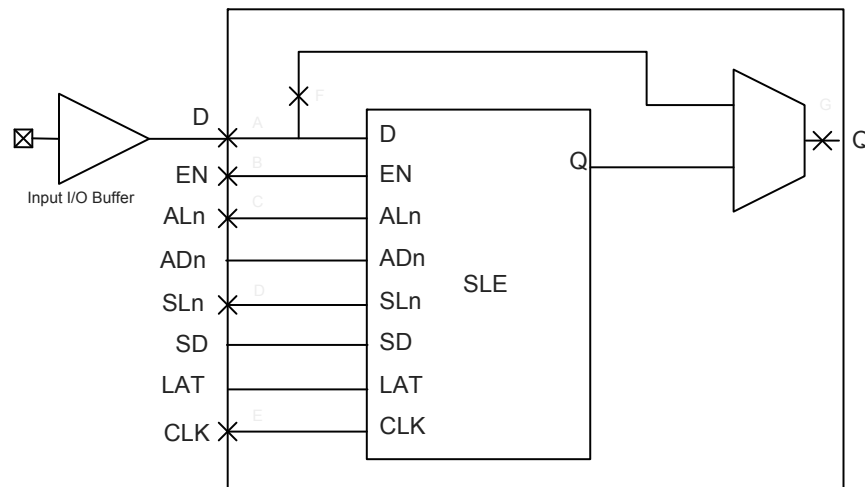


Figure 5 • Timing Model for Input Register

8.10.3 Timing Characteristics

Table 110 • Input DDR Propagation Delays
Worst-Case Military Conditions: $T_j = 125^{\circ}\text{C}$, $V_{DD}=1.14\text{ V}$

Parameter	Description	Measuring Nodes (from, to)	Speed Grade -1	Units
tDDRICKQ1	Clock-to-Out Out_QR for Input DDR	B,C	0.165	ns
tDDRICKQ2	Clock-to-Out Out_QF for Input DDR	B,D	0.172	ns
tDDRISUD	Data Setup for Input DDR	A,B	0.372	ns
tDDRILD	Data Hold for Input DDR	A,B	0	ns
tDDRISUE	Enable Setup for Input DDR	E,B	0.475	ns
tDDRILHE	Enable Hold for Input DDR	E,B	0	ns
tDDRISUSLn	Synchronous Load Setup for Input DDR	G,B	0.475	ns
tDDRILSLn	Synchronous Load Hold for Input DDR	G,B	0	ns
tDDRIAL2Q1	Asynchronous Load-to-Out QR for Input DDR	F,C	0.606	ns
tDDRIAL2Q2	Asynchronous Load-to-Out QF for Input DDR	F,D	0.558	ns
tDDRIREMAL	Asynchronous Load Removal time for Input DDR	F,B	0	ns
tDDRIRECAL	Asynchronous Load Recovery time for Input DDR	F,B	0.076	ns
tDDRILWAL	Asynchronous Load Minimum Pulse Width for Input DDR	F,F	0.313	ns
tDDRICKMPWH	Clock Minimum Pulse Width High for Input DDR	B,B	0.078	ns
tDDRICKMPWL	Clock Minimum Pulse Width Low for Input DDR	B,B	0.164	ns

Table 115 • M2S090T Device Global Resource (continued)

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tRCKH	Input High Delay for Global Clock	1.412	1.498	ns
tRCKSW	Maximum Skew for Global Clock	–	0.086	ns

Table 116 • M2S050T Device Global Resource

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tRCKL	Input Low Delay for Global Clock	0.793	0.861	ns
tRCKH	Input High Delay for Global Clock	1.436	1.55	ns
tRCKSW	Maximum Skew for Global Clock	–	0.114	ns

Table 117 • M2S025T Device Global Resource

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tRCKL	Input Low Delay for Global Clock	0.713	0.762	ns
tRCKH	Input High Delay for Global Clock	1.306	1.391	ns
tRCKSW	Maximum Skew for Global Clock	–	0.085	ns

Table 118 • M2S010T Device Global Resource

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tRCKL	Input Low Delay for Global Clock	0.598	0.639	ns
tRCKH	Input High Delay for Global Clock	1.116	1.192	ns
tRCKSW	Maximum Skew for Global Clock	–	0.076	ns

11. FPGA Fabric SRAM

Refer to the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for more information.

11.1 FPGA Fabric Large SRAM (LSRAM)

Table 119 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1Kx18
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t _{cy}	Clock Period	3.333	–	ns
t _{clkmpwh}	Clock Minimum Pulse Width High	1.5	–	ns
t _{clkmpwl}	Clock Minimum pulse Width Low	1.5	–	ns
t _{p_lcy}	Pipelined Clock Period	3.333	–	ns
t _{p_lclkmpwh}	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
t _{p_lclkmpwl}	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
t _{clk2q}	Read Access Time with Pipeline Register	–	0.346	ns
	Read Access Time without Pipeline Register	–	2.346	ns
	Access Time with Feed-Through Write Timing	–	1.578	ns
t _{addr_{su}}	Address Setup Time	0.455	–	ns
t _{addr_{hd}}	Address Hold Time	0.282	–	ns
t _{dsu}	Data Setup Time	0.352	–	ns
t _{dhd}	Data Hold Time	0.11	–	ns
t _{blksu}	Block Select Setup Time	0.214	–	ns
t _{blkhd}	Block Select Hold Time	0.223	–	ns
t _{blk2q}	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	1.578	ns
t _{blkmpw}	Block Select Minimum Pulse Width	0.218	–	ns
t _{rdesu}	Read Enable Setup Time	0.463	–	ns
t _{rdehd}	Read Enable Hold Time	0.173	–	ns
t _{rdp_lesu}	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
t _{rdp_lehd}	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
t _{r2q}	Asynchronous Reset to Output Propagation Delay	–	1.561	ns
t _{rstrem}	Asynchronous Reset Removal Time	0.522	–	ns
t _{rstrec}	Asynchronous Reset Recovery Time	0.005	–	ns
t _{rstmpw}	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
t _{p_lrstrem}	Pipelined Register Asynchronous Reset Removal Time	–0.288	–	ns
t _{p_lrstrec}	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
t _{p_lrstmpw}	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns

Table 127 • uSRAM (RAM128x9) in 128x9 Mode
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
tclkmpwl	Read Clock Minimum pulse Width Low	1.8	–	ns
tplcy	Read Pipe-line clock period	4	–	ns
tplclkmpwh	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
tplclkmpwl	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.776	ns
taddrsu	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	1.959	–	ns
taddrhd	Read Address Hold Time in Synchronous Mode	0.125	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.704	–	ns
trdensu	Read Enable Setup Time	0.287	–	ns
trdenhd	Read Enable Hold Time	0.059	–	ns
tblksu	Read Block Select Setup Time	1.898	–	ns
tblkhd	Read Block Select Hold Time	-0.671	–	ns
tblk2q	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.14	ns
trstrem	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
trstrec	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
tr2q	Read Asynchronous Reset to Output Propagation Delay (with Pipe-Line Register Enabled)	–	0.865	ns
tsrstsu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.062	–	ns
tccy	Write Clock Period	4	–	ns
tcclkmpwh	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclkmpwl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblkcsu	Write Block Setup Time	0.417	–	ns
tblkchd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.104	–	ns
tdinchd	Write Input Data hold Time	0.142	–	ns
taddrcsu	Write Address Setup Time	0.091	–	ns

Table 128 • uSRAM (RAM128x8) in 128x8 Mode
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
tr2q	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.865	ns
tsrstu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.062	–	ns
tccy	Write Clock Period	4	–	ns
tcclcmpwh	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclcmpwl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblkcsu	Write Block Setup Time	0.417	–	ns
tblkchd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.104	–	ns
tdinchd	Write Input Data hold Time	0.142	–	ns
taddrcsu	Write Address Setup Time	0.091	–	ns
taddrchd	Write Address Hold Time	0.24	–	ns
twecsu	Write Enable Setup Time	0.41	–	ns
twechd	Write Enable Hold Time	-0.027	–	ns
fmax	Maximum Frequency	–	250	MHz

Table 129 • uSRAM (RAM256x4) in 256x4 Mode
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
tcy	Read Clock Period	4	–	ns
tclcmpwh	Read Clock Minimum Pulse Width High	1.8	–	ns
tclcmpwl	Read Clock Minimum pulse Width Low	1.8	–	ns
tpcy	Read Pipe-line clock period	4	–	ns
tpclcmpwh	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
tpclcmpwl	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.812	ns
taddrsu	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	1.993	–	ns
taddrhd	Read Address Hold Time in Synchronous Mode	0.125	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.669	–	ns
trdensu	Read Enable Setup Time	0.287	–	ns

Table 129 • uSRAM (RAM256x4) in 256x4 Mode
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
trdenhd	Read Enable Hold Time	0.059	–	ns
tblksu	Read Block Select Setup Time	1.898	–	ns
tblkhd	Read Block Select Hold Time	-0.671	–	ns
tblk2q	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.166	ns
trstrem	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
trstrec	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
tr2q	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.863	ns
tsrstsu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.062	–	ns
tccy	Write Clock Period	4	–	ns
tcclmpwh	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclmpwl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblkcsu	Write Block Setup Time	0.417	–	ns
tblkchd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.104	–	ns
tdinchd	Write Input Data hold Time	0.142	–	ns
taddrcsu	Write Address Setup Time	0.091	–	ns
taddrchd	Write Address Hold Time	0.253	–	ns
twecsu	Write Enable Setup Time	0.41	–	ns
twechd	Write Enable Hold Time	-0.027	–	ns
fmax	Maximum Frequency	–	250	MHz

Table 130 • uSRAM (RAM512x2) in 512x2 Mode
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
tcy	Read Clock Period	4	–	ns
tcclmpwh	Read Clock Minimum Pulse Width High	1.8		ns

Table 136 • Electrical Characteristics of the Crystal Oscillator – Low Gain Mode (32 kHz)

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Min	Typ	Max	Units
IDYNXTAL	Operating current	–	0.044	–	mA
VIHXTAL	Input logic level High	$0.9 \times V_{PP}$	–	–	V
VILXTAL	Input logic level Low	–	–	$0.1 \times V_{PP}$	V
SUXTAL	Startup time (with regard to stable oscillator output)	–	–	120	ms

14. On-Chip Oscillator

Table 137 and Table 138 describe the electrical characteristics of the available on-chip oscillators in the IGLOO2 FPGAs and SmartFusion2 SoC FPGAs.

Table 137 • Electrical Characteristics of the 50 MHz RC Oscillator

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Condition	Min	Typ	Max	Units
F50RC	Operating frequency	–	–	50	–	MHz
ACC50RC	Accuracy	–	–	1	8	%
CYC50RC	Output duty cycle	–	–	49–51	46–54	%
JIT50RC	Output jitter (peak to peak)	Period Jitter	–	200	500	ps
		Cycle-to-Cycle Jitter	–	320	900	ps
IDYN50RC	Operating current	–	–	8.5	–	mA

Table 138 • Electrical Characteristics of the 1 MHz RC Oscillator

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Condition	Min	Typ	Max	Units
F1RC	Operating frequency	–	–	1	–	MHz
ACC1RC	Accuracy	–	–	1	6	%
CYC1RC	Output duty cycle	–	–	49–51	46.5–53.5	%
JIT1RC	Output jitter (peak to peak)	Period Jitter	–	10	36	ps
		Cycle-to-Cycle Jitter	–	10	50	ps
IDYN1RC	Operating current	–	–	0.1	–	mA
SU1RC	Startup time	–	–	–	20	μs

15. Clock Conditioning Circuits (CCC)

Table 139 • IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification
Military Worst-Case Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Conditions	Min	Typ	Max	Units	Notes
Clock conditioning circuitry input frequency f_{IN_CCC}	All CCC	1	–	200	MHz	–
	32 kHz Capable CCC	0.032		200	MHz	–
Clock conditioning circuitry output frequency f_{OUT_CCC}	–	0.078	–	400	MHz	1
PLL VCO frequency	–	500	–	1000	MHz	2
Delay increments in programmable delay blocks	–	–	75	100	ps	–
Number of programmable values in each programmable delay block	–	–	–	64	–	–
Acquisition time	–	–	70	100	μs	–
Input Duty Cycle (Reference Clock)	Internal Feedback					
	$1\text{ MHz} \leq f_{IN_CCC} \leq 25\text{ MHz}$	10	–	90	%	–
	$25\text{ MHz} \leq f_{IN_CCC} \leq 100\text{ MHz}$	25	–	75	%	–
	$100\text{ MHz} \leq f_{IN_CCC} \leq 150\text{ MHz}$	35	–	65	%	–
	$150\text{ MHz} \leq f_{IN_CCC} \leq 200\text{ MHz}$	45	–	55	%	–
	External Feedback (CCC, FPGA, Off-chip)					
	$1\text{ MHz} \leq f_{IN_CCC} \leq 25\text{ MHz}$	25	–	75	%	–
	$25\text{ MHz} \leq f_{IN_CCC} \leq 35\text{ MHz}$	35	–	65	%	–
	$35\text{ MHz} \leq f_{IN_CCC} \leq 50\text{ MHz}$	45	–	55	%	–
Output duty cycle	010, 025, and 050 Devices	46	–	52	%	–
	090 and 150 Devices	44	–	52	%	–
Spread Spectrum Characteristics						
Modulation frequency range	–	25	35	50	kHz	–
Modulation depth range	–	0	–	1.5	%	–
Modulation depth control	–	–	0.5	–	%	–
Notes:						
1. The minimum output clock frequency is limited by the PLL. For more information refer to the UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide.						
2. The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance will be limited by the CCC output frequency.						

Table 140 • IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications
Worst-Case Military Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Conditions/Package Combinations					Units	Notes
CCC Output Peak-to-Peak Period Jitter fOUT_CCC							
010, 050 FG484 Packages	SSO = 0	0 < SSO <= 2	SSO <= 4	SSO <= 8	SSO <= 16	–	*
20 MHz to 100 MHz	Max(110, ± 1% x (1/fOUT_CCC))	Max(150, ± 1% x (1/fOUT_CCC))				ps	–
100 MHz to 400 MHz	120	150			170	ps	–
025 FG484 Package	0 < SSO <=16						*
20 MHz to 74 MHz	± 1% x (1/fOUT_CCC)					ps	–
74 MHz to 400 MHz	210					ps	–
090 FG484 and 150 FC1152 Packages	0 < SSO <=16						*
20 MHz to 100 MHz	± 1% x (1/fOUT_CCC)					ps	–
100 MHz to 400 MHz	150					ps	–
Note: *SSO Data is based on LVCMOS 2.5 V MSIO and/or MSIOD Bank I/Os.							

16. JTAG

Table 141 • JTAG 1532
Worst-Case Military Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	-1 Speed Grade					Units
		010	025	050	090	150	
tTCK2Q	Clock to Q (data out)	7.91	7.95	8.15	9.21	8.85	ns
tRSTB2Q	Reset to Q (data out)	6.54	6.27	7.54	7.94	8.99	ns
tDISU	Test Data Input Setup Time	-0.70	-0.70	-0.31	-1.33	-1.02	ns
tDIHD	Test Data Input Hold Time	2.38	2.47	2.13	2.71	2.59	ns
tTMSSU	Test Mode Select Setup Time	-0.86	-1.13	0.26	-1.03	-0.56	ns
tTMDHD	Test Mode Select Hold Time	1.48	1.98	0.21	1.69	1.05	ns
tTRSTREM	ResetB Removal Time	-1.1	-1.38	-0.49	-0.8	-1.07	ns
tTRSTREC	ResetB Recovery Time	-1.1	-1.38	-0.47	-0.8	-1.07	ns
FTCKMAX	TCK Maximum frequency	25	25	25	25	25	MHz

Table 147 • Mathblock With Input Register Used and Output in Bypass Mode
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Mathblock With Input Register Used and Output in Bypass Mode		Speed Grade -1		Units
Parameter	Description	Min	Max	
TMISU	Input Register Setup time	0.149	–	ns
TMIHD	Input Register Hold time	0.08	–	ns
TMSRSTENSU	Synchronous Reset/Enable Setup time	0.185	–	ns
TMSRSTENHD	Synchronous Reset/Enable Hold time	-0.012	–	ns
TMARSTREM	Asynchronous Reset Removal time	-0.005	–	ns
TMARSTREC	Asynchronous Reset Recovery time	0.088	–	ns
TMICQ	Input Register Clock to Output delay	–	2.52	ns
TMCDIN2Q	CDIN to Output delay	–	1.951	ns

Table 148 • Mathblock With Input and Output in Bypass Mode
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Mathblock With Input and Output in Bypass Mode		Speed Grade -1		Units
Parameter	Description	Min	Max	
TMIQ	Input to Output delay	–	2.568	ns
TMCDIN2Q	CDIN to Output delay	–	1.951	ns

20. Flash*Freeze Timing Characteristics

Table 149 • Flash*Freeze Entry and Exit Times
Military Worst-Case conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Symbols	Parameters	Conditions	Entry/Exit Timing	Units	Notes
TFF_ENTRY	Entry time	eNVM and MSS/HPMS PLL = ON	160	μs	1
		eNVM and MSS/HPMS PLL = OFF	215	μs	1

23. PCIe Electrical and Timing AC and DC Characteristics

PCIe® is a high speed, packet-based, point-to-point, low pin count, serial interconnect bus. The IGLOO2 and SmartFusion2 SoC FPGAs has up to four hard high-speed serial interface blocks. Each SERDES block contains a PCIe system block. The PCIe system is connected to the SERDES block.

Table 152 • Transmitter Parameters

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Min	Typ	Max	Units
VTX-DIFF-PP	Differential swing PCIe Gen1	0.8	–	1.2	V
VTX-CM-AC-P	Output common mode voltage PCIe Gen1	–	–	20	mV
VTX-RISE-FALL	Rise and fall time (20% to 80%) PCIe Gen1	0.125	–	–	UI
ZTX-DIFF-DC	Output impedance – differential	80	–	120	Ω
LTX-SKEW	Lane-to-lane TX skew within a SERDES block PCIe Gen1	–	–	500 ps + 2 UI	ps
RLTX-DIFF	Return loss differential mode PCIe Gen1	–10	–	–	dB
RLTX-CM	Return loss common mode PCIe Gen1	–6	–	–	dB
TX-LOCK-RST	Transmit PLL lock time from reset	–	–	10	μs

Table 153 • Receiver Parameters

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Min	Typ	Max	Units
VRX-DIFF-PP-CC	Input levels PCIe Gen1	0.175	–	1.2	V
VRX-CM-DC-P	Input common mode range (DC coupled) Note: PCIe standard mandates AC coupling	NA	NA	NA	–
VRX-CM-AC-P	Input common mode range (AC coupled)	–	–	150	mV
VRX-DIFF-PP-CC	Differential input sensitivity Gen1	0.175	–	–	mV
ZRX-DIFF-DC	Differential input termination	80	100	120	Ω
REXT	External calibration resistor	1,188	1,200	1,212	Ω
CDR-LOCK-RST	CDR relock time from reset	–	–	15	μs
RLRX-DIFF	Return loss differential mode PCIe Gen1	–10	–	–	dB
RLRX-CM	Return loss common mode PCIe Gen1	–6	–	–	dB
	CID limit (set by 8B/10B coding, not the receiver PLL)	–	–	4	UI
VRX-IDLE-DET-DIFF-PP	Signal detect limit	65	–	175	mV

Table 154 • SERDES Reference Clock AC Specifications

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, Worst-Case $V_{DD} = 1.14\text{ V}$

Symbols	Description	Min	Typ	Max	Units
FREFCLK	Reference Clock Frequency	100	–	160	MHz
TRISE	Reference Clock Rise Time	0.6	–	4	V/ns
TFALL	Reference Clock Fall Time	0.6	–	4	V/ns
TCYC	Reference Clock Duty Cycle	40	–	60	%
Mmrefclk	Reference Clock Mismatch	–300	–	300	ppm
SSCref	Reference Spread Spectrum Clock	0	–	5000	ppm

Table 160 • SPI Characteristics

Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Symbol	Description	Conditions	All Devices/Speed Grades			Unit	Notes
			Min	Typ	Max		
sp4	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%-90%)	IO Configuration: LVCMOS 2.5 V - 8mA AC Loading: 35pF Test Conditions: Typical Voltage, 25°C	–	2.77	–	ns	1
sp5	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%-90%)	IO Configuration: LVCMOS 2.5 V - 8mA AC Loading: 35pF Test Conditions: Typical Voltage, 25°C	–	2.90 6	–	ns	1
SPI Master Configuration							
sp6m	SPI_[0 1]_DO setup time	–	(SPI_x_CLK_period/2) – 3.0	–	–	ns	2
sp7m	SPI_[0 1]_DO hold time	–	(SPI_x_CLK_period/2) – 2.5	–	–	ns	2
sp8m	SPI_[0 1]_DI setup time	–	8	–	–	ns	2
sp9m	SPI_[0 1]_DI hold time	–	2.5	–	–	ns	2
SPI Slave Configuration							
sp6s	SPI_[0 1]_DO setup time	–	(SPI_x_CLK_period/2) – 12.0	–	–	ns	2
sp7s	SPI_[0 1]_DO hold time	–	(SPI_x_CLK_period/2) + 3.0	–	–	ns	2
sp8s	SPI_[0 1]_DI setup time	–	2	–	–	ns	2
sp9s	SPI_[0 1]_DI hold time	–	3	–	–	ns	2
Notes: 1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models . 2. For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.							

27. IGLOO2 Specifications

27.1 HPMS Clock Frequency

Table 163 • Maximum Frequency for HPMS Main Clock

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Symbol	Description	Speed Grade –1	Units
HPMS_CLK	Maximum Frequency for the HPMS Main Clock (FCLK)	133	MHz

27.2 IGLOO2 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_0_CLK. For timing parameter definitions, refer to Figure 18 on page 120.

Table 164 • SPI Characteristics

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Symbol	Description	Conditions	All Devices/Speed Grades			Unit	Notes
			Min	Typ	Max		
sp1	SPI_[0 1]_CLK minimum period						
	SPI_[0 1]_CLK = PCLK/2	–	12	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/4	–	24.1	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/8	–	48.2	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/16	–	0.1	–	–	μs	–
	SPI_[0 1]_CLK = PCLK/32	–	0.19	–	–	μs	–
	SPI_[0 1]_CLK = PCLK/64	–	0.39	–	–	μs	–
	SPI_[0 1]_CLK = PCLK/128	–	0.77	–	–	μs	–
sp2	SPI_[0 1]_CLK minimum pulse width high						
	SPI_[0 1]_CLK = PCLK/2	–	6	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/4	–	12.05	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/8	–	24.1	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/16	–	0.05	–	–	μs	–
	SPI_[0 1]_CLK = PCLK/32	–	0.095	–	–	μs	–
	SPI_[0 1]_CLK = PCLK/64	–	0.195	–	–	μs	–
	SPI_[0 1]_CLK = PCLK/128	–	0.385	–	–	μs	–