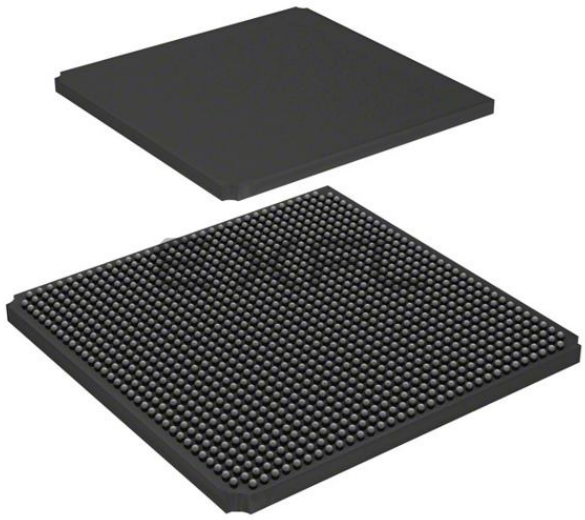

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 146124 |
| Total RAM Bits | 5120000 |
| Number of I/O | 574 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | -55°C ~ 125°C (TJ) |
| Package / Case | 1152-BBGA, FCBGA |
| Supplier Device Package | 1152-FCBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m2gl150ts-1fc1152m |

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# IGLOO2 and SmartFusion2 SoC FPGA Military Grade AC/DC Electrical Characteristics

## 1. Introduction

Microsemi®'s military grade SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) and IGLOO®2 FPGA families integrate an industry standard 4-input lookup table-based (LUT) FPGA fabric with integrated mathblocks, multiple embedded memory blocks, and high-performance SERDES communications interfaces on a single chip. Both families benefit from low power flash technology and are the most secure and reliable FPGAs in the industry. These next generation devices offer up to 150K Logic Elements, up to five MB of embedded RAM, up to 16 SERDES lanes, and up to four PCI Express Gen 1 endpoints, as well as integrated hard DDR3 memory controllers with error correction.

SmartFusion2 military grade devices integrate an entire low power real time Microcontroller Subsystem with a rich set of Industry standard peripherals including Ethernet, USB, and CAN, while the IGLOO2 military devices integrate a high-performance memory subsystem with on-chip flash, 32 Kbyte embedded SRAM, and multiple DMA controllers.

## 2. Device Status

For more information on device status, refer to the "Datasheet Categories".

***Table 1 •*** **IGLOO2 FPGA and SmartFusion2 SoC FPGA Device Status**

| **Design Security Device Densities** | **Status** |
|---|---|
| 010T | Production |
| 025T | Production |
| 050T | Production |
| 060T | Preliminary |
| 090T | Production |
| 150T | Production |
| **Data Security Device Densities** | **Status** |
| 010TS | Production |
| 025TS | Production |
| 050TS | Production |
| 060TS | Preliminary |
| 090TS | Production |
| 150TS | Production |

# 3. Product Briefs and Pin Descriptions

The product brief and pin descriptions are published separately:

- PB0121: IGLOO2 Product Brief
- DS0124: IGLOO2 Pin Descriptions
- PB0115: SmartFusion2 SoC FPGA Product Brief
- DS0115: SmartFusion2 Pin Descriptions

# 4. General Specifications

## 4.1 Operating Conditions

Stresses beyond those listed in Table 2 may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in Table 2 is not implied.

***Table 2 •*** **Absolute Maximum Ratings**

| Symbol | Parameter | Limits | | Units | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| VDD | DC core supply voltage. Must always power this pin. | –0.3 | 1.32 | V | – |
| VPP | Power supply for charge pumps (for normal operation and programming). Must always power this pin. | –0.3 | 3.63 | V | – |
| MSS_MDDR_PLL_VDDA | Analog power pad for MDDR PLL | –0.3 | 3.63 | V | – |
| HPMS_MDDR_PLL_VDDA | Analog power pad for MDDR PLL | –0.3 | 3.63 | V | – |
| FDDR_PLL_VDDA | Analog power pad for FDDR PLL | –0.3 | 3.63 | V | – |
| PLL0_PLL1_MSS_MDDR_VDDA | Analog power pad for MDDR PLL | –0.3 | 3.63 | V | – |
| PLL0_PLL1_HPMS_MDDR_VDDA | Analog power pad for MDDR PLL | –0.3 | 3.63 | V | – |
| CCC_XX[01]_PLL_VDDA | Analog power pad for PLL0–5 | –0.3 | 3.63 | V | – |
| SERDES_[01]_PLL_VDDA | High supply voltage for PLL SERDES[01] | –0.3 | 3.63 | V | – |
| SERDES_[01]_L[0123]_VDDAPLL | Analog power for SERDES[01] PLL lane0 to lane3. This is a +2.5 V SERDES internal PLL supply. | –0.3 | 2.75 | V | – |
| SERDES_[01]_L[0123]_VDDAIO | TX/RX analog I/O voltage. Low voltage power for the lanes of SERDESIF0. This is a +1.2 V SERDES PMA supply. | –0.3 | 1.32 | V | – |
| SERDES_[01]_VDD | PCIe®/PCS power supply | –0.3 | 1.32 | V | – |
| VDDIx | DC FPGA I/O buffer supply voltage for MSIO I/O Bank | –0.3 | 3.63 | V | – |
| | DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O Banks | –0.3 | 2.75 | V | – |
| VI | I/O Input voltage for MSIO I/O Bank | –0.3 | 3.63 | V | – |
| | I/O Input voltage for MSIOD/DDRIO I/O Bank | –0.3 | 2.75 | V | – |
| VPPNVM | Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP. | –0.3 | 3.63 | V | – |

## 8.4 I/O Speeds

***Table 16 •*** **Maximum Data Rate Summary for Worst-Case Military Conditions**

| **Single-Ended I/O** | **MSIO** | **MSIOD** | **DDRIO** | **Units** |
|---|---|---|---|---|
| PCI 3.3 V | 560 | – | – | Mbps |
| LVTTL 3.3 V | 540 | – | – | Mbps |
| LVCMOS 3.3 V | 540 | – | – | Mbps |
| LVCMOS 2.5 V | 360 | 370 | 360 | Mbps |
| LVCMOS 1.8 V | 260 | 360 | 360 | Mbps |
| LVCMOS 1.5 V | 140 | 190 | 210 | Mbps |
| LVCMOS 1.2 V | 100 | 140 | 180 | Mbps |
| LPDDR – LVCMOS 1.8 V Mode | – | – | 360 | Mbps |
| **Voltage-Referenced I/O** | MSIO | MSIOD | DDRIO | Units |
| LPDDR | – | – | 360 | Mbps |
| HSTL1.5 V | – | – | 360 | Mbps |
| SSTL 2.5 V | 450 | 480 | 360 | Mbps |
| SSTL 1.8 V | – | – | 600 | Mbps |
| **Voltage-Referenced I/O** | MSIO | MSIOD | DDRIO | Units |
| SSTL 1.5 V | – | – | 600 | Mbps |
| **Differential I/O** | **MSIO** | **MSIOD** | **DDRIO** | **Units** |
| LVPECL (input only) | 810 | – | – | Mbps |
| LVDS 3.3 V | 480 | 480 | – | Mbps |
| LVDS 2.5 V | 480 | 480 | – | Mbps |
| RSDS | 460 | 480 | – | Mbps |
| BLVDS | 450 | – | – | Mbps |
| MLVDS | 450 | – | – | Mbps |
| Mini-LVDS | 460 | 480 | – | Mbps |

### 8.6.3 2.5 V LVCMOS

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in IGLOO2 FPGA and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-5A.

#### 8.6.3.1 Minimum and Maximum AC/DC Input and Output Levels Specification

**Table 27 • LVCMOS 2.5 V DC Voltage Specification**

| Symbol | Parameters | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| **LVCMOS 2.5 V Recommended DC Operating Conditions** | | | | | | | |
| VDDI | Supply voltage | | 2.375 | 2.5 | 2.625 | V | – |
| **LVCMOS 2.5 V DC Input Voltage Specification** | | | | | | | |
| VIH (DC) | DC input logic High (for MSIOD and DDRIO I/O Bank) | | 1.7 | – | 2.625 | V | – |
| VIH (DC) | DC input logic High (for MSIO I/O Bank) | | 1.7 | – | 2.75 | V | – |
| VIL (DC) | DC input logic Low | | –0.3 | – | 0.7 | V | – |
| IIH (DC) | Input current High | | – | – | 10 | µA | – |
| IIL (DC) | Input current Low | | – | – | 10 | µA | – |
| **LVCMOS 2.5 V DC Output Voltage Specification** | | | | | | | |
| VOH | DC output logic High | | 1.7 | – | – | V | * |
| VOL | DC output logic Low | | – | – | 0.7 | V | * |
| *Note: * The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.* | | | | | | | |

**Table 28 • LVCMOS 2.5 V Maximum AC Switching Speeds**

| Symbol | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Dmax | Maximum data rate (for DDRIO I/O Bank) | AC loading: 17 pF load, maximum drive/slew | – | – | 360 | Mbps |
| Dmax | Maximum data rate (for MSIO I/O Bank) | AC loading: 17 pF load, maximum drive/slew | – | – | 360 | Mbps |
| Dmax | Maximum data rate (for MSIOD I/O Bank) | AC loading: 17 pF load, maximum drive/slew | – | – | 370 | Mbps |

**Table 29 • LVCMOS 2.5 V AC Test Parameters and Driver Impedance Specifications**

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **LVCMOS 2.5 V Calibrated Impedance Option** | | | | | | |
| Rodt_cal | Supported output driver calibrated impedance (for DDRIO I/O Bank) | – | – | 75, 60, 50, 33, 25, 20 | – | Ω |
| **LVCMOS 2.5 V AC Test Parameters Specifications** | | | | | | |
| Vtrip | Measuring/trip point for data path | – | – | 1.2 | – | V |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | – | – | 2k | – | Ω |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | – | – | 5 | – | pF |
| Cload | Capacitive loading for data path ($t_{DP}$) | – | – | 5 | – | pF |

***AC Switching Characteristics for Transmitter (Output and Tristate Buffers)***

***Table 59 •*** **HSTL 15 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V, VDDI = 1.425 V**

| | Speed Grade –1 | | | | | Units |
|---|---|---|---|---|---|---|
| | $t_{DP}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ | |
| **HSTL Class I (for DDRIO I/O Bank)** | | | | | | |
| Single Ended | 2.922 | 2.91 | 2.904 | 3.225 | 3.218 | ns |
| Differential | 2.907 | 2.757 | 2.755 | 2.662 | 2.66 | ns |
| **HSTL Class II (for DDRIO I/O Bank)** | | | | | | |
| Single Ended | 2.817 | 2.735 | 2.735 | 2.644 | 2.644 | ns |
| Differential | 2.827 | 2.81 | 2.803 | 3.205 | 3.197 | ns |

## 8.7.2 Stub-Series Terminated Logic

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in IGLOO2 and SmartFusion2 SoC FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. IGLOO2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

## 8.7.3 Stub-Series Terminated Logic 2.5 V (SSTL2)

SSTL2 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs and also comply with reduced and full drive of double data rate (DDR) standards. IGLOO2 and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

### 8.7.3.1 Minimum and Maximum DC Input and Output Levels Specification

***Table 60 •*** **DDR1/SSTL2 Minimum and Maximum DC Input and Output Levels**

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Recommended DC Operating Conditions** | | | | | | |
| VDDI | Supply voltage | | 2.375 | 2.5 | 2.625 | V |
| VTT | Termination voltage | | 1.164 | 1.250 | 1.339 | V |
| VREF | Input reference voltage | | 1.164 | 1.250 | 1.339 | V |
| **SSTL2 DC Input Voltage Specification** | | | | | | |
| VIH (DC) | DC input logic High | | VREF + 0.15 | – | 2.625 | V |
| VIL (DC) | DC input logic Low | | –0.3 | – | VREF – 0.15 | V |
| IIH (DC) | Input current High | | – | – | 10 | µA |
| IIL (DC) | Input current Low | | – | – | 10 | µA |
| **SSTL2 DC Output Voltage Specification** | | | | | | |
| **SSTL2 Class I (DDR Reduced Drive)** | | | | | | |
| VOH | DC output logic High | | VTT + 0.608 | – | – | V |
| VOL | DC output logic Low | | – | – | VTT – 0.608 | V |
| IOH at VOH | Output minimum source DC current | | 8.1 | – | – | mA |

***Table 64 •*** **DDR2/SSTL18 AC/DC Minimum and Maximum Input and Output Levels Specification (continued)**

| Symbols | Parameters | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| IOL at VOL | Output minimum sink current (DDRIO I/O Bank only) | | –12.0 | – | – | mA | – |
| **SSTL18 DC Differential Voltage Specification** | | | | | | | |
| VID (DC) | DC input differential voltage | | 0.3 | – | – | V | – |
| *Note: *To meet JEDEC Electrical Compliance, use DDR2 Full Drive Transmitter.* | | | | | | | |

***Table 65 •*** **DDR2/SSTL18 AC Specifications (Applicable to DDRIO Bank Only)**

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **SSTL18 AC Differential Voltage Specification** | | | | | | |
| VDIFF (AC) | AC input differential voltage | | 0.5 | – | – | V |
| Vx (AC) | AC differential cross point voltage | | 0.5 × VDDI – 0.175 | – | 0.5 × VDDI + 0.175 | V |
| **SSTL18 Maximum AC Switching Speed** | | | | | | |
| Dmax | Maximum data rate (for DDRIO I/O Bank) | AC loading: per JEDEC specification | – | – | 600 | Mbps |
| **SSTL18 Impedance Specifications** | | | | | | |
| Rref | Supported output driver calibrated impedance (for DDRIO I/O Bank) | Reference resistor = 150 Ω | – | 20, 42 | – | Ω |
| RTT | Effective impedance value (ODT) | Reference resistor = 150 Ω | – | 50, 75, 150 | – | Ω |
| **SSTL18 AC Test Parameters Specifications** | | | | | | |
| Vtrip | Measuring/trip point for data path | | – | 0.9 | – | V |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 2k | – | Ω |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 5 | – | pF |
| Rtt_test | Reference resistance for data test path for SSTL18 Class I ($t_{DP}$) | | – | 50 | – | Ω |
| Rtt_test | Reference resistance for data test path for SSTL18 Class II ($t_{DP}$) | | – | 25 | – | Ω |
| Cload | Capacitive loading for data path ($t_{DP}$) | | – | 5 | – | pF |

***Table 68 •*** **DDR3 SSTL15 DC Voltage Specification (for DDRIO I/O Bank Only) (continued)**

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **SSTL15 DC Output Voltage Specification** | | | | | | |
| **DDR3/SSTL15 Class I (DDR3 Reduced Drive)** | | | | | | |
| VOH | DC output logic High | | 0.8 x VDDI | – | – | V |
| VOL | DC output logic Low | | – | – | 0.2 x VDDI | V |
| IOH at VOH | Output minimum source DC current | | 6.5 | – | – | mA |
| IOL at VOL | Output minimum sink current | | –6.5 | – | – | mA |
| **SSTL15 Class II (DDR3 Full Drive)** | | | | | | |
| VOH | DC output logic High | | 0.8 × VDDI | – | – | V |
| VOL | DC output logic Low | | – | – | 0.2 x VDDI | V |
| IOH at VOH | Output minimum source DC current | | 7.6 | – | – | mA |
| IOL at VOL | Output minimum sink current | | –7.6 | – | – | mA |
| **SSTL15 Differential Voltage Specification** | | | | | | |
| VID | DC input differential voltage | | 0.2 | – | – | V |
| *Note: *To meet JEDEC Electrical Compliance, use DDR3 Full Drive Transmitter.* | | | | | | |

***Table 69 •*** **DDR3/SSTL15 AC Specifications**

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **SSTL15 AC Differential Voltage Specification** | | | | | | |
| VDIFF | AC input differential voltage | | 0.3 | – | – | V |
| Vx | AC differential cross point voltage | | 0.5 × VDDI – 0.150 | – | 0.5 × VDDI + 0.150 | V |
| **SSTL15 Maximum AC Switching Speed (for DDRIO I/O Banks Only)** | | | | | | |
| Dmax | Maximum data rate | AC loading: per JEDEC specifications | – | – | 600 | Mbps |
| **SSTL15 AC Calibrated Impedance Option** | | | | | | |
| Rref | Supported output driver calibrated impedance | Reference resistor = 240 Ω | – | 34, 40 | – | Ω |
| RTT | Effective impedance value (ODT) | Reference resistor = 240 Ω | – | 20, 30, 40, 60, 120 | – | Ω |
| **SSTL15 AC Test Parameters Specifications** | | | | | | |
| Vtrip | Measuring/trip point for data path | | – | 0.75 | – | V |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 2k | – | Ω |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 5 | – | pF |
| Rtt_test | Reference resistance for data test path for SSTL15 Class I ($t_{DP}$) | | – | 50 | – | Ω |
| Rtt_test | Reference resistance for data test path for SSTL15 Class II ($t_{DP}$) | | – | 25 | – | Ω |
| Cload | Capacitive loading for data path ($t_{DP}$) | | – | 5 | – | pF |

### 8.8.1.2 LVDS25 AC Switching Characteristics

#### AC Switching Characteristics for Receiver (Input Buffers)

**Table 85 • LVDS25 Receiver Characteristics**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V, VDDI = 2.375 V**

| | On-Die Termination (ODT) | Speed Grade –1 | Units |
|---|---|---|---|
| | | $t_{PY}$ | |
| **LVDS (for MSIO I/O Bank)** | None | 3.061 | ns |
| | 100 | 3.057 | ns |
| **LVDS (for MSIOD I/O Bank)** | None | 2.792 | ns |
| | 100 | 2.787 | ns |

#### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 86 • LVDS25 Transmitter Characteristics**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V, VDDI = 2.375 V**

| | Speed Grade –1 | | | | | Units |
|---|---|---|---|---|---|---|
| | $t_{DP}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ | |
| **LVDS (for MSIO I/O Bank)** | 2.299 | 2.602 | 2.589 | 2.305 | 2.32 | ns |
| **LVDS (for MSIOD I/O Bank)** | | | | | | |
| No pre-emphasis | 1.656 | 1.845 | 1.838 | 1.992 | 1.969 | ns |
| Min pre-emphasis | 1.583 | 1.868 | 1.866 | 2.018 | 1.998 | ns |
| Med pre-emphasis | 1.559 | 1.893 | 1.886 | 2.045 | 2.021 | ns |

### 8.8.1.3 LVDS33 AC Switching Characteristics

#### AC Switching Characteristics for Receiver (Input Buffers)

**Table 87 • LVDS33 Receiver Characteristics**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V, VDDI = 3.15 V**

| | On Die Termination (ODT) | Speed Grade –1 | Units |
|---|---|---|---|
| | | $t_{PY}$ | |
| **LVDS33 (for MSIO I/O Bank)** | None | 2.763 | ns |
| | 100 | 2.76 | ns |

#### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 88 • LVDS33 Transmitter Characteristics**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V, VDDI = 3.15 V**

| | Speed Grade –1 | | | | | Units |
|---|---|---|---|---|---|---|
| | $t_{DP}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ | |
| **LVDS33 (for MSIO I/O Bank)** | 2.069 | 2.112 | 2.106 | 2.078 | 2.09 | ns |

***Table 109 •*** **Output/Enable Data Register Propagation Delays**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V (continued)**

| Parameter | Description | Measuring Nodes (from, to)* | Speed Grade –1 | Units |
|---|---|---|---|---|
| tORECALn | Asynchronous Load Recovery Time for the Output/Enable Register | C,E | 0.035 | ns |
| tOWALn | Asynchronous Load Minimum Pulse Width for the Output/Enable Register | C,C | 0.266 | ns |
| tOCKMPWH | Clock Minimum Pulse Width High for the Output/Enable Register | E,E | 0.065 | ns |
| tOCKMPWL | Clock Minimum Pulse Width Low for the Output/Enable Register | E,E | 0.139 | ns |

## 8.10 DDR Module Specification

### *8.10.1 Input DDR Module*

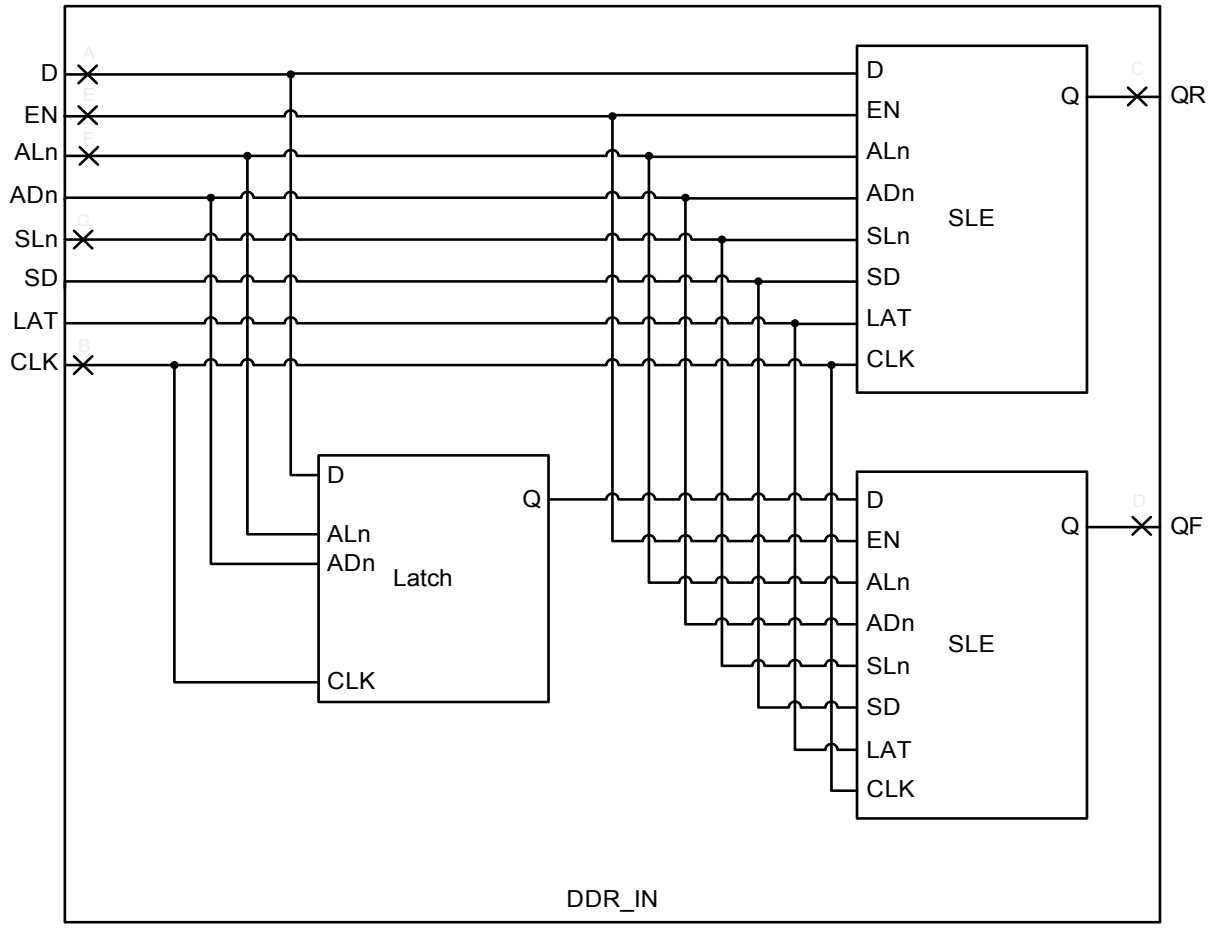


***Figure 9 •*** **Input DDR Module**

## 9.2 Sequential Module

IGLOO2 and SmartFusion2 SoC FPGAs offer a separate flip-flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset).

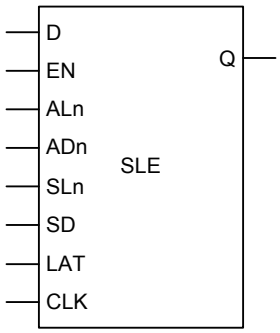


***Figure 14 •*** **Sequential Module**

Figure 15 shows a configuration with SD = 0 (synchronous clear) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

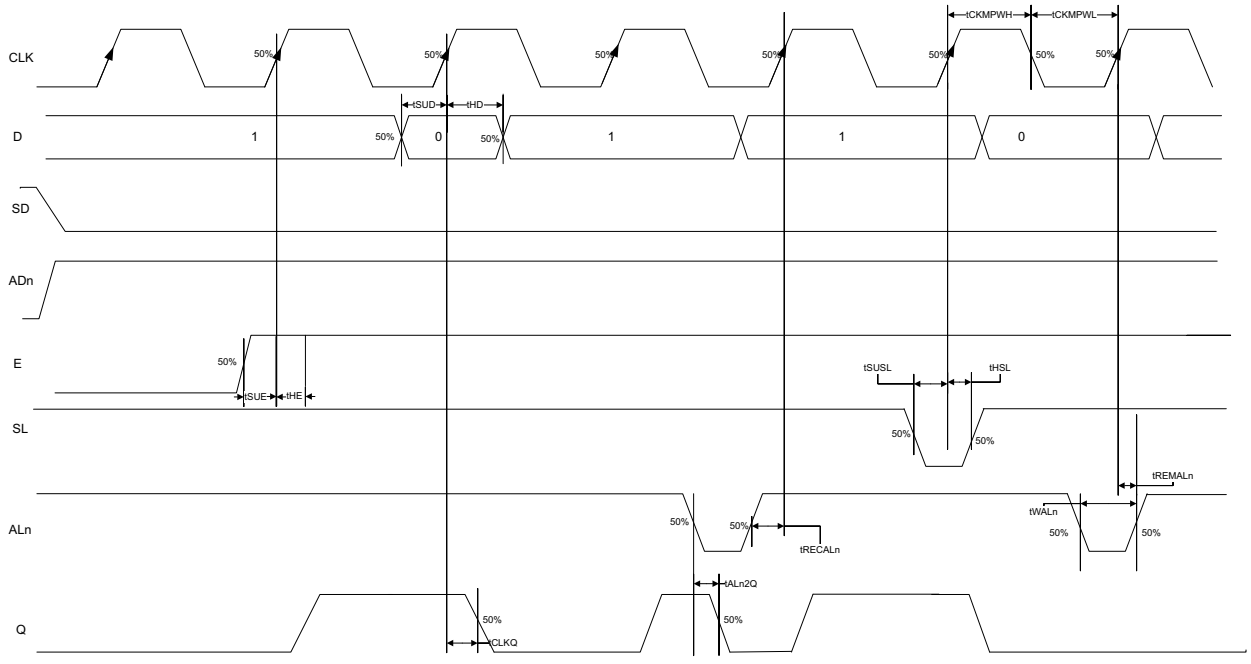


***Figure 15 •*** **Sequential Module Timing Diagram**

# 12. Embedded NVM (eNVM) Characteristics

***Table 132 •*** **eNVM Read Performance**
**Worst-Case Conditions: VDD = 1.14 V, VPPNVM = VPP = 2.375 V**

| Symbol | Description | Operating Temperature Range | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| $T_j$ | Junction Temperature Range | -55°C to 125°C | | -40°C to 100°C | | 0°C to 85°C | | °C |
| Speed grade | | -1 | Std | -1 | Std | -1 | Std | – |
| $F_{MAXREAD}$ | eNVM Maximum Read Frequency | 25 | 25 | 25 | 25 | 25 | 25 | MHz |

***Table 133 •*** **eNVM Page Programming**
**Worst-Case Conditions: VDD = 1.14 V, VPPNVM = VPP = 2.375 V**

| Symbol | Description | Operating Temperature Range | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| $T_j$ | Junction Temperature Range | -55°C to 125°C | | -40°C to 100°C | | 0°C to 85°C | | °C |
| Speed grade | | -1 | Std | -1 | Std | -1 | Std | – |
| $t_{PAGEPGM}$ | eNVM Page Programming Time | 40 | 40 | 40 | 40 | 40 | 40 | ms |

# 15. Clock Conditioning Circuits (CCC)

***Table 139 •*** **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification**
**Military Worst-Case Conditions: $T_J$ = 125°C, VDD = 1.14 V**

| Parameter | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Clock conditioning circuitry input frequency $f_{IN\_CCC}$ | All CCC | 1 | – | 200 | MHz | – |
| | 32 kHz Capable CCC | 0.032 | | 200 | MHz | – |
| Clock conditioning circuitry output frequency $f_{OUT\_CCC}$ | – | 0.078 | – | 400 | MHz | 1 |
| PLL VCO frequency | – | 500 | – | 1000 | MHz | 2 |
| Delay increments in programmable delay blocks | – | – | 75 | 100 | ps | – |
| Number of programmable values in each programmable delay block | – | – | – | 64 | – | – |
| Acquisition time | – | – | 70 | 100 | µs | – |
| Input Duty Cycle (Reference Clock) | Internal Feedback | | | | | |
| | 1 MHz ≤ $f_{IN\_CCC}$ ≤ 25 MHz | 10 | – | 90 | % | – |
| | 25 MHz ≤ $f_{IN\_CCC}$ ≤ 100 MHz | 25 | – | 75 | % | – |
| | 100 MHz ≤ $f_{IN\_CCC}$ ≤ 150 MHz | 35 | – | 65 | % | – |
| | 150 MHz ≤ $f_{IN\_CCC}$ ≤ 200 MHz | 45 | – | 55 | % | – |
| | External Feedback (CCC, FPGA, Off-chip) | | | | | |
| | 1 MHz ≤ $f_{IN\_CCC}$ ≤ 25 MHz | 25 | – | 75 | % | – |
| | 25 MHz ≤ $f_{IN\_CCC}$ ≤ 35 MHz | 35 | – | 65 | % | – |
| | 35 MHz ≤ $f_{IN\_CCC}$ ≤ 50 MHz | 45 | – | 55 | % | – |
| Output duty cycle | 010, 025, and 050 Devices | 46 | – | 52 | % | – |
| | 090 and 150 Devices | 44 | – | 52 | % | – |
| **Spread Spectrum Characteristics** | | | | | | |
| Modulation frequency range | – | 25 | 35 | 50 | kHz | – |
| Modulation depth range | – | 0 | – | 1.5 | % | – |
| Modulation depth control | – | – | 0.5 | – | % | – |

*Notes:*

1. *The minimum output clock frequency is limited by the PLL. For more information refer to the UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide.*
2. *The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance will be limited by the CCC output frequency.*

# 17. DEVRST_N Characteristics

***Table 142 •*** **DEVRST_N Characteristics**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V**

| Symbol | Description | All Devices/Speed Grades | | | Units | Notes |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| TRAMPDEVRSTN | DEVRST_N ramp rate | – | – | 10 | ns | * |
| *Note: * Slower ramp rates are susceptible to board level noise.* | | | | | | |

## 24.3 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to Figure 17 on page 115.

***Table 160 •*** **SPI Characteristics**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V**

| Symbol | Description | Conditions | All Devices/Speed Grades | | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| sp1 | **SPI_[0\|1]_CLK minimum period** | | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | – | 12 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/4 | – | 24.1 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/8 | – | 48.2 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/16 | – | 0.1 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/32 | – | 0.19 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/64 | – | 0.39 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/128 | – | 0.77 | – | – | µs | – |
| sp2 | **SPI_[0\|1]_CLK minimum pulse width high** | | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | – | 6 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/4 | – | 12.05 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/8 | – | 24.1 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/16 | – | 0.05 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/32 | – | 0.095 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/64 | – | 0.195 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/128 | – | 0.385 | – | – | µs | – |
| sp3 | **SPI_[0\|1]_CLK minimum pulse width low** | | | | | | |
| | SPI_[0\|1]_CLK = PCLK/2 | – | 6 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/4 | – | 12.05 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/8 | – | 24.1 | – | – | ns | – |
| | SPI_[0\|1]_CLK = PCLK/16 | – | 0.05 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/32 | – | 0.095 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/64 | – | 0.195 | – | – | µs | – |
| | SPI_[0\|1]_CLK = PCLK/128 | – | 0.385 | – | – | µs | – |

*Notes:*

1. *For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.*

***Table 160 •*** **SPI Characteristics**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V (continued)**

| Symbol | Description | Conditions | All Devices/Speed Grades | | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| sp4 | SPI_[0\|1]_CLK, SPI_[0\|1]_DO, SPI_[0\|1]_SS rise time (10%-90%) | IO Configuration: LVCMOS 2.5 V - 8mA<br>AC Loading: 35pF<br>Test Conditions: Typical Voltage, 25°C | – | 2.77 | – | ns | 1 |
| sp5 | SPI_[0\|1]_CLK, SPI_[0\|1]_DO, SPI_[0\|1]_SS fall time (10%-90%) | IO Configuration: LVCMOS 2.5 V - 8mA<br>AC Loading: 35pF<br>Test Conditions: Typical Voltage, 25°C | – | 2.906 | – | ns | 1 |
| **SPI Master Configuration** | | | | | | | |
| sp6m | SPI_[0\|1]_DO setup time | – | (SPI_x_CLK_period/2) – 3.0 | – | – | ns | 2 |
| sp7m | SPI_[0\|1]_DO hold time | – | (SPI_x_CLK_period/2) – 2.5 | – | – | ns | 2 |
| sp8m | SPI_[0\|1]_DI setup time | – | 8 | – | – | ns | 2 |
| sp9m | SPI_[0\|1]_DI hold time | – | 2.5 | – | – | ns | 2 |
| **SPI Slave Configuration** | | | | | | | |
| sp6s | SPI_[0\|1]_DO setup time | – | (SPI_x_CLK_period/2) – 12.0 | – | – | ns | 2 |
| sp7s | SPI_[0\|1]_DO hold time | – | (SPI_x_CLK_period/2) + 3.0 | – | – | ns | 2 |
| sp8s | SPI_[0\|1]_DI setup time | – | 2 | – | – | ns | 2 |
| sp9s | SPI_[0\|1]_DI hold time | – | 3 | – | – | ns | 2 |

*Notes:*

1. *For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.*