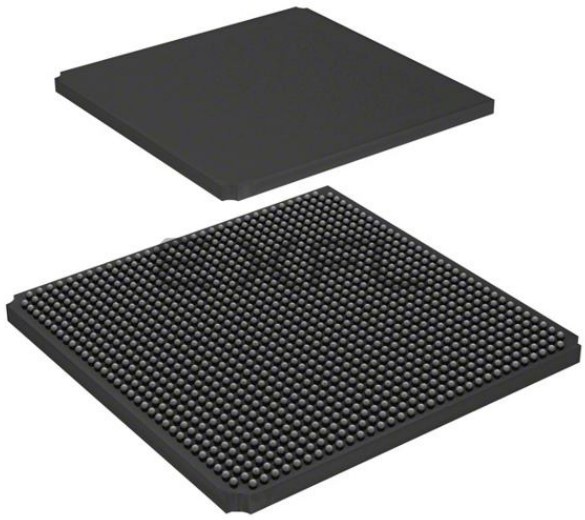

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	146124
Total RAM Bits	5120000
Number of I/O	574
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl150ts-1fcg1152m

List of Figures

IGLOO2 and SmartFusion2 SoC FPGA Military Grade AC/DC Electrical Characteristics

1. Introduction

Microsemi®'s military grade SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) and IGLOO®2 FPGA families integrate an industry standard 4-input lookup table-based (LUT) FPGA fabric with integrated mathblocks, multiple embedded memory blocks, and high-performance SERDES communications interfaces on a single chip. Both families benefit from low power flash technology and are the most secure and reliable FPGAs in the industry. These next generation devices offer up to 150K Logic Elements, up to five MB of embedded RAM, up to 16 SERDES lanes, and up to four PCI Express Gen 1 endpoints, as well as integrated hard DDR3 memory controllers with error correction.

SmartFusion2 military grade devices integrate an entire low power real time Microcontroller Subsystem with a rich set of Industry standard peripherals including Ethernet, USB, and CAN, while the IGLOO2 military devices integrate a high-performance memory subsystem with on-chip flash, 32 Kbyte embedded SRAM, and multiple DMA controllers.

2. Device Status

For more information on device status, refer to the "Datasheet Categories".

Table 1 • **IGLOO2 FPGA and SmartFusion2 SoC FPGA Device Status**

Design Security Device Densities	**Status**
010T	Production
025T	Production
050T	Production
060T	Preliminary
090T	Production
150T	Production
Data Security Device Densities	**Status**
010TS	Production
025TS	Production
050TS	Production
060TS	Preliminary
090TS	Production
150TS	Production

4.3. Thermal Characteristics

4.3.1 Introduction

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures.

EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

where

θ_{JA} = Junction-to-air thermal resistance
θ_{JB} = Junction-to-board thermal resistance
θ_{JC} = Junction-to-case thermal resistance
T_J = Junction temperature
T_A = Ambient temperature
T_B = Board temperature (measured 1.0 mm away from the package edge)
T_C = Case temperature
P = Total power dissipated by the device

Table 7 • **Package Thermal Resistance**

Product M2GL/M2S	θ_{JA}			θ_{JB}	θ_{JC}	Units
	Still Air	1.0 m/s	2.5 m/s			
010						
FG484	18.22	14.83	13.62	8.83	4.92	°C/W
025						
FG484	17.03	13.66	12.45	7.66	4.18	°C/W
050						
FG484	15.29	12.19	10.99	6.27	3.24	°C/W
060						
FG484	15.40	12.06	10.85	6.14	3.15	°C/W
090						
FG484	14.64	11.37	10.16	5.43	2.77	°C/W
150						
FC1152	9.08	6.81	5.87	2.56	0.38	°C/W

Table 15 • **Timing Model Parameters**

Index	Parameter	Description	Speed Grade –1	Units	Notes
A	t_{PY}	Propagation Delay of DDR3 Receiver	1.672	ns	Refer to page 52 for more information
B	t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.165	ns	Refer to page 67 for more information
	t_{ISUD}	Setup Time of the Input Data Register	0.369	ns	Refer to page 67 for more information
C	t_{RCKH}	Input High Delay for Global Clock	1.55	ns	Refer to page 78 for more information
	t_{RCKL}	Input Low Delay for Global Clock	0.861	ns	Refer to page 78 for more information
D	t_{PY}	Input Propagation Delay of LVDS Receiver	3.061	ns	Refer to page 58 for more information
E	t_{DP}	Propagation Delay of a three input AND Gate	0.217	ns	Refer to page 76 for more information
F	t_{DP}	Propagation Delay of a OR Gate	0.17	ns	Refer to page 76 for more information
G	t_{DP}	Propagation Delay of a LVDS Transmitter	2.299	ns	Refer to page 58 for more information
H	t_{DP}	Propagation Delay of a three input XOR Gate	0.236	ns	Refer to page 76 for more information
I	t_{DP}	Propagation Delay of LVCMOS 2.5 V Transmitter, Drive strength of 16mA on the MSIO Bank	2.717	ns	Refer to page 31 for more information
J	t_{DP}	Propagation Delay of a two input NAND Gate	0.17	ns	Refer to page 76 for more information
K	t_{DP}	Propagation Delay of LVCMOS 2.5 V Transmitter, Drive strength of 8mA on the MSIO Bank	2.594	ns	Refer to page 31 for more information
L	t_{CLKQ}	Clock-to-Q of the Data Register	0.112	ns	Refer to page 67 for more information
	t_{SUD}	Setup Time of the Data Register	0.262	ns	Refer to page 67 for more information
M	t_{DP}	Propagation Delay of a two input AND gate	0.17	ns	Refer to page 76 for more information
N	t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.272	ns	Refer to page 69 for more information
	t_{OSUD}	Setup Time of the Output Data Register	0.196	ns	Refer to page 69 for more information

Table 17 • **Maximum Frequency Summary for Worst-Case Military Conditions**

Single-Ended I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
PCI 3.3 V	280	–	–	MHz
LVTTL 3.3 V	270	–	–	MHz
LVCMOS 3.3 V	270	–	–	MHz
LVCMOS 2.5 V	180	185	180	MHz
LVCMOS 1.8 V	130	180	180	MHz
LVCMOS 1.5 V	70	95	105	MHz
LVCMOS 1.2 V	50	70	90	MHz
LPDDR - LVCMOS 1.8 V mode	–	–	180	MHz
Voltage-Referenced I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
LPDDR	–	–	180	MHz
HSTL1.5 V	–	–	180	MHz
SSTL 2.5 V	225	240	180	MHz
SSTL 1.8 V	–	–	300	MHz
SSTL 1.5 V	–	–	300	MHz
Differential I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
LVPECL (input only)	405	–	–	MHz
LVDS 3.3 V	240	240	–	MHz
LVDS 2.5 V	240	240	–	MHz
RSDS	230	240	–	MHz
BLVDS	225	–	–	MHz
MLVDS	225	–	–	MHz
Mini-LVDS	230	240	–	MHz

8.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

8.6.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 21 • LVTTL/LVCMOS 3.3 V DC Voltage Specification (Applicable to MSIO I/O Bank Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units	Notes
LVTTL/LVCMOS 3.3 V Recommended DC Operating Conditions							
VDDI	Supply voltage		3.15	3.3	3.45	V	–
LVTTL/LVCMOS 3.3 V DC Input Voltage Specification							
VIH (DC)	DC input logic High		2.0	–	3.45	V	–
VIL (DC)	DC input logic Low		–0.3	–	0.8	V	–
IIH (DC)	Input current High		–	–	10	µA	–
IIL (DC)	Input current Low		–	–	10	µA	–
LVCMOS 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		2.4	–	–	V	*
VOL	DC output logic Low		–	–	0.4	V	*
LVTTL 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		2.4	–	–	V	–
VOL	DC output logic Low		–	–	0.4	V	–
*Note: * The VOH/VOL test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.*							

Table 22 • LVTTL/LVCMOS 3.3 V Maximum Switching Speeds (Applicable to MSIO I/O Bank Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
LVTTL/LVCMOS 3.3 V Maximum Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	540	Mbps

Table 23 • LVTTL/LVCMOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO Bank Only)

LVTTL/LVCMOS 3.3 V AC Test Parameter Specifications						
Symbol	**Parameters**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Vtrip	Measuring/trip point for data path		–	1.4	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

8.6.4.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 38 • LVCMOS 1.8 V AC Switching Characteristics for Receiver (Input Buffers)
Worst-case Military conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.71 V

	ODT (On Die Termination)	Speed Grade –1		Units
		t_{PY}	t_{PYS}	
LVCMOS 1.8 V (for DDRIO I/O Bank with Fixed Codes)	None	2.071	2.213	ns
LVCMOS 1.8 V (for MSIO I/O Bank)	None	3.185	3.171	ns
	50	3.394	3.397	ns
	75	3.322	3.316	ns
	150	3.252	3.239	ns
LVCMOS 1.8 V (for MSIOD I/O Bank)	None	2.827	2.813	ns
	50	3.043	3.053	ns
	75	2.968	2.963	ns
	150	2.898	2.886	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 39 • LVCMOS 1.8 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-case Military conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.71 V

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVCMOS 1.8 V (for DDRIO I/O Bank with Fixed Codes)							
2 mA	slow	4.681	4.017	4.69	5.388	4.852	ns
	medium	4.211	3.599	4.219	5.058	4.488	ns
	medium_fast	3.978	3.392	3.986	4.874	4.327	ns
	fast	3.953	3.373	3.961	4.858	4.316	ns
4 mA	slow	4.355	3.657	4.346	5.967	5.399	ns
	medium	3.886	3.246	3.879	5.628	5.01	ns
	medium_fast	3.656	3.05	3.647	5.461	4.845	ns
	fast	3.635	3.033	3.626	5.447	4.838	ns
6 mA	slow	4.105	3.422	4.092	6.221	5.599	ns
	medium	3.68	3.05	3.668	5.9	5.257	ns
	medium_fast	3.477	2.867	3.463	5.739	5.118	ns
	fast	3.451	2.849	3.437	5.72	5.104	ns
8 mA	slow	4.015	3.32	3.998	6.458	5.808	ns
	medium	3.59	2.947	3.574	6.129	5.449	ns
	medium_fast	3.383	2.761	3.366	5.963	5.304	ns
	fast	3.357	2.746	3.34	5.954	5.289	ns
10 mA	slow	3.888	3.18	3.864	6.739	6.045	ns
	medium	3.485	2.822	3.467	6.422	5.7	ns
	medium_fast	3.281	2.642	3.26	6.277	5.553	ns
	fast	3.258	2.627	3.238	6.27	5.546	ns

Table 78 • LPDDR-LVCMOS 1.8 V Maximum AC Switching Speeds (Applicable to DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Dmax	Maximum Data Rate (for DDRIO I/O Bank)	AC Loading: 17pF Load, 8mA Drive and Above/All Slew	–	–	360	Mbps

Table 79 • LPDDR-LVCMOS 1.8 V AC Test Parameters and Driver Impedance Specifications (Applicable to DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LPDDR - LVCMOS 1.8 V Calibrated Impedance Option						
Rodt_cal	Supported Output Driver Calibrated Impedance (for DDRIO I/O Bank)	–	–	75, 60, 50, 33, 25, 20	–	Ω
LPDDR- LVCMOS 1.8 V AC Test Parameters Specifications						
Vtrip	Measuring/Trip Point for Data Path	–	–	0.9	–	V
Rent	Resistance for Enable Path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})	–	–	2k	–	Ω
Cent	Capacitive Loading for Enable Path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})	–	–	5	–	pF
Cload	Capacitive Loading for Data Path (t_{DP})	–	–	5	–	pF

Table 80 • LPDDR-LVCMOS 1.8 V Mode Transmitter Drive Strength Specification (Applicable to DDRIO I/O Bank Only)

Output Drive Selection	VOH (V) Min	VOL (V) Max	IOH (at VOH) mA	IOL (at VOL) mA	Notes
2 mA	VDDI – 0.45	0.45	2	2	–
4 mA	VDDI – 0.45	0.45	4	4	–
6 mA	VDDI – 0.45	0.45	6	6	–
8 mA	VDDI – 0.45	0.45	8	8	–
10 mA	VDDI – 0.45	0.45	10	10	–
12 mA	VDDI – 0.45	0.45	12	12	–
16 mA	VDDI – 0.45	0.45	16	16	*
*Note: * 16mA Drive Strengths, All Slews, meet LPDDR JEDEC electrical compliance*					

8.7.6.4 AC Switching Characteristics

Table 81 • LPPDR - LVCMOS 1.8 V AC Switching Characteristics for Receiver (Input Buffers)
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.71 V

	ODT (On Die Termination)	Speed Grade –1		Units
		t_{PY}	t_{PYS}	
LPDDR-LVCMOS 1.8 mode (for DDRIO I/O Bank with Fixed Codes)	None	2.071	2.213	ns

8.8.4 Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

8.8.4.1 Mini-LVDS Minimum and Maximum Input and Output Levels

Table 97 • **Mini-LVDS DC Voltage Specification**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
VDDI	Supply voltage		2.375	2.5	2.625	V
Mini-LVDS DC Input Voltage Specification						
VI	DC Input voltage		0	–	2.925	V
Mini-LVDS DC Output Voltage Specification						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
Mini-LVDS Differential Voltage Specification						
VOD	Differential output voltage swing		300	–	600	mV
VOCM	Output common mode voltage		1	–	1.4	V
VICM	Input common mode voltage		0.3	–	1.2	V
VID	Input differential voltage		100	–	600	mV

Table 98 • **Mini-LVDS AC Specifications**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Mini-LVDS Maximum AC Switching Speed						
Dmax	Maximum data rate (MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	460	Mbps
Dmax	Maximum data rate (MSIOD I/O Bank)	AC loading: 10 pF / 100 Ω differential load	–	–	480	Mbps
Mini-LVDS Impedance Specification						
Rt	Termination resistance		–	100	–	Ω
Mini-LVDS AC Test Parameters Specifications						
VTrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF

8.10.4 Output DDR Module

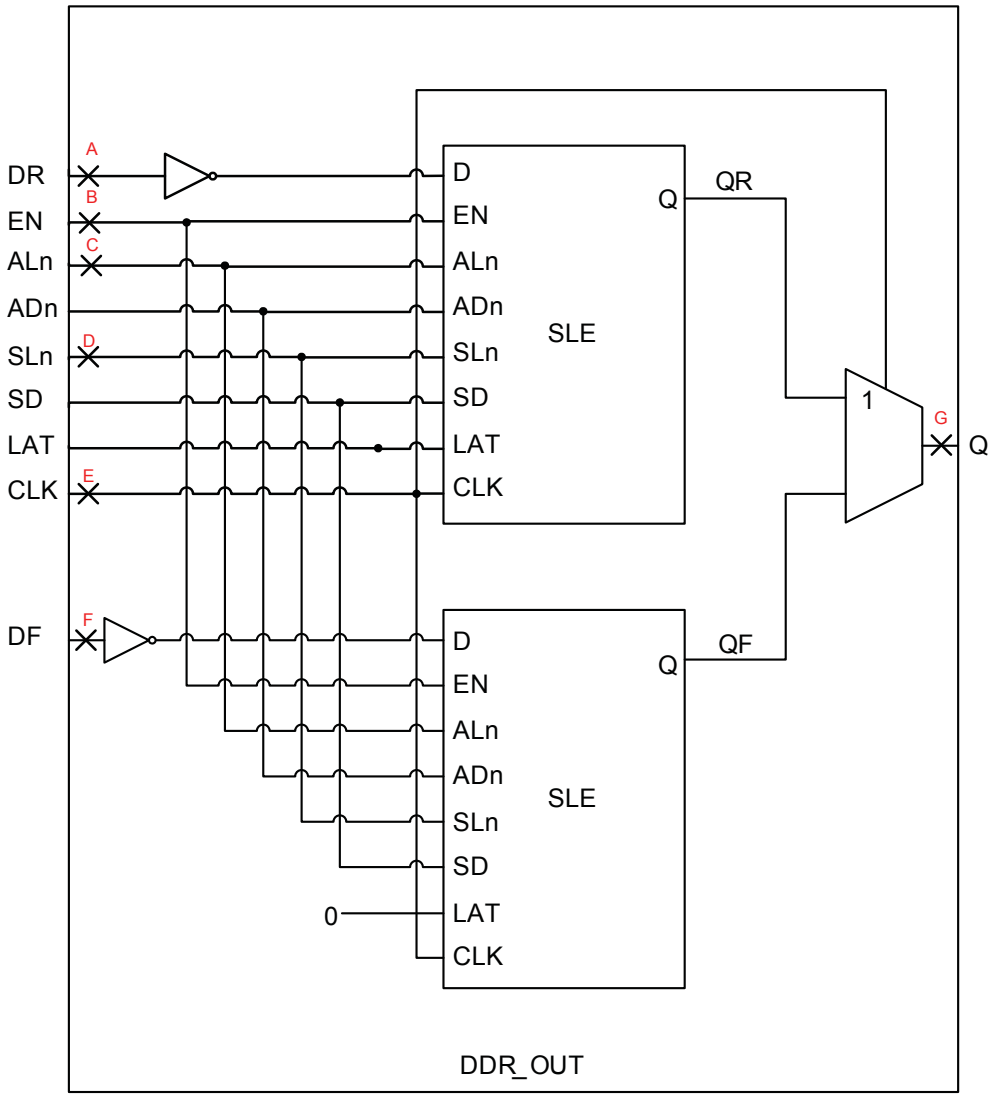

***Figure 11* • Output DDR Module**

Table 119 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1Kx18
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tsrstsu	Synchronous Reset Setup Time	0.233	–	ns
tsrsthd	Synchronous Reset Hold Time	0.037	–	ns
twesu	Write Enable Setup Time	0.402	–	ns
twehd	Write Enable Hold Time	0.25	–	ns
Fmax	Maximum Frequency	–	300	MHz

Table 120 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2Kx9
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tcy	Clock Period	3.333	–	ns
tclkmpwh	Clock Minimum Pulse Width High	1.5	–	ns
tclkmpwl	Clock Minimum pulse Width Low	1.5	–	ns
tplcy	Pipelined Clock Period	3.333	–	ns
tplclkmpwh	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
tplclkmpwl	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.346	ns
	Read Access Time without Pipeline Register	–	2.346	ns
	Access Time with Feed-Through Write Timing	–	1.578	ns
taddrsu	Address Setup Time	0.49	–	ns
taddrhd	Address Hold Time	0.282	–	ns
tdsu	Data Setup Time	0.346	–	ns
tdhd	Data Hold Time	0.084	–	ns
tblksu	Block Select Setup Time	0.214	–	ns
tblkhd	Block Select Hold Time	0.223	–	ns
tblk2q	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	1.578	ns
tblkmpw	Block Select Minimum Pulse Width	0.218	–	ns
trdesu	Read Enable Setup Time	0.5	–	ns
trdehd	Read Enable Hold Time	0.073	–	ns
trdplesu	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
trdplehd	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
tr2q	Asynchronous Reset to Output Propagation Delay	–	1.569	ns

Table 128 • uSRAM (RAM128x8) in 128x8 Mode
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tr2q	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.865	ns
tsrstsu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.062	–	ns
tccy	Write Clock Period	4	–	ns
tcclkmpwh	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclkmpwl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblkcsu	Write Block Setup Time	0.417	–	ns
tblkchd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.104	–	ns
tdinchd	Write Input Data hold Time	0.142	–	ns
taddrcsu	Write Address Setup Time	0.091	–	ns
taddrchd	Write Address Hold Time	0.24	–	ns
twecsu	Write Enable Setup Time	0.41	–	ns
twechd	Write Enable Hold Time	-0.027	–	ns
fmax	Maximum Frequency	–	250	MHz

Table 129 • uSRAM (RAM256x4) in 256x4 Mode
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tcy	Read Clock Period	4	–	ns
tclkmpwh	Read Clock Minimum Pulse Width High	1.8	–	ns
tclkmpwl	Read Clock Minimum pulse Width Low	1.8	–	ns
tplcy	Read Pipe-line clock period	4	–	ns
tplclkmpwh	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
tplclkmpwl	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.812	ns
taddrsu	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	1.993	–	ns
taddrhd	Read Address Hold Time in Synchronous Mode	0.125	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.669	–	ns
trdensu	Read Enable Setup Time	0.287	–	ns

Table 131 • uSRAM (RAM1024x1) in 1024x1 Mode
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tr2q	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.862	ns
tsrstsu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.062	–	ns
tccy	Write Clock Period	4	–	ns
tcclkmpwh	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclkmpwl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblkcsu	Write Block Setup Time	0.417	–	ns
tblkchd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.003	–	ns
tdinchd	Write Input Data hold Time	0.142	–	ns
taddrcsu	Write Address Setup Time	0.091	–	ns
taddrchd	Write Address Hold Time	0.255	–	ns
twecsu	Write Enable Setup Time	0.41	–	ns
twechd	Write Enable Hold Time	-0.027	–	ns
fmax	Maximum Frequency	–	250	MHz

15. Clock Conditioning Circuits (CCC)

Table 139 • **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification**
Military Worst-Case Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Conditions	Min	Typ	Max	Units	Notes
Clock conditioning circuitry input frequency f_{IN_CCC}	All CCC	1	–	200	MHz	–
	32 kHz Capable CCC	0.032		200	MHz	–
Clock conditioning circuitry output frequency f_{OUT_CCC}	–	0.078	–	400	MHz	1
PLL VCO frequency	–	500	–	1000	MHz	2
Delay increments in programmable delay blocks	–	–	75	100	ps	–
Number of programmable values in each programmable delay block	–	–	–	64	–	–
Acquisition time	–	–	70	100	µs	–
Input Duty Cycle (Reference Clock)	Internal Feedback					
	1 MHz ≤ f_{IN_CCC} ≤ 25 MHz	10	–	90	%	–
	25 MHz ≤ f_{IN_CCC} ≤ 100 MHz	25	–	75	%	–
	100 MHz ≤ f_{IN_CCC} ≤ 150 MHz	35	–	65	%	–
	150 MHz ≤ f_{IN_CCC} ≤ 200 MHz	45	–	55	%	–
	External Feedback (CCC, FPGA, Off-chip)					
	1 MHz ≤ f_{IN_CCC} ≤ 25 MHz	25	–	75	%	–
	25 MHz ≤ f_{IN_CCC} ≤ 35 MHz	35	–	65	%	–
	35 MHz ≤ f_{IN_CCC} ≤ 50 MHz	45	–	55	%	–
Output duty cycle	010, 025, and 050 Devices	46	–	52	%	–
	090 and 150 Devices	44	–	52	%	–
Spread Spectrum Characteristics						
Modulation frequency range	–	25	35	50	kHz	–
Modulation depth range	–	0	–	1.5	%	–
Modulation depth control	–	–	0.5	–	%	–

Notes:

1. *The minimum output clock frequency is limited by the PLL. For more information refer to the UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide.*
2. *The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance will be limited by the CCC output frequency.*

18. System Controller SPI Characteristics

Table 143 • **System Controller SPI Characteristics**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Symbol	Description	Conditions	All Devices/Speed Grades			Units	Notes
			Min	Typ	Max		
sp1	SC_SPI_SCK minimum period	–	20	–	–	ns	–
sp2	SC_SPI_SCK minimum pulse width high	–	10	–	–	ns	–
sp3	SC_SPI_SCK minimum pulse width low	–	10	–	–	ns	–
sp4	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS rise time (10%-90%) 1	I/O Configuration: LVTTL 3.3V- 20mA AC Loading: 35pF Test Conditions: Typical Voltage, 25C	–	1.239	–	ns	*
sp5	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS fall time (10%-90%) 1	I/O Configuration: LVTTL 3.3V- 20mA AC Loading: 35pF Test Conditions: Typical Voltage, 25C	–	1.245	–	ns	*
sp6	Data from master (SC_SPI_SDO) setup time	–	160	–	–	ns	–
sp7	Data from master (SC_SPI_SDO) hold time	–	160	–	–	ns	–
sp8	SC_SPI_SDI setup time	–	20	–	–	ns	–
sp9	SC_SPI_SDI hold time	–	20	–	–	ns	–

*Note: *For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models. Use the supported I/O Configurations for the System Controller SPI in Table 144.*

Table 144 • **Supported I/O Configurations for System Controller SPI (for MSIO Bank Only)**

Voltage Supply	I/O Drive Configuration	Units
3.3 V	20	mA
2.5 V	16	mA
1.8 V	12	mA
1.5 V	8	mA
1.2 V	4	mA

23. PCIe Electrical and Timing AC and DC Characteristics

PCIe® is a high speed, packet-based, point-to-point, low pin count, serial interconnect bus. The IGLOO2 and SmartFusion2 SoC FPGAs has up to four hard high-speed serial interface blocks. Each SERDES block contains a PCIe system block. The PCIe system is connected to the SERDES block.

Table 152 • **Transmitter Parameters**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Min	Typ	Max	Units
VTX-DIFF-PP	Differential swing PCIe Gen1	0.8	–	1.2	V
VTX-CM-AC-P	Output common mode voltage PCIe Gen1	–	–	20	mV
VTX-RISE-FALL	Rise and fall time (20% to 80%) PCIe Gen1	0.125	–	–	UI
ZTX-DIFF-DC	Output impedance – differential	80	–	120	Ω
LTX-SKEW	Lane-to-lane TX skew within a SERDES block PCIe Gen1	–	–	500 ps + 2 UI	ps
RLTX-DIFF	Return loss differential mode PCIe Gen1	–10	–	–	dB
RLTX-CM	Return loss common mode PCIe Gen1	–6	–	–	dB
TX-LOCK-RST	Transmit PLL lock time from reset	–	–	10	µs

Table 153 • **Receiver Parameters**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Min	Typ	Max	Units
VRX-DIFF-PP-CC	Input levels PCIe Gen1	0.175	–	1.2	V
VRX-CM-DC-P	Input common mode range (DC coupled) Note: PCIe standard mandates AC coupling	NA	NA	NA	–
VRX-CM-AC-P	Input common mode range (AC coupled)	–	–	150	mV
VRX-DIFF-PP-CC	Differential input sensitivity Gen1	0.175	–	–	mV
ZRX-DIFF-DC	Differential input termination	80	100	120	Ω
REXT	External calibration resistor	1,188	1,200	1,212	Ω
CDR-LOCK-RST	CDR relock time from reset	–	–	15	µs
RLRX-DIFF	Return loss differential mode PCIe Gen1	–10	–	–	dB
RLRX-CM	Return loss common mode PCIe Gen1	–6	–	–	dB
	CID limit (set by 8B/10B coding, not the receiver PLL)	–	–	4	UI
VRX-IDLE-DET-DIFF-PP	Signal detect limit	65	–	175	mV

Table 154 • **SERDES Reference Clock AC Specifications**
Worst-Case Military Conditions: T_J = 125°C, Worst-Case VDD = 1.14V

Symbols	Description	Min	Typ	Max	Units
FREFCLK	Reference Clock Frequency	100	–	160	MHz
TRISE	Reference Clock Rise Time	0.6	–	4	V/ns
TFALL	Reference Clock Fall Time	0.6	–	4	V/ns
TCYC	Reference Clock Duty Cycle	40	–	60	%
Mmrefclk	Reference Clock Mismatch	-300	–	300	ppm
SSCref	Reference Spread Spectrum Clock	0	–	5000	ppm

25. CAN Controller Characteristics

Table 161 • **CAN Controller Characteristics**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Min	Typ	Max	Units	Notes
FCANREFCLK	Internally Sourced CAN Reference Clock Frequency	–	–	128	MHz	*
BAUDCAN	CAN Performance Baud Rate	0.05	–	1	Mbps	–
Note: PCLK to CAN controller must be a multiple of 8 MHz.						

Table 164 • SPI Characteristics
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Symbol	Description	Conditions	All Devices/Speed Grades			Unit	Notes
			Min	Typ	Max		
sp9s	SPI_[0|1]_DI hold time	–	3	–	–	ns	2

Notes:

1. *For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.*

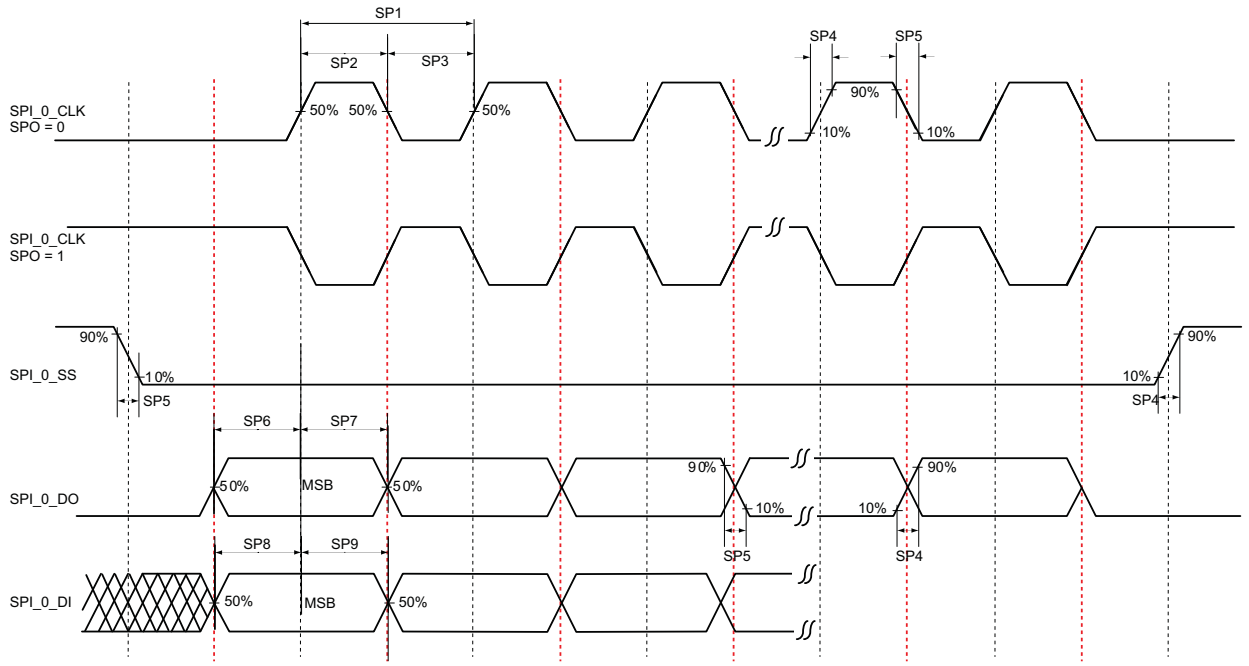

Figure 18 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)

Safety Critical, Life Support, and High-Reliability Applications Policy

The products described in this advance status document may not have completed the Microsemi qualification process. Products may be amended or enhanced during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult the Microsemi SoC Products Group Terms and Conditions for specific liability exclusions relating to life-support applications.

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