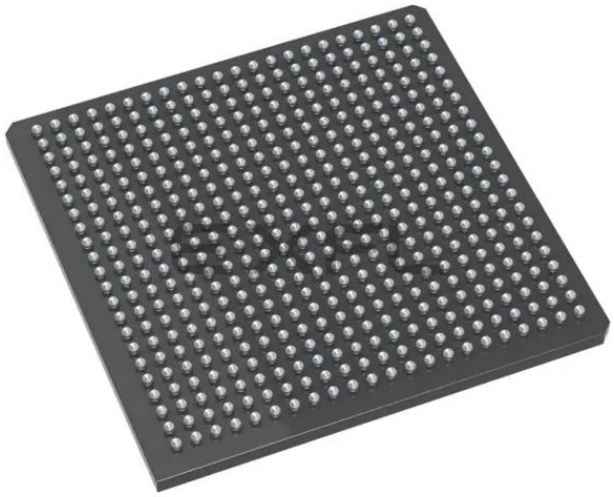

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 10K Logic Modules
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s010t-1fgg484m

List of Tables

IGLOO2 and SmartFusion2 SoC FPGA Military Grade AC/DC Electrical Characteristics

1. Introduction

Microsemi®'s military grade SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) and IGLOO®2 FPGA families integrate an industry standard 4-input lookup table-based (LUT) FPGA fabric with integrated mathblocks, multiple embedded memory blocks, and high-performance SERDES communications interfaces on a single chip. Both families benefit from low power flash technology and are the most secure and reliable FPGAs in the industry. These next generation devices offer up to 150K Logic Elements, up to five MB of embedded RAM, up to 16 SERDES lanes, and up to four PCI Express Gen 1 endpoints, as well as integrated hard DDR3 memory controllers with error correction.

SmartFusion2 military grade devices integrate an entire low power real time Microcontroller Subsystem with a rich set of Industry standard peripherals including Ethernet, USB, and CAN, while the IGLOO2 military devices integrate a high-performance memory subsystem with on-chip flash, 32 Kbyte embedded SRAM, and multiple DMA controllers.

2. Device Status

For more information on device status, refer to the "Datasheet Categories".

Table 1 • **IGLOO2 FPGA and SmartFusion2 SoC FPGA Device Status**

Design Security Device Densities	**Status**
010T	Production
025T	Production
050T	Production
060T	Preliminary
090T	Production
150T	Production
Data Security Device Densities	**Status**
010TS	Production
025TS	Production
050TS	Production
060TS	Preliminary
090TS	Production
150TS	Production

Table 3 • **Recommended Operating Conditions (continued)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
VPPNVM	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–

Notes:

1. *Programming at this temperature range is available only with VPP in 3.3 V Range*
2. *Power supply ramps must all be strictly monotonic, without plateaus.*

Table 4 • **FPGA Operating Limits**

Product Grade	Element	Programming Temperature	Operating Temperature	Programming Cycles	Retention (Biased/Unbiased)	Note
Military	FPGA	Min T_J = 0°C Max T_J = 85°C	Min T_J = -55°C Max T_J = 125°C	500	10 Years	–
		Min T_J = -40°C Max T_J = 100°C	Min T_J = -55°C Max T_J = 125°C	500	10 Years	*

*Note: *: Programming at this temperature range is available only with VPP in 3.3 V Range*

Table 5 • **Embedded Flash Limits**

Product Grade	Element	Programming Temperature	Maximum Operating Temperature	Programming Cycles	Retention (Biased/Unbiased)
Military	Embedded flash	Min T_J = -55°C Max T_J = 125°C	Min T_J = -55°C Max T_J = 125°C	< 10,000 cycles per pages, up to one million cycles per eNVM array	10 Years

Table 6 • **Device Storage Temperature and Retention**

Product Grade	Storage Temperature (Tstg)	Retention
Military	Min T_J = -55°C Max T_J = 125°C	10 Years

4.2 Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to -1.0 V for no longer than 10% or the period. The current during the transition must not exceed 100mA.

For AC signals, the input signal may overshoot during transitions to VCCI + 1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100mA.

Note: The above specification does not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant to the PCI standard including the PCI overshoot/undershoot specifications.

5. Power Consumption

5.1 Quiescent Supply Current

Table 8 • **Quiescent Supply Current Characteristics**

Power Supplies/Blocks	Modes and Configurations		Notes
	Non-Flash*Freeze Mode	Flash*Freeze Mode	
FPGA Core	On	Off	–
VDD / SERDES_[01]_VDD	On	On	1
VPP / VPPNVM	On	On	–
MDDR_PLL_VDDA CCC_XX[01]_PLL_VDDA PLL0_PLL1_MDDR_VDDA FDDR_PLL_VDDA	0 V	0 V	–
SERDES_[01]_PLL_VDDA	0 V	0 V	3
SERDES_[01]_L[0123]_VDDAPLL / VDD_2V5	On	On	3
SERDES_[01]_L[0123]_VDDAIIO	On	On	3
VDDIx	On	On	2, 4
VREFx	On	On	–
MSSDDR CLK	32 kHz	32 kHz	–
RAM	On	Sleep state	–
HPMS Controller	50 MHz	50 MHz	–
50 MHz Oscillator (enable/disable)	Enabled	Disabled	–
1 MHz Oscillator (enable/disable)	Disabled	Disabled	–
Crystal Oscillator (enable/disable)	Disabled	Disabled	–

Notes:

1. *SERDES_[01]_VDD Power Supply is shorted to VDD.*
2. *VDDIx has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate VDDI Bank supplies. For details on bank power supplies, refer to the "Recommendation for Unused Bank Supplies" table in the AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note.*
3. *SERDES and DDR blocks to be unused.*
4. *No Differential (that is to say, LVDS) I/O's or ODT attributes to be used.*

Table 9 • **SmartFusion2 and IGLOO2 Quiescent Supply Current – Typical Process**

Parameter	Modes	Conditions	010	025	050	090	150	Units
			VDD=1.2 V	VDD=1.2 V	VDD=1.2 V	VDD=1.2 V	VDD=1.2 V	
IDC1	Non-Flash*Freeze	Typical (T_J = 25°C)	6.9	8.9	13.1	15.4	27.5	mA
		Military (T_J = 125°C)	73.0	106.4	180.9	217.5	390.5	mA
IDC2	Flash*Freeze	Typical (T_J = 25°C)	2.6	3.7	5.1	5.1	8.9	mA
		Military (T_J = 125°C)	55.6	74.2	98.5	99.5	161.0	mA

Table 13 • **Inrush Currents at Power up, –55°C <= T_J <=125°C, Typical Process**

VDDI	2.62	141	161	187	283	404	mA
Number of banks		8	8	10	9	19	–

6. Average Fabric Temperature and Voltage Derating Factors

Table 14 • **Average Temperature and Voltage Derating Factors for Fabric Timing Delays**
(Normalized to T_J = 125°C, Worst-Case VDD = 1.14 V)

Core Voltage VDD (V)	Junction Temperature (°C)							
	–55°C	–40°C	0°C	25°C	70°C	85°C	100°C	125°C
1.14	0.91	0.91	0.93	0.94	0.96	0.97	0.98	1.00
1.2	0.82	0.83	0.84	0.85	0.87	0.87	0.88	0.90
1.26	0.75	0.75	0.77	0.77	0.79	0.80	0.81	0.75

Table 15 • **Timing Model Parameters (continued)**

Index	Parameter	Description	Speed Grade –1	Units	Notes
O	t_{DP}	Propagation Delay of SSTL2, Class I Transmitter on the MSIO Bank	2.283	ns	Refer to page 47 for more information
P	t_{DP}	Propagation Delay of LVCMOS 1.5 V Transmitter, Drive strength of 12mA, fast slew on the DDRIO Bank	3.703	ns	Refer to page 38 for more information

8. User I/O Characteristics

There are three types of I/Os supported in the IGLOO2 FPGA and SmartFusion2 SoC FPGA families: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the “I/Os” section of the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

8.1 Input Buffer and AC Loading

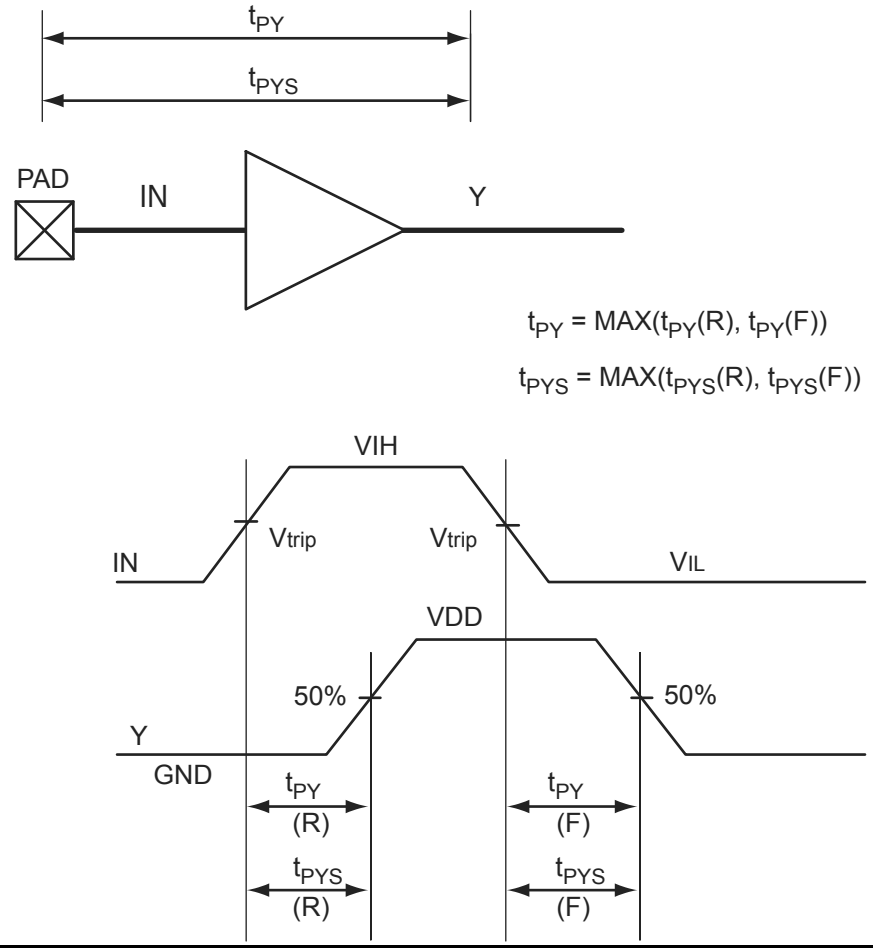

Figure 2 • **Input Buffer AC Loading**

Table 39 • **LVCMOS 1.8 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
Worst-case Military conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.71 V (continued)

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
12 mA	slow	3.795	3.096	3.773	6.773	6.067	ns
	medium	3.408	2.764	3.389	6.47	5.743	ns
	medium_fast	3.215	2.599	3.194	6.346	5.61	ns
	fast	3.196	2.584	3.175	6.335	5.604	ns
16 mA	slow	3.744	3.035	3.719	6.944	6.207	ns
	medium	3.358	2.712	3.339	6.657	5.868	ns
	medium_fast	3.175	2.546	3.153	6.547	5.751	ns
	fast	3.156	2.531	3.133	6.541	5.747	ns
LVCMOS 1.8 V (for MSIO I/O Bank)							
2 mA	slow	3.957	4.784	5.023	5.643	5.866	ns
4 mA	slow	3.668	4.162	4.485	6.543	6.382	ns
6 mA	slow	3.586	3.994	4.358	7.622	6.941	ns
8 mA	slow	3.616	3.782	4.162	7.988	7.161	ns
10 mA	slow	3.662	3.732	4.121	8.396	7.423	ns
12 mA	slow	3.75	3.615	4.006	8.576	7.543	ns
LVCMOS 1.8 V (for MSIOD I/O Bank)							
2 mA	slow	3.048	3.692	3.898	5.818	5.609	ns
4 mA	slow	2.5	3.088	3.288	6.421	6.121	ns
6 mA	slow	2.225	2.747	2.937	7.18	6.753	ns
8 mA	slow	2.233	2.72	2.904	7.49	6.992	ns
10 mA	slow	2.263	2.577	2.759	7.851	7.253	ns

8.6.5 1.5 V LVCMOS

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-11A.

8.6.5.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 40 • **LVCMOS 1.5 V Minimum and Maximum DC Input and Output Levels**

Symbols	Parameters	Min	Typ	Max	Units
LVCMOS 1.5 V Recommended DC Operating Conditions					
VDDI	Supply voltage	1.425	1.5	1.575	V
LVCMOS 1.5 V DC Input Voltage Specification					
VIH (DC)	DC input logic High for (MSIOD and DDRIO I/O banks)	0.65 × VDDI	–	1.575	V
VIH (DC)	DC input logic High (for MSIO I/O Bank)	0.65 × VDDI	–	2.75	V
VIL (DC)	DC input logic Low	–0.3	–	0.35 × VDDI	V
IIH (DC)	Input current High	–	–	10	µA
IIL (DC	Input current Low	–	–	10	µA
LVCMOS 1.5 V DC Output Voltage Specification					
VOH	DC output logic High	VDDI × 0.75	–	–	V
VOL	DC output logic Low	–	–	VDDI × 0.25	V

Table 51 • **LVCMOS 1.2 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
Worst-Case Military Conditions: T_J=125°C, VDD=1.14 V, VDDI= 1.14 V (continued)

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVCMOS 1.2 V (for MSIOD I/O Bank)							
2 mA	slow	4.048	5.123	5.552	8.401	7.824	ns
4 mA	slow	3.941	4.406	4.814	9.422	8.656	ns

8.6.7 3.3 V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3 V standards specify support for 33 MHz and 66 MHz PCI bus applications.

8.6.7.1 Minimum and Maximum Input and Output Levels Specification

Table 52 • **PCI/PCI-X DC Voltage Specification (Applicable to MSIO Bank Only**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
PCI/PCIX Recommended DC Operating Conditions						
VDDI	Supply voltage		3.15	3.3	3.45	V
PCI/PCIX DC Input Voltage Specification						
VI	DC input voltage		0	–	3.45	V
IIH(DC)	Input current High		–	–	10	µA
IIL(DC)	Input current Low		–	–	10	µA
PCI/PCIX DC Output Voltage Specification						
VOH	DC output logic High		Per PCI Specification			V
VOL	DC output logic Low		Per PCI Specification			V

Table 53 • **PCI/PCI-X AC Specifications (Applicable to MSIO Bank Only)**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
PCI/PCI-X AC Specifications						
Dmax	Maximum data rate (MSIO I/O Bank)	AC Loading: per JEDEC specifications	–	–	560	Mbps
PCI/PCI-X AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path (falling edge)		–	0.615 × VDDI	–	V
Vtrip	Measuring/trip point for data path (rising edge)		–	0.285 × VDDI	–	V
Rtt_test	Resistance for data test path		–	25	–	Ω
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})		–	10	–	pF

8.7.3.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 62 • DDR1/SSTL2 AC Switching Characteristics for Receiver (Input Buffers)
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V, VDDI= 2.375 V

	ODT (On Die Termination)	Speed Grade –1	Units
		t_{PY}	
SSTL2 (DDRIO I/O Bank)			
Pseudo-Differential	None	1.613	ns
True-Differential	None	1.647	ns
SSTL2 (MSIO I/O Bank)			
Pseudo-Differential	None	3.083	ns
True-Differential	None	3.028	ns
SSTL2 (MSIOD I/O Bank)			
Pseudo-Differential	None	2.721	ns
True-Differential	None	2.71	ns

Table 63 • DDR1/SSTL2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V, VDDI= 2.375 V

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
SSTL2 Class I						
DDRIO I/O Bank						
Single Ended	2.457	2.145	2.137	2.302	2.293	ns
Differential	2.454	2.38	2.375	2.589	2.584	ns
MSIO I/O Bank						
Single Ended	2.283	2.255	2.243	2.286	2.273	ns
Differential	2.434	2.702	2.691	2.39	2.381	ns
MSIOD I/O Bank						
Single Ended	1.646	1.59	1.589	1.82	1.818	ns
Differential	1.774	1.93	1.926	2.012	2.007	ns
SSTL2 Class II						
DDRIO I/O Bank						
Single Ended	2.317	2.06	2.053	2.229	2.221	ns
Differential	2.32	2.213	2.21	2.57	2.565	ns

8.8.4.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 99 • Mini-LVDS AC Switching Characteristics for Receiver (Input Buffers)
Worst-case Military Conditions: T_J = 125°C, VDD = 1.14 V, VDDI= 2.375 V

	On-Die Termination (ODT)	Speed Grade –1	Units
		t_{PY}	
Mini-LVDS (for MSIO I/O Bank)	None	3.112	ns
	100	2.995	ns
Mini-LVDS (for MSIOD I/O Bank)	None	2.612	ns
	100	2.612	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 100 • Mini-LVDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-case Military Conditions: T_J = 125°C, VDD = 1.14 V, VDDI= 2.375 V

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
Mini-LVDS (for MSIO I/O Bank)	2.3	2.602	2.59	2.306	2.32	ns
Mini-LVDS (for MSIOD I/O Bank)						
No pre-emphasis	1.652	1.84	1.833	1.988	1.965	ns
Min pre-emphasis	1.652	1.84	1.833	1.988	1.965	ns
Med pre-emphasis	1.577	1.868	1.86	2.02	1.994	ns
Max pre-emphasis	1.555	1.894	1.883	2.048	2.019	ns

8.10.5 Timing Characteristics

Table 111 • Output DDR Propagation Delays
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Measuring Nodes (from, to)	Speed Grade –1	Units
tDDROCLKQ	Clock-to-Out of DDR for Output DDR	E,G	0.272	ns
tDDROSUDF	DF Data Setup for Output DDR	F,E	0.148	ns
tDDROSUDR	DR Data Setup for Output DDR	A,E	0.196	ns
tDDROHDF	DF Data Hold for Output DDR	F,E	0	ns
tDDROHDR	DR Data Hold for Output DDR	A,E	0	ns
tDDROSUE	Enable Setup for Output DDR	B,E	0.433	ns
tDDROHE	Enable Hold for Output DDR	B,E	0	ns
tDDROSUSLn	Synchronous Load Setup for Output DDR	D,E	0.203	ns
tDDROHSLn	Synchronous Load Hold for Output DDR	D,E	0	ns
tDDROAL2Q	Asynchronous Load-to-Out for Output DDR	C,G	0.545	ns
tDDROREMAL	Asynchronous Load Removal time for Output DDR	C,E	0	ns
tDDRORECAL	Asynchronous Load Recovery time for Output DDR	C,E	0.035	ns
tDDROWAL	Asynchronous Load Minimum Pulse Width for Output DDR	C,C	0.266	ns
tDDROCKMPWH	Clock Minimum Pulse Width High for the Output DDR	E,E	0.065	ns
tDDROCKMPWL	Clock Minimum Pulse Width Low for the Output DDR	E,E	0.139	ns

Table 115 • **M2S090T Device Global Resource (continued)**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tRCKH	Input High Delay for Global Clock	1.412	1.498	ns
tRCKSW	Maximum Skew for Global Clock	–	0.086	ns

Table 116 • **M2S050T Device Global Resource**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tRCKL	Input Low Delay for Global Clock	0.793	0.861	ns
tRCKH	Input High Delay for Global Clock	1.436	1.55	ns
tRCKSW	Maximum Skew for Global Clock	–	0.114	ns

Table 117 • **M2S025T Device Global Resource**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tRCKL	Input Low Delay for Global Clock	0.713	0.762	ns
tRCKH	Input High Delay for Global Clock	1.306	1.391	ns
tRCKSW	Maximum Skew for Global Clock	–	0.085	ns

Table 118 • **M2S010T Device Global Resource**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tRCKL	Input Low Delay for Global Clock	0.598	0.639	ns
tRCKH	Input High Delay for Global Clock	1.116	1.192	ns
tRCKSW	Maximum Skew for Global Clock	–	0.076	ns

Table 120 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2Kx9**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
trstrem	Asynchronous Reset Removal Time	0.522	–	ns
trstrec	Asynchronous Reset Recovery Time	0.005	–	ns
trstmpw	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
tplrstrem	Pipelined Register Asynchronous Reset Removal Time	-0.288	–	ns
tplrstrec	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
tplrstmpw	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
tsrstsu	Synchronous Reset Setup Time	0.233	–	ns
tsrsthd	Synchronous Reset Hold Time	0.037	–	ns
twesu	Write Enable Setup Time	0.428	–	ns
twehd	Write Enable Hold Time	0.05	–	ns
Fmax	Maximum Frequency	–	300	MHz

Table 121 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4Kx4**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		
		Min	Max	Units
tcy	Clock Period	3.333	–	ns
tclkmpwh	Clock Minimum Pulse Width High	1.5	–	ns
tclkmpwl	Clock Minimum pulse Width Low	1.5	–	ns
tplcy	Pipelined Clock Period	3.333	–	ns
tplclkmpwh	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
tplclkmpwl	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.334	ns
	Read Access Time without Pipeline Register	–	2.346	ns
	Access Time with Feed-Through Write Timing	–	1.56	ns
taddrsu	Address Setup Time	0.56	–	ns
taddrhd	Address Hold Time	0.282	–	ns
tdsu	Data Setup Time	0.345	–	ns
tdhd	Data Hold Time	0.084	–	ns
tblksu	Block Select Setup Time	0.214	–	ns
tblkhd	Block Select Hold Time	0.223	–	ns
tblk2q	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	1.56	ns
tblkmpw	Block Select Minimum Pulse Width	0.218	–	ns

Table 136 • **Electrical Characteristics of the Crystal Oscillator – Low Gain Mode (32 kHz)**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Min	Typ	Max	Units
IDYNXTAL	Operating current	–	0.044	–	mA
VIHXTAL	Input logic level High	0.9 × VPP	–	–	V
VILXTAL	Input logic level Low	–	–	0.1 × VPP	V
SUXTAL	Startup time (with regard to stable oscillator output)	–	–	120	ms

14. On-Chip Oscillator

Table 137 and Table 138 describe the electrical characteristics of the available on-chip oscillators in the IGLOO2 FPGAs and SmartFusion2 SoC FPGAs.

Table 137 • **Electrical Characteristics of the 50 MHz RC Oscillator**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Condition	Min	Typ	Max	Units
F50RC	Operating frequency	–	–	50	–	MHz
ACC50RC	Accuracy	–	–	1	8	%
CYC50RC	Output duty cycle	–	–	49–51	46–54	%
JIT50RC	Output jitter (peak to peak)	Period Jitter	–	200	500	ps
		Cycle-to-Cycle Jitter	–	320	900	ps
IDYN50RC	Operating current	–	–	8.5	–	mA

Table 138 • **Electrical Characteristics of the 1 MHz RC Oscillator**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Condition	Min	Typ	Max	Units
F1RC	Operating frequency	–	–	1	–	MHz
ACC1RC	Accuracy	–	–	1	6	%
CYC1RC	Output duty cycle	–	–	49–51	46.5–53.5	%
JIT1RC	Output jitter (peak to peak)	Period Jitter	–	10	36	ps
		Cycle-to-Cycle Jitter	–	10	50	ps
IDYN1RC	Operating current	–	–	0.1	–	mA
SU1RC	Startup time	–	–	–	20	µs

Table 140 • **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Conditions/Package Combinations					Units	Notes
CCC Output Peak-to-Peak Period Jitter fOUT_CCC							
010, 050 FG484 Packages	SSO = 0	0 < SSO <= 2	SSO <= 4	SSO <= 8	SSO <= 16	–	*
20 MHz to 100 MHz	Max(110, ± 1% x (1/fOUT_CCC))	Max(150, ± 1% x (1/fOUT_CCC))				ps	–
100 MHz to 400 MHz	120	150			170	ps	–
025 FG484 Package	0 < SSO <=16						*
20 MHz to 74 MHz	± 1% x (1/fOUT_CCC)					ps	–
74 MHz to 400 MHz	210					ps	–
090 FG484 and 150 FC1152 Packages	0 < SSO <=16						*
20 MHz to 100 MHz	± 1% x (1/fOUT_CCC)					ps	–
100 MHz to 400 MHz	150					ps	–
*Note: *SSO Data is based on LVCMOS 2.5 V MSIO and/or MSIOD Bank I/Os.*							

16. JTAG

Table 141 • **JTAG 1532**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	-1 Speed Grade					Units
		010	025	050	090	150	
tTCK2Q	Clock to Q (data out)	7.91	7.95	8.15	9.21	8.85	ns
tRSTB2Q	Reset to Q (data out)	6.54	6.27	7.54	7.94	8.99	ns
tDISU	Test Data Input Setup Time	-0.70	-0.70	-0.31	-1.33	-1.02	ns
tDIHD	Test Data Input Hold Time	2.38	2.47	2.13	2.71	2.59	ns
tTMSSU	Test Mode Select Setup Time	-0.86	-1.13	0.26	-1.03	-0.56	ns
tTMDHD	Test Mode Select Hold Time	1.48	1.98	0.21	1.69	1.05	ns
tTRSTREM	ResetB Removal Time	-1.1	-1.38	-0.49	-0.8	-1.07	ns
tTRSTREC	ResetB Recovery Time	-1.1	-1.38	-0.47	-0.8	-1.07	ns
FTCKMAX	TCK Maximum frequency	25	25	25	25	25	MHz

19. Mathblock Timing Characteristics

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. Each IGLOO2 and SmartFusion2 SoC mathblock supports 18x18 signed multiplication, dot product, and built-in addition, subtraction, and accumulation units to combine multiplication results efficiently.

Table 145 • **Mathblocks With All Registers Used**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Mathblock With All Registers Used		Speed Grade –1		
Parameter	**Description**	**Min**	**Max**	**Units**
TMISU	Input, Control Register Setup time	0.149	–	ns
TMIHD	Input, Control Register Hold time	0.08	–	ns
TMOCDINSU	CDIN Input Setup time	1.68	–	ns
TMOCDINHD	CDIN Input Hold time	-0.419	–	ns
TMSRSTENSU	Synchronous Reset/Enable Setup time	0.185	–	ns
TMSRSTENHD	Synchronous Reset/Enable Hold time	0.011	–	ns
TMARSTREM	Asynchronous Reset Removal time	0	–	ns
TMARSTREC	Asynchronous Reset Recovery time	0.088	–	ns
TMOCQ	Output Register Clock to Out delay	–	0.232	ns
TMCLKMP	CLK Minimum period	2.245	–	ns

Table 146 • **Mathblock With Input Bypassed and Output Registers Used**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Mathblock With Input Bypassed and Output Registers Used		Speed Grade –1		
Parameter	**Description**	**Min**	**Max**	**Units**
TMOSU	Output Register Setup time	2.294	–	ns
TMOHD	Output Register Hold time	-0.444	–	ns
TMOCDINSU	CDIN Input Setup time	1.68	–	ns
TMOCDINHD	CDIN Input Hold time	-0.419	–	ns
TMSRSTENSU	Synchronous Reset/Enable Setup time	0.115	–	ns
TMSRSTENHD	Synchronous Reset/Enable Hold time	0.011	–	ns
TMARSTREM	Asynchronous Reset Removal time	0	–	ns
TMARSTREC	Asynchronous Reset Recovery time	0.014	–	ns
TMOCQ	Output Register Clock to Out delay	–	0.232	ns
TMCLKMP	CLK Minimum period	2.179	–	ns

23. PCIe Electrical and Timing AC and DC Characteristics

PCIe® is a high speed, packet-based, point-to-point, low pin count, serial interconnect bus. The IGLOO2 and SmartFusion2 SoC FPGAs has up to four hard high-speed serial interface blocks. Each SERDES block contains a PCIe system block. The PCIe system is connected to the SERDES block.

Table 152 • **Transmitter Parameters**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Min	Typ	Max	Units
VTX-DIFF-PP	Differential swing PCIe Gen1	0.8	–	1.2	V
VTX-CM-AC-P	Output common mode voltage PCIe Gen1	–	–	20	mV
VTX-RISE-FALL	Rise and fall time (20% to 80%) PCIe Gen1	0.125	–	–	UI
ZTX-DIFF-DC	Output impedance – differential	80	–	120	Ω
LTX-SKEW	Lane-to-lane TX skew within a SERDES block PCIe Gen1	–	–	500 ps + 2 UI	ps
RLTX-DIFF	Return loss differential mode PCIe Gen1	–10	–	–	dB
RLTX-CM	Return loss common mode PCIe Gen1	–6	–	–	dB
TX-LOCK-RST	Transmit PLL lock time from reset	–	–	10	µs

Table 153 • **Receiver Parameters**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Min	Typ	Max	Units
VRX-DIFF-PP-CC	Input levels PCIe Gen1	0.175	–	1.2	V
VRX-CM-DC-P	Input common mode range (DC coupled) Note: PCIe standard mandates AC coupling	NA	NA	NA	–
VRX-CM-AC-P	Input common mode range (AC coupled)	–	–	150	mV
VRX-DIFF-PP-CC	Differential input sensitivity Gen1	0.175	–	–	mV
ZRX-DIFF-DC	Differential input termination	80	100	120	Ω
REXT	External calibration resistor	1,188	1,200	1,212	Ω
CDR-LOCK-RST	CDR relock time from reset	–	–	15	µs
RLRX-DIFF	Return loss differential mode PCIe Gen1	–10	–	–	dB
RLRX-CM	Return loss common mode PCIe Gen1	–6	–	–	dB
	CID limit (set by 8B/10B coding, not the receiver PLL)	–	–	4	UI
VRX-IDLE-DET-DIFF-PP	Signal detect limit	65	–	175	mV

Table 154 • **SERDES Reference Clock AC Specifications**
Worst-Case Military Conditions: T_J = 125°C, Worst-Case VDD = 1.14V

Symbols	Description	Min	Typ	Max	Units
FREFCLK	Reference Clock Frequency	100	–	160	MHz
TRISE	Reference Clock Rise Time	0.6	–	4	V/ns
TFALL	Reference Clock Fall Time	0.6	–	4	V/ns
TCYC	Reference Clock Duty Cycle	40	–	60	%
Mmrefclk	Reference Clock Mismatch	-300	–	300	ppm
SSCref	Reference Spread Spectrum Clock	0	–	5000	ppm

Table 158 • **I2C Characteristics**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Definition	Conditions	Min	Typ	Max	Units	Notes
VHYS	Hysteresis of Schmitt triggered inputs for VDDI > 2 V	Refer to Table 20 on page 27 for more information.	0.05 x VDDI	–	–	V	–
IIL	Input current high	Refer to the "Single-Ended I/O Standards" section on page 27 for more information.	–	–	10	µA	–
IIH	Input current low	Refer to the "Single-Ended I/O Standards" section on page 27 for more information.	–	–	10	µA	–
Tir	Input rise time	Standard Mode	–	–	1000	ns	–
–	–	Fast Mode	–	–	300	ns	–
Tif	Input fall time	Standard Mode	–	–	300	ns	–
–	–	Fast Mode	–	–	300	ns	–
VOL	Maximum output voltage low (open drain) at 3 mA sink current for VDDI > 2 V	Refer to the "Single-Ended I/O Standards" section on page 27 for more information. I/O standard used for illustration: MSIO bank – LVTTL 8 mA low drive.	–	–	0.4	V	–
Cin	Pin capacitance	VIN = 0, f = 1.0 MHz	–	–	10	pF	–
t_{OF}	Output fall time from VIHMin to VILMax	VIHmin to VILMax, Cload = 400 pF	–	21.04	–	ns	1
		VIHmin to VILMax, Cload = 100 pF	–	5.556	–	ns	
t_{OR}	Output rise time from VILMax to VIHMin	VILMax to VIHmin, Cload = 400pF	–	19.887	–	ns	1
		VILMax to VIHmin, Cload = 100pF	–	5.218	–	ns	
Rpull-up	Output buffer maximum pull-down resistance	–	–	–	50	Ω	2, 3
Rpull-down	Output buffer maximum pull-up resistance	–	–	–	131.25	Ω	2, 4
Dmax	Maximum data rate	Fast mode	–	–	400	Kbps	–
		Standard mode	–	–	100	Kbps	–
t_{FILT}	Pulse width of spikes which must be suppressed by the input filter	Fast mode	–	50	–	ns	–

Notes:

1. *These values are provided for MSIO Bank - LVTTL 8 mA Low Drive at 25°C, typical conditions. For Board Design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models.*
2. *These maximum values are provided for information only. Minimum output buffer resistance values depend on VDDIx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models.*
3. *R(PULL-DOWN-MAX) = (VOLspec) / IOLspec*
4. *R(PULL-UP-MAX) = (VDDImax – VOHspec) / IOHspec*

Datasheet Information

List of Changes

The following table shows important changes made in this document for each revision.

Revision	Changes	Page
Revision 4 (September 2015)	Updated Table 9: "SmartFusion2 and IGLOO2 Quiescent Supply Current – Typical Process" for typical process values (SAR 69218).	17
	Updated Table 10: "SmartFusion2 and IGLOO2 Quiescent Supply Current – Worst-Case Process" for worst process values (SAR 69218).	18
	Updated Table 140: "IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications" for FG484 package (SAR 69804).	101
Revision 3 (June 2015)	Updated Table 1: "IGLOO2 FPGA and SmartFusion2 SoC FPGA Device Status" (SAR 68620).	10
Revision 2 (June 2015)	Updated Table 1: "IGLOO2 FPGA and SmartFusion2 SoC FPGA Device Status"	10
	Updated Table 3: "Recommended Operating Conditions"	12
	Updated Table 4: "FPGA Operating Limits" (SAR 63109).	14
	Updated Table 7: "Package Thermal Resistance"	15
	Updated Table 65: "DDR2/SSTL18 AC Specifications (Applicable to DDRIO Bank Only)" and Table 69: "DDR3/SSTL15 AC Specifications" (SAR 67210).	49, 51
	Added "Embedded NVM (eNVM) Characteristics" (SAR 52509).	97
	Updated Table 139: "IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification" (SAR 65958, SAR 62012, and SAR 56666).	100
	Updated Table 141: "JTAG 1532"	101
	Added "DEVRST_N Characteristics " (SAR 64100).	102
	Added "DDR Memory Interface Characteristics" (SAR 66223).	107
	Added "SFP Transceiver Characteristics" (SAR 63105).	108
	Added "CAN Controller Characteristics" (SAR 50424).	116
	Added "USB Characteristics" (SAR 50424).	117
	Updated Table 157: "Maximum Frequency for MSS Main Clock" and Table 163: "Maximum Frequency for HPMS Main Clock" (SAR 66314).	110, 118
Revision 1 (December 2014)	Initial release.	NA