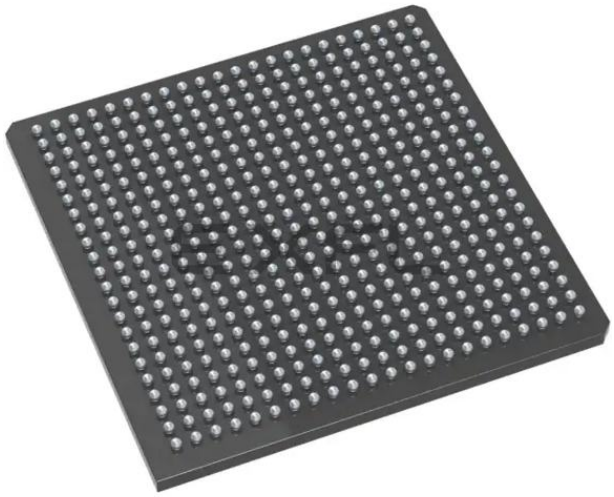

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What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 25K Logic Modules
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s025t-1fg484m

7. Timing Model

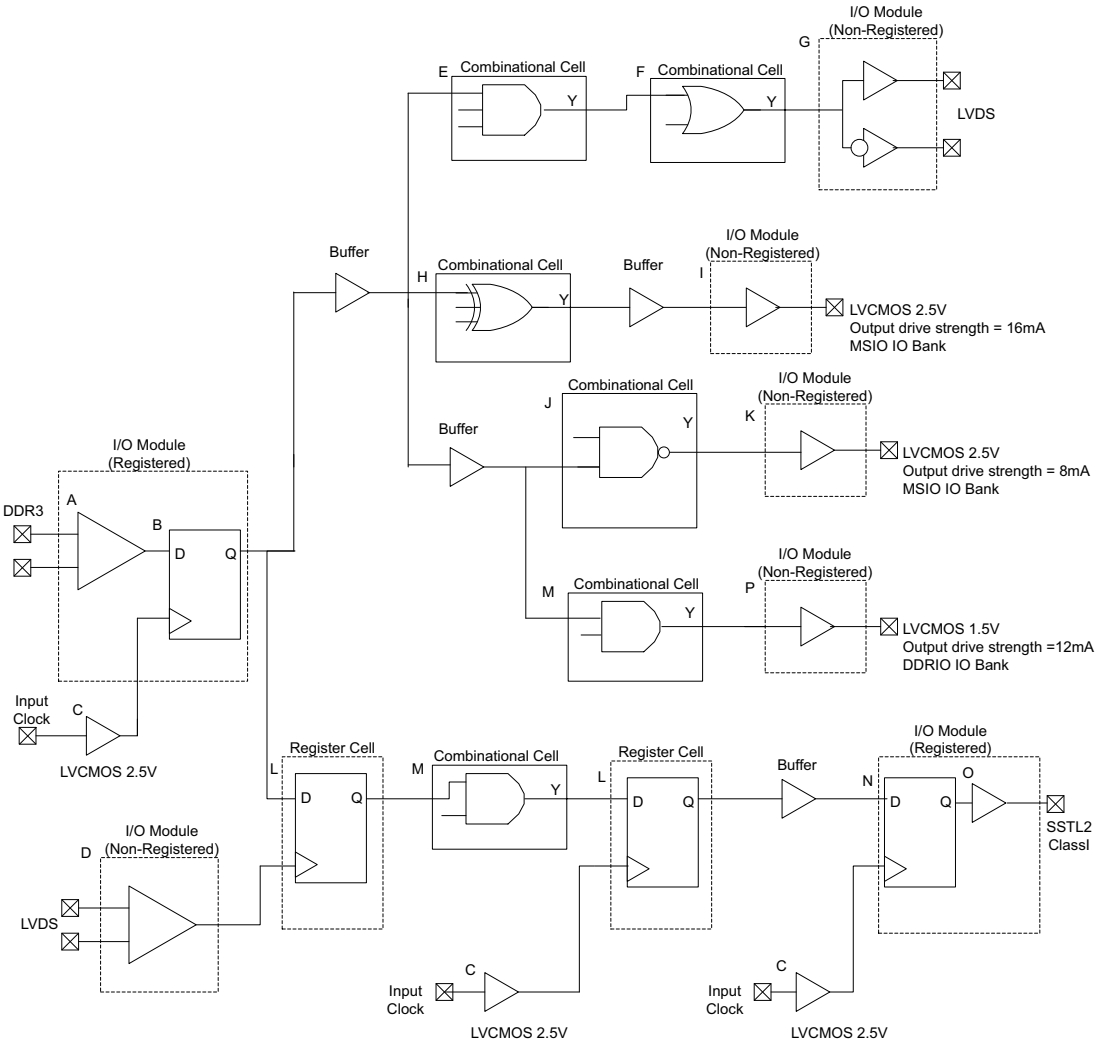

***Figure 1* • Timing Model**

8.4 I/O Speeds

Table 16 • **Maximum Data Rate Summary for Worst-Case Military Conditions**

Single-Ended I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
PCI 3.3 V	560	–	–	Mbps
LVTTL 3.3 V	540	–	–	Mbps
LVCMOS 3.3 V	540	–	–	Mbps
LVCMOS 2.5 V	360	370	360	Mbps
LVCMOS 1.8 V	260	360	360	Mbps
LVCMOS 1.5 V	140	190	210	Mbps
LVCMOS 1.2 V	100	140	180	Mbps
LPDDR – LVCMOS 1.8 V Mode	–	–	360	Mbps
Voltage-Referenced I/O	MSIO	MSIOD	DDRIO	Units
LPDDR	–	–	360	Mbps
HSTL1.5 V	–	–	360	Mbps
SSTL 2.5 V	450	480	360	Mbps
SSTL 1.8 V	–	–	600	Mbps
Voltage-Referenced I/O	MSIO	MSIOD	DDRIO	Units
SSTL 1.5 V	–	–	600	Mbps
Differential I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
LVPECL (input only)	810	–	–	Mbps
LVDS 3.3 V	480	480	–	Mbps
LVDS 2.5 V	480	480	–	Mbps
RSDS	460	480	–	Mbps
BLVDS	450	–	–	Mbps
MLVDS	450	–	–	Mbps
Mini-LVDS	460	480	–	Mbps

8.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

8.6.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 21 • **LVTTL/LVCMOS 3.3 V DC Voltage Specification (Applicable to MSIO I/O Bank Only)**

Symbol	Parameters	Conditions	Min	Typ	Max	Units	Notes
LVTTL/LVCMOS 3.3 V Recommended DC Operating Conditions							
VDDI	Supply voltage		3.15	3.3	3.45	V	–
LVTTL/LVCMOS 3.3 V DC Input Voltage Specification							
VIH (DC)	DC input logic High		2.0	–	3.45	V	–
VIL (DC)	DC input logic Low		–0.3	–	0.8	V	–
IIH (DC)	Input current High		–	–	10	µA	–
IIL (DC)	Input current Low		–	–	10	µA	–
LVCMOS 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		2.4	–	–	V	*
VOL	DC output logic Low		–	–	0.4	V	*
LVTTL 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		2.4	–	–	V	–
VOL	DC output logic Low		–	–	0.4	V	–
*Note: * The VOH/VOL test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.*							

Table 22 • **LVTTL/LVCMOS 3.3 V Maximum Switching Speeds (Applicable to MSIO I/O Bank Only)**

Symbol	Parameters	Conditions	Min	Typ	Max	Units
LVTTL/LVCMOS 3.3 V Maximum Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	540	Mbps

Table 23 • **LVTTL/LVCMOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO Bank Only)**

LVTTL/LVCMOS 3.3 V AC Test Parameter Specifications						
Symbol	**Parameters**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Vtrip	Measuring/trip point for data path		–	1.4	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

8.6.4 1.8 V LVCMOS

LVCMOS 1.8 is a general standard for 1.8 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-7A.

8.6.4.1 Minimum and Maximum AC/DC Input and Output Levels

Table 33 • **LVCMOS 1.8 V DC Voltage Specification**

Symbols	Parameters	Min	Typ	Max	Units
Recommended DC Operating Conditions					
VDDI	Supply Voltage	1.710	1.8	1.89	V
LVCMOS 1.8 V DC Input Voltage Specification					
VIH(DC)	DC input Logic HIGH (for MSIOD and DDRIO I/O Banks)	0.65 x VDDI	–	1.89	V
VIH(DC)	DC input Logic HIGH (for MSIO I/O Bank)	0.65 x VDDI	–	2.75	V
VIL(DC)	DC input Logic LOW	-0.3	–	0.35 × VDDI	V
IIH(DC)	Input Current HIGH	–	–	10	uA
IIL(DC)	Input Current LOW	–	–	10	uA
LVCMOS 1.8 V DC Output Voltage Specification					
VOH	DC output Logic HIGH	VDDI - 0.45	–	–	V
VOL	DC output Logic LOW	–	–	0.45	V

Table 34 • **LVCMOS 1.8 V Maximum AC Switching Speeds**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 1.8 V Maximum AC Switching Speed						
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	360	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	260	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	360	Mbps
*Note: * Maximum data rate applies for drive strength 8mA and above, all slews*						

Table 35 • **LVCMOS 1.8 V Transmitter Drive Strength Specifications**

Output Drive Selection		VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	Min	Max		
2 mA	2 mA	VDDI – 0.45	0.45	2	2
4 mA	4 mA	VDDI – 0.45	0.45	4	4
6 mA	6 mA	VDDI – 0.45	0.45	6	6
8 mA	8 mA	VDDI – 0.45	0.45	8	8
10 mA	10 mA	VDDI – 0.45	0.45	10	10
12 mA	N/A	VDDI – 0.45	0.45	12	12

Table 41 • **LVCMOS 1.5 V Maximum AC Switching Speeds**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 1.5 V Maximum AC Switching Speed						
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	210	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	140	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	190	Mbps

Table 42 • **LVCMOS 1.5 V AC Test Parameters and Driver Impedance Specifications**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 1.5 V AC Calibrated Impedance Option						
Rodt_cal	Supported output driver calibrated impedance (for DDRIO I/O Bank)		–	75, 60, 50, 40	–	Ω
LVCMOS 1.5 V AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	0.75	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

Table 43 • **LVCMOS 1.5 V Transmitter Drive Strength Specifications**

Output Drive Selection			VOH (V)	VOL (V)		
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (with Fixed Code)	Min	Max	IOH (at VOH) mA	IOL (at VOL) mA
2 mA	2 mA	2 mA	VDDI × 0.75	VDDI × 0.25	2	2
4 mA	4 mA	4 mA	VDDI × 0.75	VDDI × 0.25	4	4
6 mA	6 mA	6 mA	VDDI × 0.75	VDDI × 0.25	6	6
8 mA	N/A	8 mA	VDDI × 0.75	VDDI × 0.25	8	8
N/A	N/A	10 mA	VDDI × 0.75	VDDI × 0.25	10	10
N/A	N/A	12 mA	VDDI × 0.75	VDDI × 0.25	12	12

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 59 • **HSTL 15 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.425 V

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
HSTL Class I (for DDRIO I/O Bank)						
Single Ended	2.922	2.91	2.904	3.225	3.218	ns
Differential	2.907	2.757	2.755	2.662	2.66	ns
HSTL Class II (for DDRIO I/O Bank)						
Single Ended	2.817	2.735	2.735	2.644	2.644	ns
Differential	2.827	2.81	2.803	3.205	3.197	ns

8.7.2 Stub-Series Terminated Logic

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in IGLOO2 and SmartFusion2 SoC FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. IGLOO2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

8.7.3 Stub-Series Terminated Logic 2.5 V (SSTL2)

SSTL2 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs and also comply with reduced and full drive of double data rate (DDR) standards. IGLOO2 and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

8.7.3.1 Minimum and Maximum DC Input and Output Levels Specification

Table 60 • **DDR1/SSTL2 Minimum and Maximum DC Input and Output Levels**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
VDDI	Supply voltage		2.375	2.5	2.625	V
VTT	Termination voltage		1.164	1.250	1.339	V
VREF	Input reference voltage		1.164	1.250	1.339	V
SSTL2 DC Input Voltage Specification						
VIH (DC)	DC input logic High		VREF + 0.15	–	2.625	V
VIL (DC)	DC input logic Low		–0.3	–	VREF – 0.15	V
IIH (DC)	Input current High		–	–	10	µA
IIL (DC)	Input current Low		–	–	10	µA
SSTL2 DC Output Voltage Specification						
SSTL2 Class I (DDR Reduced Drive)						
VOH	DC output logic High		VTT + 0.608	–	–	V
VOL	DC output logic Low		–	–	VTT – 0.608	V
IOH at VOH	Output minimum source DC current		8.1	–	–	mA

Table 72 • **LPDDR AC/DC Specifications (for DDRIO IO Bank Only)**

LPDDR Reduced Drive						
VOH	DC output logic High	0.9 × VDDI	–	–	V	–
VOL	DC output logic Low	–	–	0.1 × VDDI	V	–
IOH at VOH	Output minimum source DC current	0.1	–	–	mA	–
IOL at VOL	Output minimum sink current	–0.1	–	–	mA	–
LPDDR Full Drive						*
VOH	DC output logic High	0.9 × VDDI	–	–	V	–
VOL	DC output logic Low	–	–	0.1 × VDDI	V	–
IOH at VOH	Output minimum source DC current	0.1	–	–	mA	–
IOL at VOL	Output minimum sink current	–0.1	–	–	mA	–
LPDDR DC Differential Voltage Specification						
VID (DC)	DC input differential voltage	0.4 × VDDI	–	–	V	–
*Note: *To meet JEDEC Electrical Compliance, use LPDDR Full Drive Transmitter.*						

Table 73 • **LPDDR Maximum AC Switching Speeds (for DDRIO I/O Bank Only)**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Dmax	Maximum data rate	AC loading: per JEDEC specifications	–	–	360	Mbps

Table 74 • **LPDDR AC Specifications (for DDRIO IO Bank Only)**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LPDDR AC Differential Voltage Specification						
VDIFF (AC)	AC Input differential voltage	–	0.6 × VDDI	–	–	V
Vx (AC)	AC Differential Cross Point Voltage	–	0.4 × VDDI	–	0.6 × VDDI	V
LPDDR Impedance Specifications						
Rref	Supported Output Driver Calibrated Impedance	Reference Resistor = 150 Ω	–	20,42	–	Ω
RTT	Effective impedance Value - ODT	Reference Resistor = 150 Ω	–	50, 75, 150	–	Ω
LPDDR AC Test Parameters Specifications						
Vtrip	Measuring/Trip Point for Data Path	–	–	0.9	–	V
Rent	Resistance for Enable Path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})	–	–	2k	–	Ω
Cent	Capacitive Loading for Enable Path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})	–	–	5	–	pF
Rtt_test	Reference resistance for Data Test Path for LPDDR ($t_{DP)}$	–	–	50	–	Ω
Cload	Capacitive Loading for Data Path (t_{DP})	–	–	5	–	pF

8.7.6.2 AC Switching Characteristics

Table 75 • LPDDR AC Switching Characteristics for Receiver (Input Buffers)
Worst-Case Military Conditions: T_J=125°C, VDD=1.14 V, VDDI= 1.71 V

		Speed Grade –1	
	ODT (On Die Termination)	t_{PY}	Units
LPDDR (for DDRIO I/O Bank with Fixed Codes)			
Pseudo-Differential	None	1.633	ns
True-Differential	None	1.65	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 76 • LPDDR AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Military Conditions: T_J=125°C, VDD=1.14 V, VDDI= 1.71 V

	Speed Grade –1					
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	Units
LPDDR Reduced Drive (for DDRIO I/O Bank)						
Single Ended	2.645	2.431	2.434	2.396	2.398	ns
Differential	2.652	3.044	3.038	2.46	2.455	ns
LPDDR Full Drive (for DDRIO I/O Bank)						
Single Ended	2.532	2.401	2.398	2.368	2.365	ns
Differential	2.546	2.509	2.503	2.852	2.845	ns

8.7.6.3 Minimum and Maximum AC/DC Input and Output Levels Specification using LPDDR-LVCMOS 1.8 V Mode

Table 77 • LPDDR-LVCMOS 1.8 V Mode, Minimum and Maximum DC Input and Output Levels (Applicable to DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LPDDR-LVCMOS 1.8 V Recommended DC Operating Conditions						
VDDI	Supply Voltage	–	1.710	1.8	1.89	V
LPDDR-LVCMOS 1.8 V Mode DC Input Voltage Specification						
VIH(DC)	DC input Logic HIGH for (MSIOD and DDRIO I/O Banks)	–	0.65 x VDDI	–	1.89	V
VIH(DC)	DC input Logic HIGH (for MSIO I/O Bank)	–	0.65 x VDDI	–	3.45	V
VIL(DC)	DC input Logic LOW	–	-0.3	–	0.35 x VDDI	V
IIH(DC)	Input current HIGH	–	–	–	10	uA
IIL(DC)	Input current LOW	–	–	–	10	uA
LPDDR-LVCMOS 1.8 V Mode DC Output Voltage Specification						
VOH	DC output Logic HIGH	–	VDDI - 0.45	–	–	V
VOL	DC output Logic LOW	–	–	–	0.45	V

Table 127 • **uSRAM (RAM128x9) in 128x9 Mode**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tclkmpwl	Read Clock Minimum pulse Width Low	1.8	–	ns
tplcy	Read Pipe-line clock period	4	–	ns
tplclkmpwh	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
tplclkmpwl	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.776	ns
taddrsu	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	1.959	–	ns
taddrhd	Read Address Hold Time in Synchronous Mode	0.125	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.704	–	ns
trdensu	Read Enable Setup Time	0.287	–	ns
trdenhd	Read Enable Hold Time	0.059	–	ns
tblksu	Read Block Select Setup Time	1.898	–	ns
tblkhd	Read Block Select Hold Time	-0.671	–	ns
tblk2q	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.14	ns
trstrem	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
trstrec	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
tr2q	Read Asynchronous Reset to Output Propagation Delay (with Pipe-Line Register Enabled)	–	0.865	ns
tsrstsu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.062	–	ns
tccy	Write Clock Period	4	–	ns
tcclkmpwh	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclkmpwl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblkcsu	Write Block Setup Time	0.417	–	ns
tblkchd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.104	–	ns
tdinchd	Write Input Data hold Time	0.142	–	ns
taddrcsu	Write Address Setup Time	0.091	–	ns

Table 127 • **uSRAM (RAM128x9) in 128x9 Mode**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
taddrchd	Write Address Hold Time	0.24	–	ns
twecsu	Write Enable Setup Time	0.41	–	ns
twechd	Write Enable Hold Time	-0.027	–	ns
fmax	Maximum Frequency	–	250	MHz

Table 128 • **uSRAM (RAM128x8) in 128x8 Mode**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tcy	Read Clock Period	4	–	ns
tclkmpwh	Read Clock Minimum Pulse Width High	1.8	–	ns
tclkmpwl	Read Clock Minimum pulse Width Low	1.8	–	ns
tplcy	Read Pipe-line clock period	4	–	ns
tplclkmpwh	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
tplclkmpwl	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.776	ns
taddrsu	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	1.959	–	ns
taddrhd	Read Address Hold Time in Synchronous Mode	0.125	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.704	–	ns
trdensu	Read Enable Setup Time	0.287	–	ns
trdenhd	Read Enable Hold Time	0.059	–	ns
tblksu	Read Block Select Setup Time	1.898	–	ns
tblkhd	Read Block Select Hold Time	-0.671	–	ns
tblk2q	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.14	ns
trstrem	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
trstrec	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns

Table 130 • **uSRAM (RAM512x2) in 512x2 Mode**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tclkmpwl	Read Clock Minimum pulse Width Low	1.8	–	ns
tplcy	Read Pipe-line clock period	4	–	ns
tplclkmpwh	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
tplclkmpwl	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.824	ns
taddrsu	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	2.023	–	ns
taddrhd	Read Address Hold Time in Synchronous Mode	0.141	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.599	–	ns
trdensu	Read Enable Setup Time	0.287	–	ns
trdenhd	Read Enable Hold Time	0.059	–	ns
tblksu	Read Block Select Setup Time	1.898	–	ns
tblkhd	Read Block Select Hold Time	-0.671	–	ns
tblk2q	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.219	ns
trstrem	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
trstrec	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
tr2q	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.862	ns
tsrstsu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.062	–	ns
tccy	Write Clock Period	4	–	ns
tcclkmpwh	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclkmpwl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblkcsu	Write Block Setup Time	0.417	–	ns
tblkchd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.104	–	ns
tdinchd	Write Input Data hold Time	0.142	–	ns
taddrcsu	Write Address Setup Time	0.091	–	ns

18. System Controller SPI Characteristics

Table 143 • **System Controller SPI Characteristics**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Symbol	Description	Conditions	All Devices/Speed Grades			Units	Notes
			Min	Typ	Max		
sp1	SC_SPI_SCK minimum period	–	20	–	–	ns	–
sp2	SC_SPI_SCK minimum pulse width high	–	10	–	–	ns	–
sp3	SC_SPI_SCK minimum pulse width low	–	10	–	–	ns	–
sp4	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS rise time (10%-90%) 1	I/O Configuration: LVTTL 3.3V- 20mA AC Loading: 35pF Test Conditions: Typical Voltage, 25C	–	1.239	–	ns	*
sp5	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS fall time (10%-90%) 1	I/O Configuration: LVTTL 3.3V- 20mA AC Loading: 35pF Test Conditions: Typical Voltage, 25C	–	1.245	–	ns	*
sp6	Data from master (SC_SPI_SDO) setup time	–	160	–	–	ns	–
sp7	Data from master (SC_SPI_SDO) hold time	–	160	–	–	ns	–
sp8	SC_SPI_SDI setup time	–	20	–	–	ns	–
sp9	SC_SPI_SDI hold time	–	20	–	–	ns	–

*Note: *For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models. Use the supported I/O Configurations for the System Controller SPI in Table 144.*

Table 144 • **Supported I/O Configurations for System Controller SPI (for MSIO Bank Only)**

Voltage Supply	I/O Drive Configuration	Units
3.3 V	20	mA
2.5 V	16	mA
1.8 V	12	mA
1.5 V	8	mA
1.2 V	4	mA

Table 147 • **Mathblock With Input Register Used and Output in Bypass Mode**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Mathblock With Input Register Used and Output in Bypass Mode		Speed Grade –1		
Parameter	**Description**	**Min**	**Max**	**Units**
TMISU	Input Register Setup time	0.149	–	ns
TMIHD	Input Register Hold time	0.08	–	ns
TMSRSTENSU	Synchronous Reset/Enable Setup time	0.185	–	ns
TMSRSTENHD	Synchronous Reset/Enable Hold time	-0.012	–	ns
TMARSTREM	Asynchronous Reset Removal time	-0.005	–	ns
TMARSTREC	Asynchronous Reset Recovery time	0.088	–	ns
TMICQ	Input Register Clock to Output delay	–	2.52	ns
TMCDIN2Q	CDIN to Output delay	–	1.951	ns

Table 148 • **Mathblock With Input and Output in Bypass Mode**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Mathblock With Input and Output in Bypass Mode		Speed Grade –1		
Parameter	**Description**	**Min**	**Max**	**Units**
TMIQ	Input to Output delay	–	2.568	ns
TMCDIN2Q	CDIN to Output delay	–	1.951	ns

20. Flash*Freeze Timing Characteristics

Table 149 • **Flash*Freeze Entry and Exit Times**
Military Worst-Case conditions: T_J = 125°C, VDD = 1.14 V

Symbols	Parameters	Conditions	Entry/Exit Timing	Units	Notes
TFF_ENTRY	Entry time	eNVM and MSS/HPMS PLL = ON	160	µs	1
		eNVM and MSS/HPMS PLL = OFF	215	µs	1

Table 159 • **I2C Switching Characteristics**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Definition	Conditions	Speed Grade –1		Units
			Min	Max	
t_{LOW}	Low period of I2C_x_SCL	–	1	–	pclk cycles
t_{HIGH}	High period of I2C_x_SCL	–	1	–	pclk cycles
$t_{HD;STA}$	START hold time	–	1	–	pclk cycles
$t_{SU;STA}$	START setup time	–	1	–	pclk cycles
$t_{HD;DAT}$	DATA hold time	–	1	–	pclk cycles
$t_{SU;DAT}$	DATA setup time	–	1	–	pclk cycles
$t_{SU;STO}$	STOP setup time	–	1	–	pclk cycles

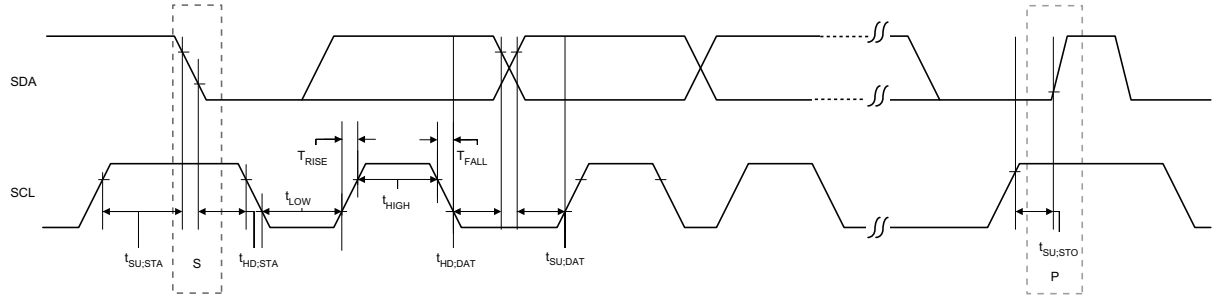

Figure 16 • **I^2C Timing Parameter Definition**

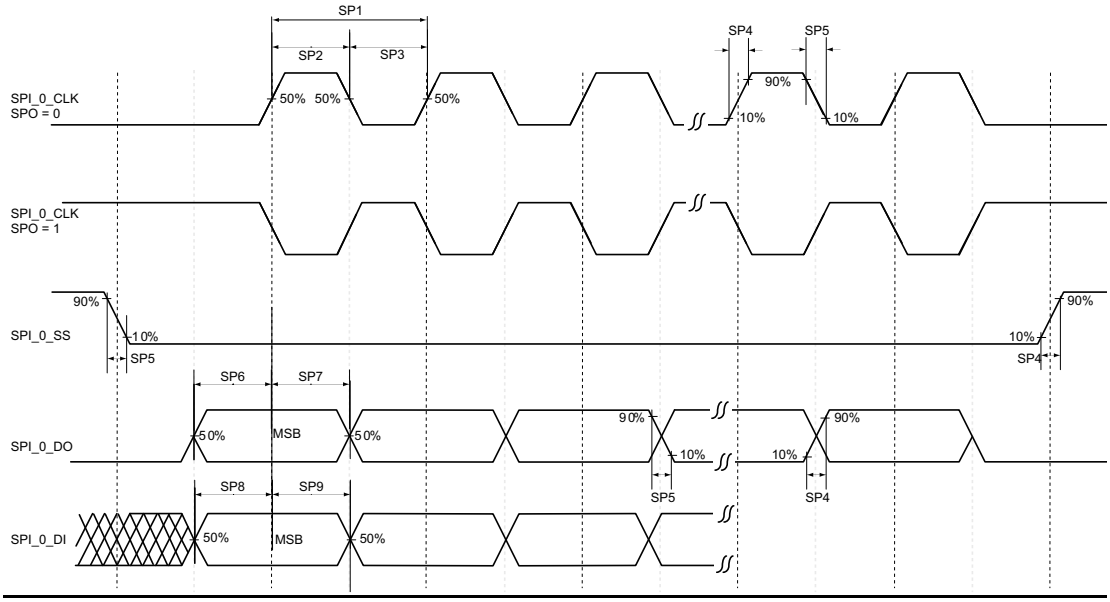

***Figure 17* • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**

25. CAN Controller Characteristics

Table 161 • **CAN Controller Characteristics**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Min	Typ	Max	Units	Notes
FCANREFCLK	Internally Sourced CAN Reference Clock Frequency	–	–	128	MHz	*
BAUDCAN	CAN Performance Baud Rate	0.05	–	1	Mbps	–
Note: PCLK to CAN controller must be a multiple of 8 MHz.						

27. IGLOO2 Specifications

27.1 HPMS Clock Frequency

Table 163 • **Maximum Frequency for HPMS Main Clock**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Symbol	Description	Speed Grade –1	Units
HPMS_CLK	Maximum Frequency for the HPMS Main Clock (FCLK)	133	MHz

27.2 IGLOO2 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_0_CLK. For timing parameter definitions, refer to Figure 18 on page 120.

Table 164 • **SPI Characteristics**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Symbol	Description	Conditions	All Devices/Speed Grades			Unit	Notes
			Min	Typ	Max		
sp1	**SPI_[0|1]_CLK minimum period**						
	SPI_[0|1]_CLK = PCLK/2	–	12	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/4	–	24.1	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/8	–	48.2	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/16	–	0.1	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/32	–	0.19	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/64	–	0.39	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/128	–	0.77	–	–	µs	–
sp2	**SPI_[0|1]_CLK minimum pulse width high**						
	SPI_[0|1]_CLK = PCLK/2	–	6	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/4	–	12.05	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/8	–	24.1	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/16	–	0.05	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/32	–	0.095	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/64	–	0.195	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/128	–	0.385	–	–	µs	–

Table 164 • **SPI Characteristics**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Symbol	Description	Conditions	All Devices/Speed Grades			Unit	Notes
			Min	Typ	Max		
sp3	**SPI_[0|1]_CLK minimum pulse width low**						
	SPI_[0|1]_CLK = PCLK/2	–	6	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/4	–	12.05	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/8	–	24.1	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/16	–	0.05	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/32	–	0.095	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/64	–	0.195	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/128	–	0.385	–	–	µs	–
sp4	SPI_[0|1]_CLK, SPI_[0|1]_DO, SPI_[0|1]_SS rise time (10%-90%)	I/O Configuration: LVCMOS 2.5 V-8mA AC Loading: 35pF Test Conditions: Typical Voltage, 25°C	–	2.77	–	ns	1
sp5	SPI_[0|1]_CLK, SPI_[0|1]_DO, SPI_[0|1]_SS fall time (10%-90%)	I/O Configuration: LVCMOS 2.5 V-8mA AC Loading: 35pF Test Conditions: Typical Voltage, 25°C	–	2.906	–	ns	1
SPI Master Configuration							
sp6m	SPI_[0|1]_DO setup time	–	(SPI_x_CLK_period/2) – 3.0	–	–	ns	2
sp7m	SPI_[0|1]_DO hold time	–	(SPI_x_CLK_period/2) – 2.5	–	–	ns	2
sp8m	SPI_[0|1]_DI setup time	–	8	–	–	ns	2
sp9m	SPI_[0|1]_DI hold time	–	2.5	–	–	ns	2
SPI Slave Configuration							
sp6s	SPI_[0|1]_DO setup time	–	(SPI_x_CLK_period/2) – 12.0	–	–	ns	2
sp7s	SPI_[0|1]_DO hold time	–	(SPI_x_CLK_period/2) + 3.0	–	–	ns	2
sp8s	SPI_[0|1]_DI setup time	–	2	–	–	ns	2

Table 164 • **SPI Characteristics**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Symbol	Description	Conditions	All Devices/Speed Grades			Unit	Notes
			Min	Typ	Max		
sp9s	SPI_[0|1]_DI hold time	–	3	–	–	ns	2

Notes:

1. *For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.*

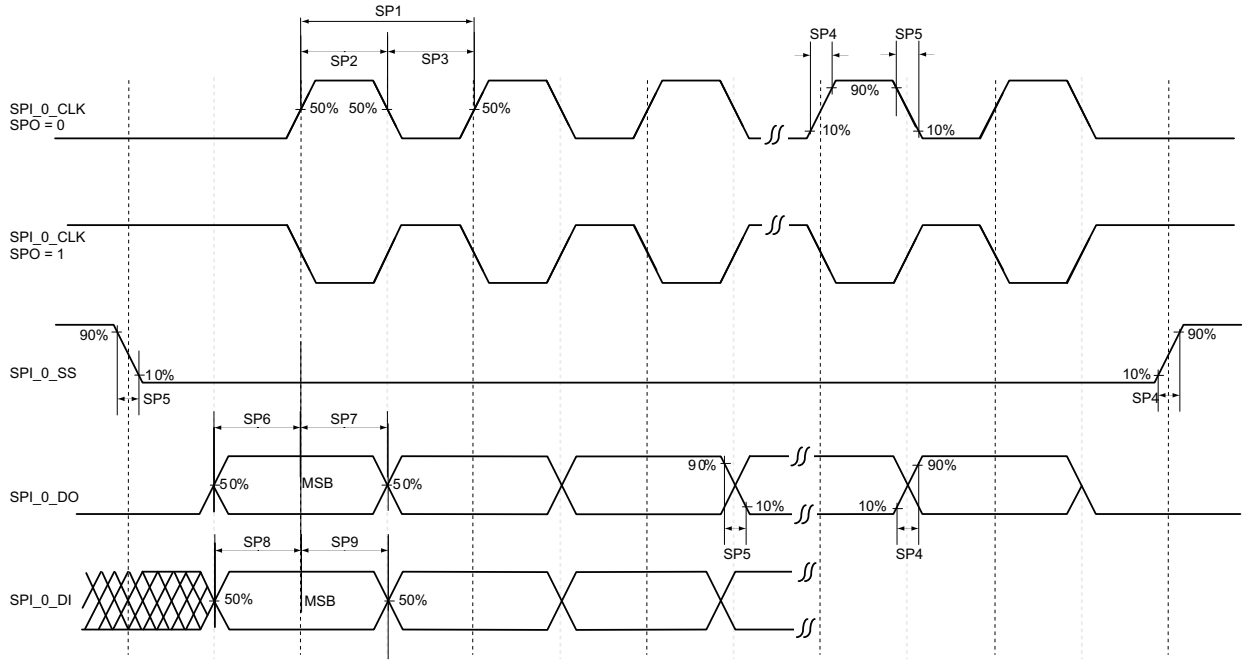

Figure 18 • **SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**