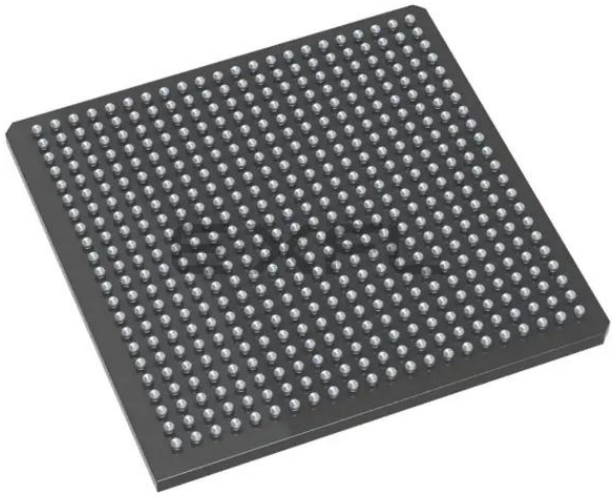

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## Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

## What are Embedded - System On Chip (SoC)?

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

| Details | |
|---|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | ARM® Cortex®-M3 |
| Flash Size | 256KB |
| RAM Size | 64KB |
| Peripherals | DDR, PCIe, SERDES |
| Connectivity | CANbus, Ethernet, I²C, SPI, UART/USART, USB |
| Speed | 166MHz |
| Primary Attributes | FPGA - 50K Logic Modules |
| Operating Temperature | -55°C ~ 125°C (TJ) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m2s050ts-1fgg484m |

***Table 2 •*** **Absolute Maximum Ratings (continued)**

| Symbol | Parameter | Limits | | Units | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $T_{STG}$ | Storage temperature | –65 | 150 | °C | * |
| $T_J$ | Junction temperature | – | 135 | °C | – |

*Note: * For flash programming and retention maximum limits, refer to Table 4 on page 14. For recommended operating conditions, refer to Table 3.*

***Table 3 •*** **Recommended Operating Conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Tj | Operating Junction Temperature | Military | -55 | 25 | 125 | °C | – |
| | Programming Junction Temperature | – | 0 | 25 | 85 | °C | – |
| | | – | -40 | 25 | 100 | °C | 1 |
| VDD | DC core supply voltage. Must always power this pin. | – | 1.14 | 1.2 | 1.26 | V | – |
| VPP | Power Supply for Charge Pumps (for Normal Operation and Programming) for 010, 025, 050 Devices | 2.5 V Range | 2.375 | 2.5 | 2.625 | V | – |
| | | 3.3 V Range | 3.15 | 3.3 | 3.45 | V | – |
| | Power Supply for Charge Pumps (for Normal Operation and Programming) for 090, and 150 devices | 3.3 V Range | 3.15 | 3.3 | 3.45 | V | – |
| MSS_MDDR_PLL_VDDA | Analog power pad for MDDR PLL | 2.5 V Range | 2.375 | 2.5 | 2.625 | V | – |
| | | 3.3 V Range | 3.15 | 3.3 | 3.45 | V | – |
| HPMS_MDDR_PLL_VDDA | Analog power pad for MDDR PLL | 2.5 V Range | 2.375 | 2.5 | 2.625 | V | – |
| | | 3.3 V Range | 3.15 | 3.3 | 3.45 | V | – |
| FDDR_PLL_VDDA | Analog power pad for FDDR PLL | 2.5 V Range | 2.375 | 2.5 | 2.625 | V | – |
| | | 3.3 V Range | 3.15 | 3.3 | 3.45 | V | – |
| PLL0_PLL1_MSS_MDDR_VDDA | Analog power pad for MDDR PLL | 2.5 V Range | 2.375 | 2.5 | 2.625 | V | – |
| | | 3.3 V Range | 3.15 | 3.3 | 3.45 | V | – |

***Table 3 •*** **Recommended Operating Conditions (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| VPPNVM | Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP | 2.5 V Range | 2.375 | 2.5 | 2.625 | V | – |
| | | 3.3 V Range | 3.15 | 3.3 | 3.45 | V | – |

*Notes:*

1. *Programming at this temperature range is available only with VPP in 3.3 V Range*
2. *Power supply ramps must all be strictly monotonic, without plateaus.*

***Table 4 •*** **FPGA Operating Limits**

| Product Grade | Element | Programming Temperature | Operating Temperature | Programming Cycles | Retention (Biased/Unbiased) | Note |
|---|---|---|---|---|---|---|
| Military | FPGA | Min $T_J$ = 0°C<br>Max $T_J$ = 85°C | Min $T_J$ = -55°C<br>Max $T_J$ = 125°C | 500 | 10 Years | – |
| | | Min $T_J$ = -40°C<br>Max $T_J$ = 100°C | Min $T_J$ = -55°C<br>Max $T_J$ = 125°C | 500 | 10 Years | * |

*Note: *: Programming at this temperature range is available only with VPP in 3.3 V Range*

***Table 5 •*** **Embedded Flash Limits**

| Product Grade | Element | Programming Temperature | Maximum Operating Temperature | Programming Cycles | Retention (Biased/Unbiased) |
|---|---|---|---|---|---|
| Military | Embedded flash | Min $T_J$ = -55°C<br>Max $T_J$ = 125°C | Min $T_J$ = -55°C<br>Max $T_J$ = 125°C | < 10,000 cycles per pages, up to one million cycles per eNVM array | 10 Years |

***Table 6 •*** **Device Storage Temperature and Retention**

| Product Grade | Storage Temperature (Tstg) | Retention |
|---|---|---|
| Military | Min $T_J$ = -55°C<br>Max $T_J$ = 125°C | 10 Years |

## 4.2 Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to -1.0 V for no longer than 10% or the period. The current during the transition must not exceed 100mA.

For AC signals, the input signal may overshoot during transitions to VCCI + 1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100mA.

Note: The above specification does not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant to the PCI standard including the PCI overshoot/undershoot specifications.

## 4.3. Thermal Characteristics

### 4.3.1 Introduction

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures.

EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

*EQ 1*

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

*EQ 2*

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

*EQ 3*

where

$\theta_{JA}$ = Junction-to-air thermal resistance
$\theta_{JB}$ = Junction-to-board thermal resistance
$\theta_{JC}$ = Junction-to-case thermal resistance
$T_J$ = Junction temperature
$T_A$ = Ambient temperature
$T_B$ = Board temperature (measured 1.0 mm away from the package edge)
$T_C$ = Case temperature
P = Total power dissipated by the device

***Table 7 •*** **Package Thermal Resistance**

| Product M2GL/M2S | $\theta_{JA}$ | | | $\theta_{JB}$ | $\theta_{JC}$ | Units |
|---|---|---|---|---|---|---|
| | Still Air | 1.0 m/s | 2.5 m/s | | | |
| **010** | | | | | | |
| FG484 | 18.22 | 14.83 | 13.62 | 8.83 | 4.92 | °C/W |
| **025** | | | | | | |
| FG484 | 17.03 | 13.66 | 12.45 | 7.66 | 4.18 | °C/W |
| **050** | | | | | | |
| FG484 | 15.29 | 12.19 | 10.99 | 6.27 | 3.24 | °C/W |
| **060** | | | | | | |
| FG484 | 15.40 | 12.06 | 10.85 | 6.14 | 3.15 | °C/W |
| **090** | | | | | | |
| FG484 | 14.64 | 11.37 | 10.16 | 5.43 | 2.77 | °C/W |
| **150** | | | | | | |
| FC1152 | 9.08 | 6.81 | 5.87 | 2.56 | 0.38 | °C/W |

***Table 10 •*** **SmartFusion2 and IGLOO2 Quiescent Supply Current – Worst-Case Process**

| Parameter | Modes | Conditions | 010 | 025 | 050 | 090 | 150 | Units |
|---|---|---|---|---|---|---|---|---|
| | | | VDD=1.26 V | VDD=1.26 V | VDD=1.26 V | VDD=1.26 V | VDD=1.26 V | |
| IDC1 | Non-Flash*Freeze | Military ($T_J$ = 125°C) | 151.5 | 227.4 | 358.9 | 443.1 | 660.4 | mA |
| IDC2 | Flash*Freeze | Military ($T_J$ = 125°C) | 127.2 | 144.2 | 174.6 | 195.0 | 236.3 | mA |

## 5.2 Programming Currents

The tables below represent programming, verify and Inrush currents for SmartFusion2 SoC and IGLOO2 FPGA devices.

***Table 11 •*** **Currents During Program Cycle, 0°C < = $T_J$ <= 85°C, Typical Process**

| Power Supplies | Voltage (V) | 010 | 025 | 050 | 090 | 150 | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| VDD | 1.26 | 53 | 55 | 58 | 42 | 52 | mA | – |
| VPP | 3.46 | 11 | 6 | 10 | 12 | 12 | mA | – |
| VPPNVM | 3.46 | 2 | 2 | 3 | 3 | – | mA | * |
| VDDI | 2.62 | 16 | 17 | 1 | 12 | 81 | mA | ** |
| | 3.46 | 31 | 36 | 1 | 17 | 84 | mA | ** |
| Number of banks | | 8 | 8 | 10 | 9 | 19 | – | – |

*Notes:*

** VPP and VPPNVM are internally shorted.*

*** The current for 050 represents JTAG I/O Bank only.*

***Table 12 •*** **Currents During Verify Cycle, 0°C <= $T_J$ <= 85°C, Typical Process**

| Power Supplies | Voltage (V) | 010 | 025 | 050 | 090 | 150 | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| VDD | 1.26 | 53 | 55 | 58 | 41 | 51 | mA | – |
| VPP | 3.46 | 5 | 3 | 15 | 11 | 12 | mA | – |
| VPPNVM | 3.46 | 0 | 0 | 1 | 1 | – | mA | * |
| VDDI | 2.62 | 16 | 17 | 1 | 11 | 81 | mA | ** |
| | 3.46 | 32 | 36 | 1 | 17 | 84 | mA | ** |
| Number of banks | | 8 | 8 | 10 | 9 | 19 | – | – |

*Notes:*

** VPP and VPPNVM are internally shorted.*

*** The current for 050 represents JTAG I/O Bank only.*

***Table 13 •*** **Inrush Currents at Power up, –55°C <= $T_J$ <=125°C, Typical Process**

| Power Supplies | Voltage (V) | 010 | 025 | 050 | 090 | 150 | Units |
|---|---|---|---|---|---|---|---|
| VDD | 1.26 | 53 | 78 | 57 | 98 | 140 | mA |
| VPP | 3.46 | 57 | 50 | 180 | 36 | 51 | mA |

## 8.3. Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The methodology of characterization is illustrated by the enable path test point shown in Figure 4.

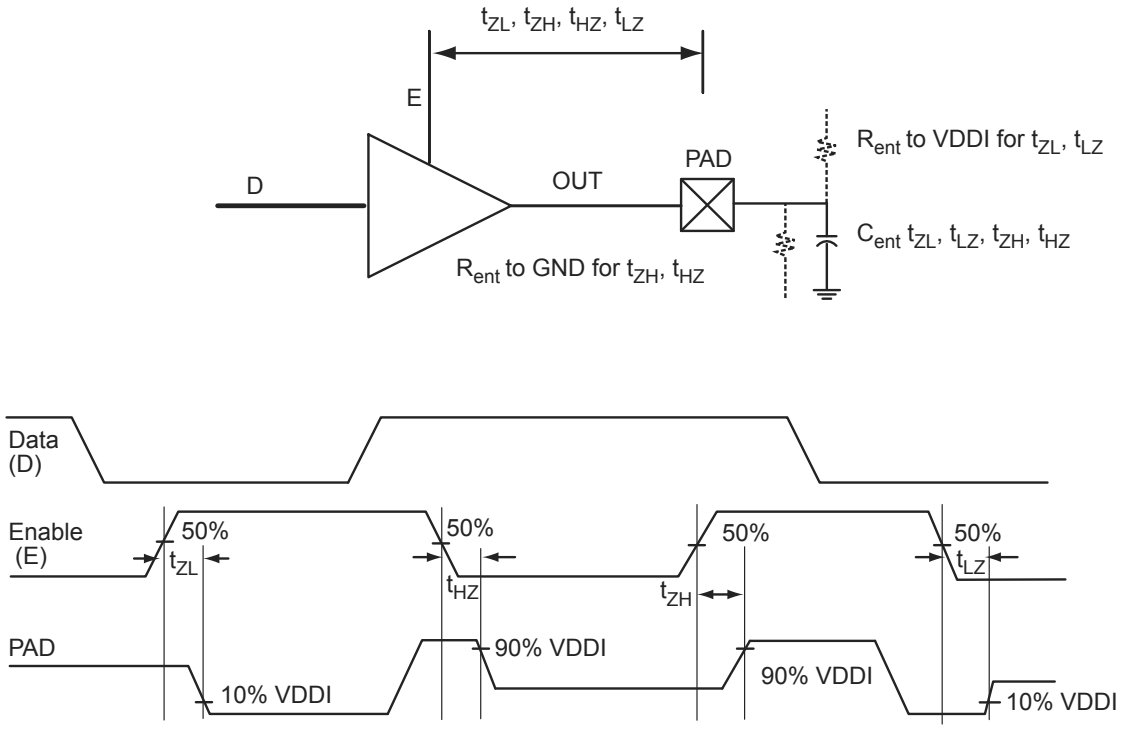


***Figure 4* • Tristate Buffer for Enable Path Test Point**

***Table 24 •*** **LVTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications (Applicable to MSIO Bank* Only)**

| Output Drive Selection | VOH (V) | VOL (V) | IOH (at VOH) mA | IOL (at VOL) mA |
|---|---|---|---|---|
| 2 mA | 2.4 | 0.4 | 2 | 2 |
| 4 mA | 2.4 | 0.4 | 4 | 4 |
| 8 mA | 2.4 | 0.4 | 8 | 8 |
| 12 mA | 2.4 | 0.4 | 12 | 12 |
| 16 mA | 2.4 | 0.4 | 16 | 16 |
| 20 mA | 2.4 | 0.4 | 18 | 18 |
| *Note: * Software Configurator GUI displays the Commercial/Industrial numeric values. The actual drive capability at temperature is defined in Table 24.* | | | | |

### *8.6.2.2 AC Switching Characteristics*

Worst-case Military conditions: $T_J$ = 125°C, VDD = 1.14 V, VDDI = 3.15 V

***AC Switching Characteristics for Receiver (Input Buffers)***

***Table 25 •*** **LVTTL/LVCMOS 3.3 V Receiver Characteristics for MSIO I/O Banks (Input Buffers)**
**Worst-case Military conditions: $T_J$ = 125°C, VDD = 1.14 V, VDDI = 3.15 V**

| | On-Die Termination (ODT) | Speed Grade –1 | | Units |
|---|---|---|---|---|
| | | $t_{PY}$ | $t_{PYS}$ | |
| **LVTTL/LVCMOS 3.3 V (for MSIO I/O Bank)** | None | 2.416 | 2.443 | ns |

***AC Switching Characteristics for Transmitter (Output and Tristate Buffers)***

***Table 26 •*** **LVTTL/LVCMOS 3.3 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)**
**Worst-case Military conditions: $T_J$ = 125°C, VDD = 1.14 V, VDDI = 3.15 V**

| Output Drive Selection | Slew Control | Speed Grade –1 | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | $t_{DP}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ | |
| 2mA | slow | 3.515 | 3.826 | 3.242 | 2.024 | 3.636 | ns |
| 4mA | slow | 2.565 | 2.948 | 2.774 | 3.339 | 4.896 | ns |
| 8mA | slow | 2.349 | 2.568 | 2.528 | 5.013 | 5.329 | ns |
| 12mA | slow | 2.261 | 2.324 | 2.386 | 6.389 | 6.05 | ns |
| 16mA | slow | 2.274 | 2.287 | 2.369 | 6.671 | 6.256 | ns |
| 20mA | slow | 2.372 | 2.206 | 2.306 | 6.976 | 6.541 | ns |

### 8.6.3 2.5 V LVCMOS

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in IGLOO2 FPGA and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-5A.

#### 8.6.3.1 Minimum and Maximum AC/DC Input and Output Levels Specification

**Table 27 • LVCMOS 2.5 V DC Voltage Specification**

| Symbol | Parameters | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| **LVCMOS 2.5 V Recommended DC Operating Conditions** | | | | | | | |
| VDDI | Supply voltage | | 2.375 | 2.5 | 2.625 | V | – |
| **LVCMOS 2.5 V DC Input Voltage Specification** | | | | | | | |
| VIH (DC) | DC input logic High (for MSIOD and DDRIO I/O Bank) | | 1.7 | – | 2.625 | V | – |
| VIH (DC) | DC input logic High (for MSIO I/O Bank) | | 1.7 | – | 2.75 | V | – |
| VIL (DC) | DC input logic Low | | –0.3 | – | 0.7 | V | – |
| IIH (DC) | Input current High | | – | – | 10 | µA | – |
| IIL (DC) | Input current Low | | – | – | 10 | µA | – |
| **LVCMOS 2.5 V DC Output Voltage Specification** | | | | | | | |
| VOH | DC output logic High | | 1.7 | – | – | V | * |
| VOL | DC output logic Low | | – | – | 0.7 | V | * |
| *Note: * The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.* | | | | | | | |

**Table 28 • LVCMOS 2.5 V Maximum AC Switching Speeds**

| Symbol | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Dmax | Maximum data rate (for DDRIO I/O Bank) | AC loading: 17 pF load, maximum drive/slew | – | – | 360 | Mbps |
| Dmax | Maximum data rate (for MSIO I/O Bank) | AC loading: 17 pF load, maximum drive/slew | – | – | 360 | Mbps |
| Dmax | Maximum data rate (for MSIOD I/O Bank) | AC loading: 17 pF load, maximum drive/slew | – | – | 370 | Mbps |

**Table 29 • LVCMOS 2.5 V AC Test Parameters and Driver Impedance Specifications**

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **LVCMOS 2.5 V Calibrated Impedance Option** | | | | | | |
| Rodt_cal | Supported output driver calibrated impedance (for DDRIO I/O Bank) | – | – | 75, 60, 50, 33, 25, 20 | – | Ω |
| **LVCMOS 2.5 V AC Test Parameters Specifications** | | | | | | |
| Vtrip | Measuring/trip point for data path | – | – | 1.2 | – | V |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | – | – | 2k | – | Ω |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | – | – | 5 | – | pF |
| Cload | Capacitive loading for data path ($t_{DP}$) | – | – | 5 | – | pF |

#### 8.7.4.2. AC Switching Characteristics

***AC Switching Characteristics for Receiver (Input Buffers)***

***Table 66 •*** **DDR2/SSTL18 AC Switching Characteristics for Receiver (Input Buffers)**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V, VDDI = 1.71 V**

| | On-Die Termination (ODT) | Speed Grade –1 | Units |
|---|---|---|---|
| | | $t_{PY}$ | |
| **SSTL18 (for DDRIO I/O Bank with Fixed Codes)** | | | |
| Pseudo differential | None | 1.633 | ns |
| True differential | None | 1.65 | ns |

***AC Switching Characteristics for Transmitter (Output and Tristate Buffers)***

***Table 67 •*** **DDR2/SSTL18 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V, VDDI = 1.71 V**

| | Speed Grade –1 | | | | | Units |
|---|---|---|---|---|---|---|
| | $t_{DP}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ | |
| **SSTL18 Class I (for DDRIO I/O Bank)** | | | | | | |
| Single Ended | 2.67 | 3.078 | 3.072 | 2.489 | 2.484 | ns |
| Differential | 2.645 | 2.431 | 2.434 | 2.396 | 2.398 | ns |
| **SSTL18 Class II (for DDRIO I/O Bank** | | | | | | |
| Single Ended | 2.564 | 2.973 | 2.965 | 2.45 | 2.444 | ns |
| Differential | 2.532 | 2.401 | 2.398 | 2.368 | 2.365 | ns |

## 8.7.5 Stub-Series Terminated Logic 1.5 V (SSTL15)

SSTL15 Class I and Class II are supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR3) standard. IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

### 8.7.5.1 Minimum and Maximum AC/DC Input and Output Levels Specification

***Table 68 •*** **DDR3 SSTL15 DC Voltage Specification (for DDRIO I/O Bank Only)**

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Recommended DC Operating Conditions** | | | | | | |
| VDDI | Supply voltage | | 1.425 | 1.5 | 1.575 | V |
| VTT | Termination voltage | | 0.698 | 0.750 | 0.803 | V |
| VREF | Input reference voltage | | 0.698 | 0.750 | 0.803 | V |
| **SSTL15 DC Input Voltage Specification** | | | | | | |
| VIH(DC) | DC input logic High | | VREF + 0.1 | – | 1.575 | V |
| VIL(DC) | DC input logic Low | | –0.3 | – | VREF – 0.1 | V |
| IIH (DC) | Input current High | | – | – | 10 | µA |
| IIL (DC) | Input current Low | | – | – | 10 | µA |

***Table 68 •*** **DDR3 SSTL15 DC Voltage Specification (for DDRIO I/O Bank Only) (continued)**

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **SSTL15 DC Output Voltage Specification** | | | | | | |
| **DDR3/SSTL15 Class I (DDR3 Reduced Drive)** | | | | | | |
| VOH | DC output logic High | | 0.8 x VDDI | – | – | V |
| VOL | DC output logic Low | | – | – | 0.2 x VDDI | V |
| IOH at VOH | Output minimum source DC current | | 6.5 | – | – | mA |
| IOL at VOL | Output minimum sink current | | –6.5 | – | – | mA |
| **SSTL15 Class II (DDR3 Full Drive)** | | | | | | |
| VOH | DC output logic High | | 0.8 × VDDI | – | – | V |
| VOL | DC output logic Low | | – | – | 0.2 x VDDI | V |
| IOH at VOH | Output minimum source DC current | | 7.6 | – | – | mA |
| IOL at VOL | Output minimum sink current | | –7.6 | – | – | mA |
| **SSTL15 Differential Voltage Specification** | | | | | | |
| VID | DC input differential voltage | | 0.2 | – | – | V |
| *Note: *To meet JEDEC Electrical Compliance, use DDR3 Full Drive Transmitter.* | | | | | | |

***Table 69 •*** **DDR3/SSTL15 AC Specifications**

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **SSTL15 AC Differential Voltage Specification** | | | | | | |
| VDIFF | AC input differential voltage | | 0.3 | – | – | V |
| Vx | AC differential cross point voltage | | 0.5 × VDDI – 0.150 | – | 0.5 × VDDI + 0.150 | V |
| **SSTL15 Maximum AC Switching Speed (for DDRIO I/O Banks Only)** | | | | | | |
| Dmax | Maximum data rate | AC loading: per JEDEC specifications | – | – | 600 | Mbps |
| **SSTL15 AC Calibrated Impedance Option** | | | | | | |
| Rref | Supported output driver calibrated impedance | Reference resistor = 240 Ω | – | 34, 40 | – | Ω |
| RTT | Effective impedance value (ODT) | Reference resistor = 240 Ω | – | 20, 30, 40, 60, 120 | – | Ω |
| **SSTL15 AC Test Parameters Specifications** | | | | | | |
| Vtrip | Measuring/trip point for data path | | – | 0.75 | – | V |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 2k | – | Ω |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 5 | – | pF |
| Rtt_test | Reference resistance for data test path for SSTL15 Class I ($t_{DP}$) | | – | 50 | – | Ω |
| Rtt_test | Reference resistance for data test path for SSTL15 Class II ($t_{DP}$) | | – | 25 | – | Ω |
| Cload | Capacitive loading for data path ($t_{DP}$) | | – | 5 | – | pF |

### 8.8.2 B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

#### 8.8.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification

***Table 89 •*** **B-LVDS DC Voltage Specification**

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Bus-LVDS Recommended DC Operating Conditions** | | | | | | |
| VDDI | Supply voltage | | 2.375 | 2.5 | 2.625 | V |
| **Bus-LVDS DC Input Voltage Specification** | | | | | | |
| VI | DC input voltage | | 0 | – | 2.925 | V |
| IIH (DC) | Input current High | | – | – | 10 | µA |
| IIL (DC) | Input current Low | | – | – | 10 | µA |
| **Bus-LVDS DC Output Voltage Specification (for MSIO I/O Bank only)** | | | | | | |
| VOH | DC output logic High | | 1.25 | 1.425 | 1.6 | V |
| VOL | DC output logic Low | | 0.9 | 1.075 | 1.25 | V |
| **Bus-LVDS Differential Voltage Specification** | | | | | | |
| VOD | Differential output voltage swing (for MSIO I/O Bank only) | | 65 | – | 460 | mV |
| VOCM | Output common mode voltage (for MSIO I/O Bank only) | | 1.1 | – | 1.5 | V |
| VICM | Input common mode voltage | | 0.05 | – | 2.4 | V |
| VID | Input differential voltage | | 0.1 | – | VDDI | V |

***Table 90 •*** **B-LVDS AC Specifications**

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Bus-LVDS Maximum AC Switching Speed** | | | | | | |
| Dmax | Maximum data rate (for MSIO I/O Bank) | AC loading: 2 pF / 100 Ω differential load | – | – | 450 | Mbps |
| **Bus-LVDS Impedance Specifications** | | | | | | |
| Rt | Termination resistance | | – | 27 | – | Ω |
| **Bus-LVDS AC Test Parameters Specifications** | | | | | | |
| Vtrip | Measuring/trip point for data path | | – | Cross point | – | V |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 2k | – | Ω |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 5 | – | pF |

### 8.8.4 Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

#### 8.8.4.1 Mini-LVDS Minimum and Maximum Input and Output Levels

***Table 97 •*** **Mini-LVDS DC Voltage Specification**

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Recommended DC Operating Conditions** | | | | | | |
| VDDI | Supply voltage | | 2.375 | 2.5 | 2.625 | V |
| **Mini-LVDS DC Input Voltage Specification** | | | | | | |
| VI | DC Input voltage | | 0 | – | 2.925 | V |
| **Mini-LVDS DC Output Voltage Specification** | | | | | | |
| VOH | DC output logic High | | 1.25 | 1.425 | 1.6 | V |
| VOL | DC output logic Low | | 0.9 | 1.075 | 1.25 | V |
| **Mini-LVDS Differential Voltage Specification** | | | | | | |
| VOD | Differential output voltage swing | | 300 | – | 600 | mV |
| VOCM | Output common mode voltage | | 1 | – | 1.4 | V |
| VICM | Input common mode voltage | | 0.3 | – | 1.2 | V |
| VID | Input differential voltage | | 100 | – | 600 | mV |

***Table 98 •*** **Mini-LVDS AC Specifications**

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Mini-LVDS Maximum AC Switching Speed** | | | | | | |
| Dmax | Maximum data rate (MSIO I/O Bank) | AC loading: 2 pF / 100 Ω differential load | – | – | 460 | Mbps |
| Dmax | Maximum data rate (MSIOD I/O Bank) | AC loading: 10 pF / 100 Ω differential load | – | – | 480 | Mbps |
| **Mini-LVDS Impedance Specification** | | | | | | |
| Rt | Termination resistance | | – | 100 | – | Ω |
| **Mini-LVDS AC Test Parameters Specifications** | | | | | | |
| VTrip | Measuring/trip point for data path | | – | Cross point | – | V |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 2k | – | Ω |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 5 | – | pF |

### 8.8.4.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

**Table 99 • Mini-LVDS AC Switching Characteristics for Receiver (Input Buffers)**
**Worst-case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V, VDDI= 2.375 V**

| | On-Die Termination (ODT) | Speed Grade –1 | Units |
|---|---|---|---|
| | | $t_{PY}$ | |
| **Mini-LVDS (for MSIO I/O Bank)** | None | 3.112 | ns |
| | 100 | 2.995 | ns |
| **Mini-LVDS (for MSIOD I/O Bank)** | None | 2.612 | ns |
| | 100 | 2.612 | ns |

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 100 • Mini-LVDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
**Worst-case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V, VDDI= 2.375 V**

| | Speed Grade –1 | | | | | Units |
|---|---|---|---|---|---|---|
| | $t_{DP}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ | |
| **Mini-LVDS (for MSIO I/O Bank)** | 2.3 | 2.602 | 2.59 | 2.306 | 2.32 | ns |
| **Mini-LVDS (for MSIOD I/O Bank)** | | | | | | |
| No pre-emphasis | 1.652 | 1.84 | 1.833 | 1.988 | 1.965 | ns |
| Min pre-emphasis | 1.652 | 1.84 | 1.833 | 1.988 | 1.965 | ns |
| Med pre-emphasis | 1.577 | 1.868 | 1.86 | 2.02 | 1.994 | ns |
| Max pre-emphasis | 1.555 | 1.894 | 1.883 | 2.048 | 2.019 | ns |

### 8.8.5 RSDS

Reduced Swing Differential Signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS devices and is only intended for point-to-point applications.

#### 8.8.5.1 Minimum and Maximum Input and Output Levels

***Table 101 •*** **RSDS DC Voltage Specification**

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Recommended DC Operating Conditions** | | | | | | |
| VDDI | Supply voltage | | 2.375 | 2.5 | 2.625 | V |
| **RSDS DC Input Voltage Specification** | | | | | | |
| VI | DC input voltage | | 0 | – | 2.925 | V |
| **RSDS DC Output Voltage Specification** | | | | | | |
| VOH | DC output logic High | | 1.25 | 1.425 | 1.6 | V |
| VOL | DC output logic Low | | 0.9 | 1.075 | 1.25 | V |
| **RSDS Differential Voltage Specification** | | | | | | |
| VOD | Differential output voltage swing | | 100 | – | 600 | mV |
| VOCM | Output common mode voltage | | 0.5 | – | 1.5 | V |
| VICM | Input common mode voltage | | 0.3 | – | 1.5 | V |
| VID | Input differential voltage | | 100 | – | 600 | mV |

***Table 102 •*** **RSDS AC Specifications**

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **RSDS Maximum AC Switching Speed** | | | | | | |
| Dmax | Maximum data rate (for MSIO I/O Bank) | AC loading: 2 pF / 100 Ω differential load | – | – | 460 | Mbps |
| Dmax | Maximum data rate (for MSIOD I/O Bank) | AC loading: 10 pF / 100 Ω differential load | – | – | 480 | Mbps |
| **RSDS Impedance Specification** | | | | | | |
| Rt | Termination resistance | | – | 100 | – | Ω |
| **RSDS AC Test Parameters Specifications** | | | | | | |
| VTrip | Measuring/trip point for data path | | – | Cross point | – | V |
| Rent | Resistance for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 2k | – | Ω |
| Cent | Capacitive loading for enable path ($t_{ZH}$, $t_{ZL}$, $t_{HZ}$, $t_{LZ}$) | | – | 5 | – | pF |

### 8.10.3 Timing Characteristics

**Table 110 • Input DDR Propagation Delays**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD=1.14 V**

| Parameter | Description | Measuring Nodes (from, to) | Speed Grade –1 | Units |
|---|---|---|---|---|
| tDDRICLKQ1 | Clock-to-Out Out_QR for Input DDR | B,C | 0.165 | ns |
| tDDRICLKQ2 | Clock-to-Out Out_QF for Input DDR | B,D | 0.172 | ns |
| tDDRISUD | Data Setup for Input DDR | A,B | 0.372 | ns |
| tDDRIHD | Data Hold for Input DDR | A,B | 0 | ns |
| tDDRISUE | Enable Setup for Input DDR | E,B | 0.475 | ns |
| tDDRIHE | Enable Hold for Input DDR | E,B | 0 | ns |
| tDDRISUSLn | Synchronous Load Setup for Input DDR | G,B | 0.475 | ns |
| tDDRIHSLn | Synchronous Load Hold for Input DDR | G,B | 0 | ns |
| tDDRIAL2Q1 | Asynchronous Load-to-Out QR for Input DDR | F,C | 0.606 | ns |
| tDDRIAL2Q2 | Asynchronous Load-to-Out QF for Input DDR | F,D | 0.558 | ns |
| tDDRIREMAL | Asynchronous Load Removal time for Input DDR | F,B | 0 | ns |
| tDDRIRECAL | Asynchronous Load Recovery time for Input DDR | F,B | 0.076 | ns |
| tDDRIWAL | Asynchronous Load Minimum Pulse Width for Input DDR | F,F | 0.313 | ns |
| tDDRICKMPWH | Clock Minimum Pulse Width High for Input DDR | B,B | 0.078 | ns |
| tDDRICKMPWL | Clock Minimum Pulse Width Low for Input DDR | B,B | 0.164 | ns |

# 9. Logic Element Specifications

## 9.1 4-input LUT (LUT-4)

The IGLOO2 and SmartFusion2 SoC FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *SmartFusion2 and IGLOO2 Macro Library Guide*.

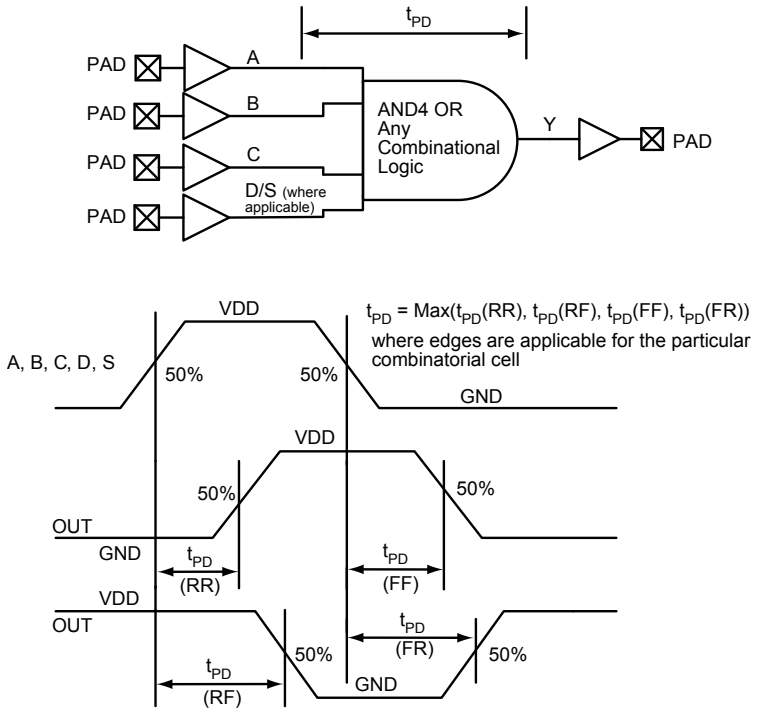


***Figure 13 •*** **LUT-4**

Timing Characteristics

***Table 112 •*** **Combinatorial Cell Propagation Delays**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V**

| Combinatorial Cell | Equation | Parameter | Speed Grade –1 | Units |
|---|---|---|---|---|
| INV | Y = !A | $t_{PD}$ | 0.106 | ns |
| AND2 | Y = A · B | $t_{PD}$ | 0.17 | ns |
| NAND2 | Y = !(A · B) | $t_{PD}$ | 0.157 | ns |
| OR2 | Y = A + B | $t_{PD}$ | 0.17 | ns |
| NOR2 | Y = !(A + B) | $t_{PD}$ | 0.157 | ns |
| XOR2 | Y = A ⊕ B | $t_{PD}$ | 0.17 | ns |
| XOR3 | Y = A ⊕ B ⊕ C | $t_{PD}$ | 0.236 | ns |
| AND3 | Y = A · B · C | $t_{PD}$ | 0.217 | ns |
| AND4 | Y = A · B · C · D | $t_{PD}$ | 0.384 | ns |

***Table 130 •*** **uSRAM (RAM512x2) in 512x2 Mode**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V (continued)**

| Parameter | Description | Speed Grade –1 | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| tclkmpwl | Read Clock Minimum pulse Width Low | 1.8 | – | ns |
| tplcy | Read Pipe-line clock period | 4 | – | ns |
| tplclkmpwh | Read Pipe-line clock Minimum Pulse Width High | 1.8 | – | ns |
| tplclkmpwl | Read Pipe-line clock Minimum Pulse Width Low | 1.8 | – | ns |
| tclk2q | Read Access Time with Pipeline Register | – | 0.276 | ns |
| | Read Access Time without Pipeline Register | – | 1.824 | ns |
| taddrsu | Read Address Setup Time in Synchronous Mode | 0.311 | – | ns |
| | Read Address Setup Time in Asynchronous Mode | 2.023 | – | ns |
| taddrhd | Read Address Hold Time in Synchronous Mode | 0.141 | – | ns |
| | Read Address Hold Time in Asynchronous Mode | -0.599 | – | ns |
| trdensu | Read Enable Setup Time | 0.287 | – | ns |
| trdenhd | Read Enable Hold Time | 0.059 | – | ns |
| tblksu | Read Block Select Setup Time | 1.898 | – | ns |
| tblkhd | Read Block Select Hold Time | -0.671 | – | ns |
| tblk2q | Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | – | 2.219 | ns |
| trstrem | Read Asynchronous Reset Removal Time (Pipelined Clock) | -0.15 | – | ns |
| | Read Asynchronous Reset Removal Time (Non-Pipelined Clock) | 0.047 | – | ns |
| trstrec | Read Asynchronous Reset Recovery Time (Pipelined Clock) | 0.524 | – | ns |
| | Read Asynchronous Reset Recovery Time (Non-Pipelined Clock) | 0.244 | – | ns |
| tr2q | Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled) | – | 0.862 | ns |
| tsrstsu | Read Synchronous Reset Setup Time | 0.279 | – | ns |
| tsrsthd | Read Synchronous Reset Hold Time | 0.062 | – | ns |
| tccy | Write Clock Period | 4 | – | ns |
| tcclkmpwh | Write Clock Minimum Pulse Width High | 1.8 | – | ns |
| tcclkmpwl | Write Clock Minimum Pulse Width Low | 1.8 | – | ns |
| tblkcsu | Write Block Setup Time | 0.417 | – | ns |
| tblkchd | Write Block Hold Time | 0.007 | – | ns |
| tdincsu | Write Input Data setup Time | 0.104 | – | ns |
| tdinchd | Write Input Data hold Time | 0.142 | – | ns |
| taddrcsu | Write Address Setup Time | 0.091 | – | ns |

**Table 130 • uSRAM (RAM512x2) in 512x2 Mode**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V (continued)**

| Parameter | Description | Speed Grade –1 | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| taddrchd | Write Address Hold Time | 0.255 | – | ns |
| twecsu | Write Enable Setup Time | 0.41 | – | ns |
| twechd | Write Enable Hold Time | -0.027 | – | ns |
| fmax | Maximum Frequency | – | 250 | MHz |

**Table 131 • uSRAM (RAM1024x1) in 1024x1 Mode**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V**

| Parameter | Description | Speed Grade –1 | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| tcy | Read Clock Period | 4 | – | ns |
| tclkmpwh | Read Clock Minimum Pulse Width High | 1.8 | | ns |
| tclkmpwl | Read Clock Minimum pulse Width Low | 1.8 | – | ns |
| tplcy | Read Pipe-line clock period | 4 | – | ns |
| tplclkmpwh | Read Pipe-line clock Minimum Pulse Width High | 1.8 | – | ns |
| tplclkmpwl | Read Pipe-line clock Minimum Pulse Width Low | 1.8 | – | ns |
| tclk2q | Read Access Time with Pipeline Register | – | 0.274 | ns |
| | Read Access Time without Pipeline Register | – | 1.839 | ns |
| taddrsu | Read Address Setup Time in Synchronous Mode | 0.311 | – | ns |
| | Read Address Setup Time in Asynchronous Mode | 2.041 | – | ns |
| taddrhd | Read Address Hold Time in Synchronous Mode | 0.141 | – | ns |
| | Read Address Hold Time in Asynchronous Mode | -0.623 | – | ns |
| trdensu | Read Enable Setup Time | 0.287 | – | ns |
| trdenhd | Read Enable Hold Time | 0.059 | – | ns |
| tblksu | Read Block Select Setup Time | 1.898 | – | ns |
| tblkhd | Read Block Select Hold Time | -0.671 | – | ns |
| tblk2q | Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | – | 2.236 | ns |
| trstrem | Read Asynchronous Reset Removal Time (Pipelined Clock) | -0.15 | – | ns |
| | Read Asynchronous Reset Removal Time (Non-Pipelined Clock) | 0.047 | – | ns |
| trstrec | Read Asynchronous Reset Recovery Time (Pipelined Clock) | 0.524 | – | ns |
| | Read Asynchronous Reset Recovery Time (Non-Pipelined Clock) | 0.244 | – | ns |

# 15. Clock Conditioning Circuits (CCC)

***Table 139 •*** **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification**
**Military Worst-Case Conditions: $T_J$ = 125°C, VDD = 1.14 V**

| Parameter | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Clock conditioning circuitry input frequency $f_{IN\_CCC}$ | All CCC | 1 | – | 200 | MHz | – |
| | 32 kHz Capable CCC | 0.032 | | 200 | MHz | – |
| Clock conditioning circuitry output frequency $f_{OUT\_CCC}$ | – | 0.078 | – | 400 | MHz | 1 |
| PLL VCO frequency | – | 500 | – | 1000 | MHz | 2 |
| Delay increments in programmable delay blocks | – | – | 75 | 100 | ps | – |
| Number of programmable values in each programmable delay block | – | – | – | 64 | – | – |
| Acquisition time | – | – | 70 | 100 | µs | – |
| Input Duty Cycle (Reference Clock) | Internal Feedback | | | | | |
| | 1 MHz ≤ $f_{IN\_CCC}$ ≤ 25 MHz | 10 | – | 90 | % | – |
| | 25 MHz ≤ $f_{IN\_CCC}$ ≤ 100 MHz | 25 | – | 75 | % | – |
| | 100 MHz ≤ $f_{IN\_CCC}$ ≤ 150 MHz | 35 | – | 65 | % | – |
| | 150 MHz ≤ $f_{IN\_CCC}$ ≤ 200 MHz | 45 | – | 55 | % | – |
| | External Feedback (CCC, FPGA, Off-chip) | | | | | |
| | 1 MHz ≤ $f_{IN\_CCC}$ ≤ 25 MHz | 25 | – | 75 | % | – |
| | 25 MHz ≤ $f_{IN\_CCC}$ ≤ 35 MHz | 35 | – | 65 | % | – |
| | 35 MHz ≤ $f_{IN\_CCC}$ ≤ 50 MHz | 45 | – | 55 | % | – |
| Output duty cycle | 010, 025, and 050 Devices | 46 | – | 52 | % | – |
| | 090 and 150 Devices | 44 | – | 52 | % | – |
| **Spread Spectrum Characteristics** | | | | | | |
| Modulation frequency range | – | 25 | 35 | 50 | kHz | – |
| Modulation depth range | – | 0 | – | 1.5 | % | – |
| Modulation depth control | – | – | 0.5 | – | % | – |

*Notes:*

1. *The minimum output clock frequency is limited by the PLL. For more information refer to the UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide.*
2. *The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance will be limited by the CCC output frequency.*

# 21. DDR Memory Interface Characteristics

***Table 150 •*** **DDR Memory Interface Characteristics**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V**

| Standard | Supported Data Rate | | | Unit |
|---|---|---|---|---|
| | Min | Typ | Max | |
| DDR3 | | 667 | | Mbps |
| DDR2 | | 667 | | Mbps |
| LPDDR | 50 | – | 400 | Mbps |

***Table 158 •*** **I2C Characteristics**
**Worst-Case Military Conditions: $T_J$ = 125°C, VDD = 1.14 V (continued)**

| Parameter | Definition | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| VHYS | Hysteresis of Schmitt triggered inputs for VDDI > 2 V | Refer to Table 20 on page 27 for more information. | 0.05 x VDDI | – | – | V | – |
| IIL | Input current high | Refer to the "Single-Ended I/O Standards" section on page 27 for more information. | – | – | 10 | µA | – |
| IIH | Input current low | Refer to the "Single-Ended I/O Standards" section on page 27 for more information. | – | – | 10 | µA | – |
| Tir | Input rise time | Standard Mode | – | – | 1000 | ns | – |
| – | – | Fast Mode | – | – | 300 | ns | – |
| Tif | Input fall time | Standard Mode | – | – | 300 | ns | – |
| – | – | Fast Mode | – | – | 300 | ns | – |
| VOL | Maximum output voltage low (open drain) at 3 mA sink current for VDDI > 2 V | Refer to the "Single-Ended I/O Standards" section on page 27 for more information. I/O standard used for illustration: MSIO bank – LVTTL 8 mA low drive. | – | – | 0.4 | V | – |
| Cin | Pin capacitance | VIN = 0, f = 1.0 MHz | – | – | 10 | pF | – |
| $t_{OF}$ | Output fall time from VIHMin to VILMax | VIHmin to VILMax, Cload = 400 pF | – | 21.04 | – | ns | 1 |
| | | VIHmin to VILMax, Cload = 100 pF | – | 5.556 | – | ns | |
| $t_{OR}$ | Output rise time from VILMax to VIHMin | VILMax to VIHmin, Cload = 400pF | – | 19.887 | – | ns | 1 |
| | | VILMax to VIHmin, Cload = 100pF | – | 5.218 | – | ns | |
| Rpull-up | Output buffer maximum pull-down resistance | – | – | – | 50 | Ω | 2, 3 |
| Rpull-down | Output buffer maximum pull-up resistance | – | – | – | 131.25 | Ω | 2, 4 |
| Dmax | Maximum data rate | Fast mode | – | – | 400 | Kbps | – |
| | | Standard mode | – | – | 100 | Kbps | – |
| $t_{FILT}$ | Pulse width of spikes which must be suppressed by the input filter | Fast mode | – | 50 | – | ns | – |

*Notes:*

1. *These values are provided for MSIO Bank - LVTTL 8 mA Low Drive at 25°C, typical conditions. For Board Design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models.*
2. *These maximum values are provided for information only. Minimum output buffer resistance values depend on VDDIx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models.*
3. *R(PULL-DOWN-MAX) = (VOLspec) / IOLspec*
4. *R(PULL-UP-MAX) = (VDDImax – VOHspec) / IOHspec*