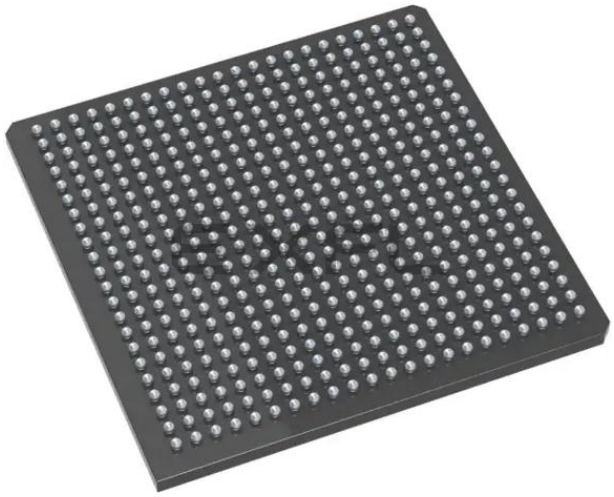

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Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 90K Logic Modules
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s090ts-1fg484m

List of Figures

Table 3 • **Recommended Operating Conditions (continued)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
PLL0_PLL1_HPMS_MDDR_VDDA	Analog power pad for MDDR PLL	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
CCC_XX[01]_PLL_VDDA	Analog power pad for PLL0-5	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
SERDES_[01]_PLL_VDDA	High supply voltage for PLL SERDES[01]	2.5 V Range	2.375	2.5	2.625	V	2
		3.3 V Range	3.15	3.3	3.45	V	2
SERDES_[01]_L[0123]_VDDAPLL	Analog power for SERDES[01] PLL lanes 0-3. It is a +2.5 V SERDES internal PLL supply.	–	2.375	2.5	2.625	V	–
SERDES_[01]_L[0123]_VDDAIO	TX/RX analog I/O voltage. Low voltage power for the lanes of SERDESIF0. It is a +1.2 V SERDES PMA supply.	–	1.14	1.2	1.26	V	–
SERDES_[01]_VDD	PCIe/PCS Power supply	–	1.14	1.2	1.26	V	–
VDDIx	1.2 V DC supply voltage	–	1.14	1.2	1.26	V	–
	1.5 V DC supply voltage	–	1.425	1.5	1.575	V	–
	1.8 V DC supply voltage	–	1.71	1.8	1.89	V	–
	2.5 V DC supply voltage	–	2.375	2.5	2.625	V	–
	3.3 V DC supply voltage	–	3.15	3.3	3.45	V	–
	LVDS differential I/O	–	2.375	2.5	3.45	V	–
	BLVDS, MLVDS, Mini-LVDS, RSDS differential I/O	–	2.375	2.5	2.625	V	–
	LVPECL differential I/O	–	3.15	3.3	3.45	V	–
VREFx	Reference Voltage Supply for FDDR (Bank0) and MDDR(Bank5)	–	0.49 × VDDIx	0.5 × VDDIx	0.51 × VDDIx	V	–

Table 13 • **Inrush Currents at Power up, –55°C <= T_J <=125°C, Typical Process**

VDDI	2.62	141	161	187	283	404	mA
Number of banks		8	8	10	9	19	–

6. Average Fabric Temperature and Voltage Derating Factors

Table 14 • **Average Temperature and Voltage Derating Factors for Fabric Timing Delays**
(Normalized to T_J = 125°C, Worst-Case VDD = 1.14 V)

Core Voltage VDD (V)	Junction Temperature (°C)							
	–55°C	–40°C	0°C	25°C	70°C	85°C	100°C	125°C
1.14	0.91	0.91	0.93	0.94	0.96	0.97	0.98	1.00
1.2	0.82	0.83	0.84	0.85	0.87	0.87	0.88	0.90
1.26	0.75	0.75	0.77	0.77	0.79	0.80	0.81	0.75

7. Timing Model

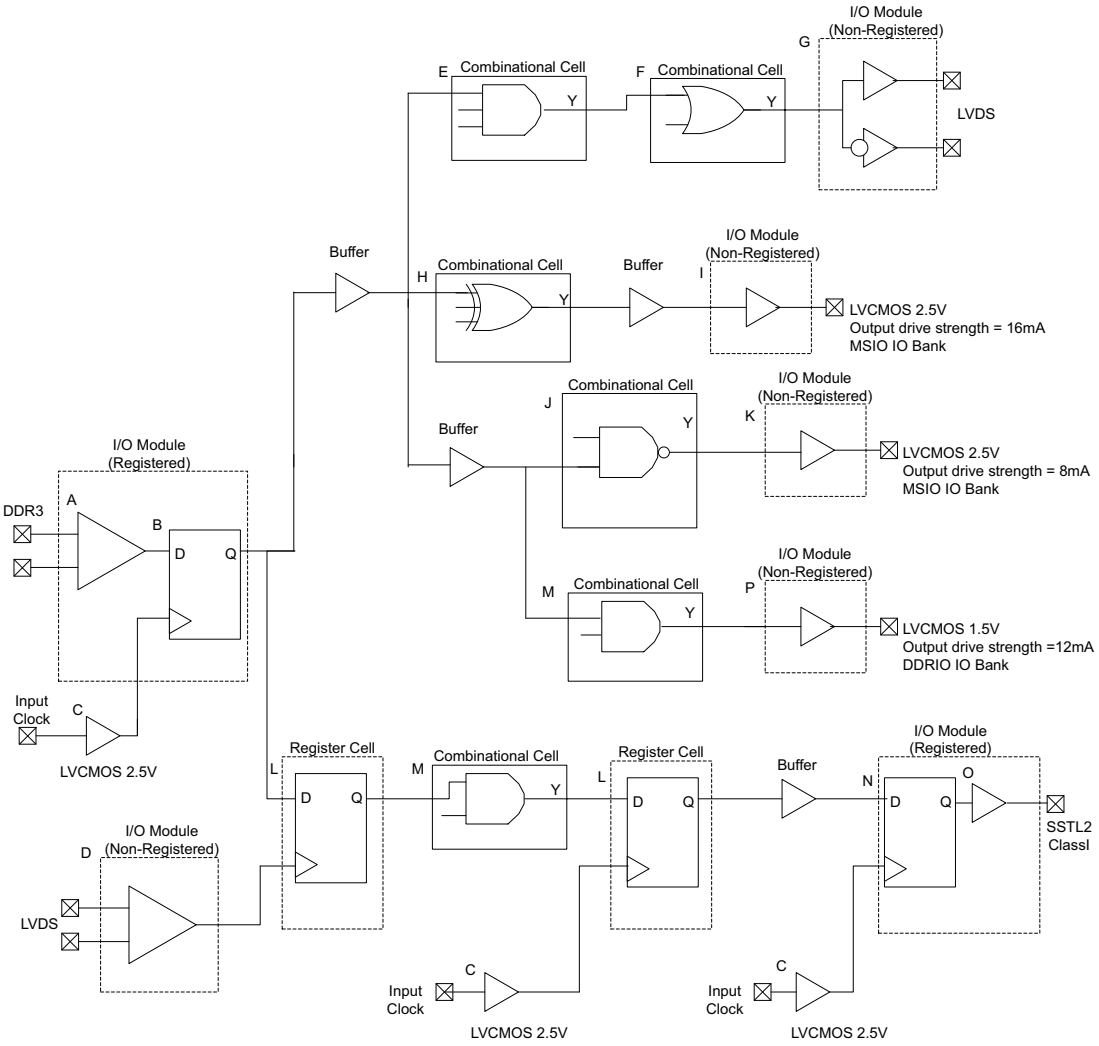

***Figure 1* • Timing Model**

Table 15 • **Timing Model Parameters (continued)**

Index	Parameter	Description	Speed Grade –1	Units	Notes
O	t_{DP}	Propagation Delay of SSTL2, Class I Transmitter on the MSIO Bank	2.283	ns	Refer to page 47 for more information
P	t_{DP}	Propagation Delay of LVCMOS 1.5 V Transmitter, Drive strength of 12mA, fast slew on the DDRIO Bank	3.703	ns	Refer to page 38 for more information

8. User I/O Characteristics

There are three types of I/Os supported in the IGLOO2 FPGA and SmartFusion2 SoC FPGA families: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the “I/Os” section of the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

8.1 Input Buffer and AC Loading

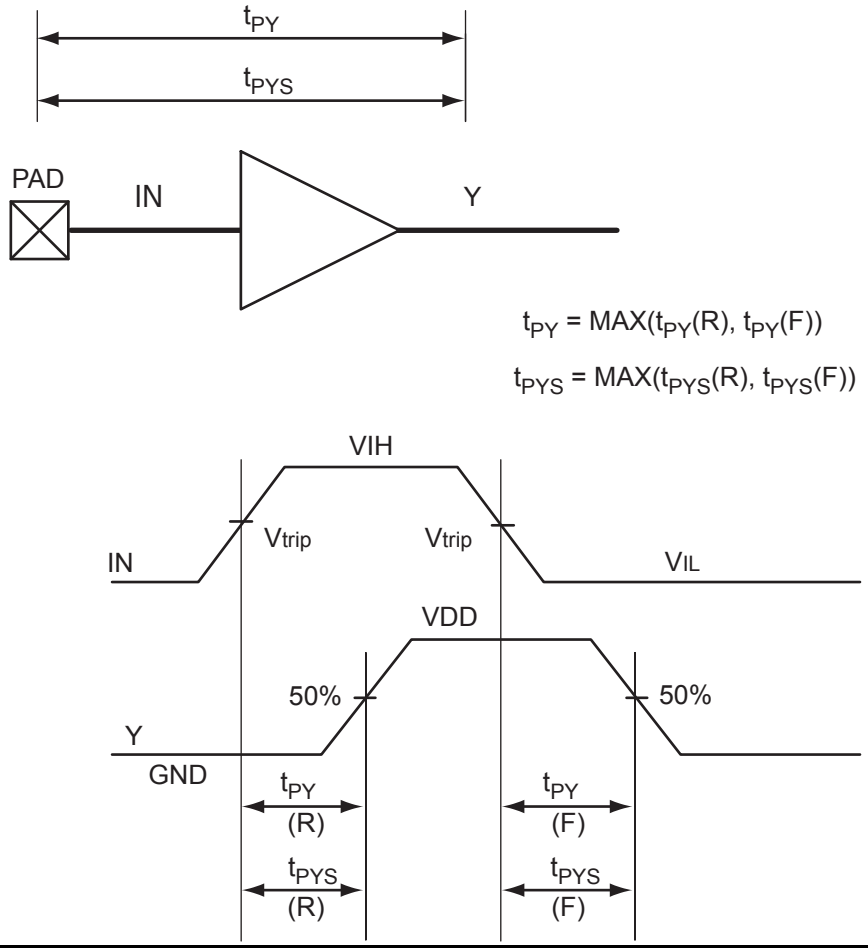

Figure 2 • **Input Buffer AC Loading**

Table 32 • LVCMOS 2.5 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-case Military conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 2.375 V (continued)

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
6 mA	slow	3.189	2.716	3.169	5.56	5.092	ns
	medium	2.886	2.473	2.876	5.273	4.752	ns
	medium_fast	2.749	2.355	2.738	5.127	4.167	ns
	fast	2.731	2.345	2.72	5.115	4.6	ns
8 mA	slow	3.132	2.646	3.109	5.686	5.207	ns
	medium	2.832	2.407	2.82	5.402	4.864	ns
	medium_fast	2.698	2.292	2.685	5.262	4.732	ns
	fast	2.684	2.282	2.671	5.252	4.724	ns
12 mA	slow	3.013	2.504	2.984	5.918	5.416	ns
	medium	2.72	2.284	2.707	5.657	5.074	ns
	medium_fast	2.592	2.176	2.578	5.537	4.949	ns
	fast	2.58	2.166	2.566	5.529	4.946	ns
16 mA	slow	2.936	2.415	2.902	6.136	5.577	ns
	medium	2.66	2.206	2.645	5.901	5.261	ns
	medium_fast	2.536	2.102	2.519	5.815	5.142	ns
	fast	2.523	2.093	2.506	5.81	5.137	ns
LVCMOS 2.5 V (for MSIO I/O Bank)							
2 mA	slow	3.933	4.352	4.22	2.358	3.838	ns
4 mA	slow	2.905	3.423	3.508	4.681	5.262	ns
6 mA	slow	2.687	2.995	3.155	5.561	5.73	ns
8 mA	slow	2.594	2.877	3.07	6.602	6.248	ns
12 mA	slow	2.623	2.732	2.944	6.974	6.478	ns
16 mA	slow	2.717	2.617	2.84	7.455	6.824	ns
LVCMOS 2.5 V (for MSIOD I/O Bank)							
2 mA	slow	2.403	2.922	2.89	5.397	5.202	ns
4 mA	slow	1.998	2.446	2.468	5.936	5.665	ns
6 mA	slow	1.861	2.329	2.375	6.391	6.068	ns
8 mA	slow	1.781	2.145	2.208	6.884	6.44	ns
12 mA	slow	1.804	2.039	2.108	7.23	6.685	ns

8.6.5.2. AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 44 • LVCMOS 1.5 V AC Switching Characteristics for Receiver (Input Buffers)
Worst-Case Military Conditions: T_J=125°C, VDD=1.14 V, VDDI= 1.425 V

	ODT (On Die Termination)	Speed Grade –1		Units
		t_{PY}	t_{PYS}	
LVCMOS 1.5 V (for DDRIO I/O Bank with Fixed Codes)	none	2.19	2.216	ns
LVCMOS 1.5 V (for MSIO I/O Bank)	none	3.679	3.652	ns
	50	4.151	4.126	ns
	75	3.984	3.953	ns
	150	3.823	3.791	ns
LVCMOS 1.5 V (for MSIOD I/O Bank)	none	3.262	3.229	ns
	50	3.76	3.739	ns
	75	3.555	3.52	ns
	150	3.395	3.359	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 45 • LVCMOS 1.5 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Military Conditions: T_J=125°C, VDD=1.14 V, VDDI=1.425 V

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVCMOS 1.5 V (for DDRIO I/O Bank with Fixed Codes)							
2 mA	slow	5.712	4.796	5.735	5.814	5.138	ns
	medium	5.094	4.274	5.114	5.484	4.779	ns
	medium_fast	4.793	4.013	4.81	5.288	4.625	ns
	fast	4.762	3.98	4.78	5.261	4.615	ns
4 mA	slow	4.966	4.133	4.956	6.763	6.05	ns
	medium	4.412	3.62	4.401	6.433	5.664	ns
	medium_fast	4.145	3.358	4.131	6.249	5.507	ns
	fast	4.116	3.338	4.103	6.238	5.498	ns
6 mA	slow	4.744	3.869	4.728	7.173	6.383	ns
	medium	4.212	3.382	4.195	6.837	6.004	ns
	medium_fast	3.951	3.135	3.93	6.668	5.861	ns
	fast	3.919	3.11	3.899	6.644	5.845	ns

8.7.5.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 70 • **DDR3/STTL15 AC Switching Characteristics for Receiver (Input Buffers)**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.425 V

		Speed Grade –1	
	ODT (On Die Termination)	t_{PY}	Units
DDR3/SSTL15 (for DDRIO I/O Bank) – Calibration Mode Only			
Pseudo-Differential	None	1.672	ns
True-Differential	None	1.694	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 71 • **DDR3/SSTL15 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.425 V

	Speed Grade –1					
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	Units
DDR3 Reduced Drive/SSTL15 Class I (for DDRIO I/O Bank)						
Single Ended	2.832	2.766	2.767	2.658	2.659	ns
Differential	2.848	3.401	3.393	3.173	3.166	ns
DDR3 Full Drive/SSTL15 Class II (for DDRIO I/O Bank)						
Single Ended	2.832	2.76	2.759	2.655	2.655	ns
Differential	2.845	3.397	3.387	3.179	3.171	ns

8.7.6 Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer. This I/O standard is supported in DDRIO I/O Bank only.

8.7.6.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 72 • **LPDDR AC/DC Specifications (for DDRIO IO Bank Only)**

Symbols	Parameters	Conditions	Min	Typ	Max	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.71	1.8	1.89	V	–
VTT	Termination voltage		0.838	0.900	0.964	V	–
VREF	Input reference voltage		0.838	0.900	0.964	V	–
LPDDR DC Input Voltage Specification							
VIH (DC)	DC input logic High		0.7 × VDDI	–	1.89	V	–
VIL (DC)	DC input logic Low		–0.3	–	0.3 × VDDI	V	–
IIH (DC)	Input current High		–	–	10	µA	–
IIL (DC)	Input current Low		–	–	10	µA	–
LPDDR DC Output Voltage Specification							

8.7.6.2 AC Switching Characteristics

Table 75 • LPDDR AC Switching Characteristics for Receiver (Input Buffers)
Worst-Case Military Conditions: T_J=125°C, VDD=1.14 V, VDDI= 1.71 V

		Speed Grade –1	
	ODT (On Die Termination)	t_{PY}	Units
LPDDR (for DDRIO I/O Bank with Fixed Codes)			
Pseudo-Differential	None	1.633	ns
True-Differential	None	1.65	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 76 • LPDDR AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Military Conditions: T_J=125°C, VDD=1.14 V, VDDI= 1.71 V

	Speed Grade –1					
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	Units
LPDDR Reduced Drive (for DDRIO I/O Bank)						
Single Ended	2.645	2.431	2.434	2.396	2.398	ns
Differential	2.652	3.044	3.038	2.46	2.455	ns
LPDDR Full Drive (for DDRIO I/O Bank)						
Single Ended	2.532	2.401	2.398	2.368	2.365	ns
Differential	2.546	2.509	2.503	2.852	2.845	ns

8.7.6.3 Minimum and Maximum AC/DC Input and Output Levels Specification using LPDDR-LVCMOS 1.8 V Mode

Table 77 • LPDDR-LVCMOS 1.8 V Mode, Minimum and Maximum DC Input and Output Levels (Applicable to DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LPDDR-LVCMOS 1.8 V Recommended DC Operating Conditions						
VDDI	Supply Voltage	–	1.710	1.8	1.89	V
LPDDR-LVCMOS 1.8 V Mode DC Input Voltage Specification						
VIH(DC)	DC input Logic HIGH for (MSIOD and DDRIO I/O Banks)	–	0.65 x VDDI	–	1.89	V
VIH(DC)	DC input Logic HIGH (for MSIO I/O Bank)	–	0.65 x VDDI	–	3.45	V
VIL(DC)	DC input Logic LOW	–	-0.3	–	0.35 x VDDI	V
IIH(DC)	Input current HIGH	–	–	–	10	uA
IIL(DC)	Input current LOW	–	–	–	10	uA
LPDDR-LVCMOS 1.8 V Mode DC Output Voltage Specification						
VOH	DC output Logic HIGH	–	VDDI - 0.45	–	–	V
VOL	DC output Logic LOW	–	–	–	0.45	V

8.8.2.2. AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 91 • **B-LVDS AC Switching Characteristics for Receiver (Input Buffers)**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 2.375 V

	On-Die Termination (ODT)	Speed Grade –1	Units
		t_{PY}	
Bus-LVDS (for MSIO I/O Bank)	None	3.011	ns
	100	3.006	ns
Bus-LVDS (for MSIOD I/O Bank)	None	2.722	ns
	100	2.725	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 92 • **B-LVDS AC *Switching Characteristics for Transmitter (Output and Tristate Buffers)***
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 2.375 V

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
Bus-LVDS (for MSIO I/O Bank)	2.78	2.632	2.617	2.448	2.436	ns

8.8.3 M-LVDS

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

8.8.3.1 Minimum and Maximum Input and Output Levels

Table 93 • **M-LVDS DC Voltage Specification**

Symbols	Parameters	Conditions	Min	Typ	Max	Units	Notes
M-LVDS Recommended DC Operating Conditions							–
VDDI	Supply voltage		2.375	2.5	2.625	V	*
M-LVDS DC Input Voltage Specification							–
VI	DC input voltage		0	–	2.925	V	–
IIH (DC)	Input current High		–	–	10	µA	–
IIL (DC)	Input current Low		–	–	10	µA	–
M-LVDS DC Output Voltage Specification (for MSIO I/O Bank Only)							–
VOH	DC output logic High		1.25	1.425	1.6	V	–
VOL	DC output logic Low		0.9	1.075	1.25	V	–
M-LVDS Differential Voltage Specification							–
VOD	Differential output voltage Swing (for MSIO I/O Bank only)		300	–	650	mV	–
VOCM	Output common mode voltage (for MSIO I/O Bank only)		0.3	–	2.1	V	–
VICM	Input common mode voltage		0.3	–	1.2	V	–

8.8.4 Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

8.8.4.1 Mini-LVDS Minimum and Maximum Input and Output Levels

Table 97 • **Mini-LVDS DC Voltage Specification**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
VDDI	Supply voltage		2.375	2.5	2.625	V
Mini-LVDS DC Input Voltage Specification						
VI	DC Input voltage		0	–	2.925	V
Mini-LVDS DC Output Voltage Specification						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
Mini-LVDS Differential Voltage Specification						
VOD	Differential output voltage swing		300	–	600	mV
VOCM	Output common mode voltage		1	–	1.4	V
VICM	Input common mode voltage		0.3	–	1.2	V
VID	Input differential voltage		100	–	600	mV

Table 98 • **Mini-LVDS AC Specifications**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Mini-LVDS Maximum AC Switching Speed						
Dmax	Maximum data rate (MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	460	Mbps
Dmax	Maximum data rate (MSIOD I/O Bank)	AC loading: 10 pF / 100 Ω differential load	–	–	480	Mbps
Mini-LVDS Impedance Specification						
Rt	Termination resistance		–	100	–	Ω
Mini-LVDS AC Test Parameters Specifications						
VTrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF

8.10.3 Timing Characteristics

Table 110 • Input DDR Propagation Delays
Worst-Case Military Conditions: T_J = 125°C, VDD=1.14 V

Parameter	Description	Measuring Nodes (from, to)	Speed Grade –1	Units
tDDRICLKQ1	Clock-to-Out Out_QR for Input DDR	B,C	0.165	ns
tDDRICLKQ2	Clock-to-Out Out_QF for Input DDR	B,D	0.172	ns
tDDRISUD	Data Setup for Input DDR	A,B	0.372	ns
tDDRIHD	Data Hold for Input DDR	A,B	0	ns
tDDRISUE	Enable Setup for Input DDR	E,B	0.475	ns
tDDRIHE	Enable Hold for Input DDR	E,B	0	ns
tDDRISUSLn	Synchronous Load Setup for Input DDR	G,B	0.475	ns
tDDRIHSLn	Synchronous Load Hold for Input DDR	G,B	0	ns
tDDRIAL2Q1	Asynchronous Load-to-Out QR for Input DDR	F,C	0.606	ns
tDDRIAL2Q2	Asynchronous Load-to-Out QF for Input DDR	F,D	0.558	ns
tDDRIREMAL	Asynchronous Load Removal time for Input DDR	F,B	0	ns
tDDRIRECAL	Asynchronous Load Recovery time for Input DDR	F,B	0.076	ns
tDDRIWAL	Asynchronous Load Minimum Pulse Width for Input DDR	F,F	0.313	ns
tDDRICKMPWH	Clock Minimum Pulse Width High for Input DDR	B,B	0.078	ns
tDDRICKMPWL	Clock Minimum Pulse Width Low for Input DDR	B,B	0.164	ns

9. Logic Element Specifications

9.1 4-input LUT (LUT-4)

The IGLOO2 and SmartFusion2 SoC FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *SmartFusion2 and IGLOO2 Macro Library Guide*.

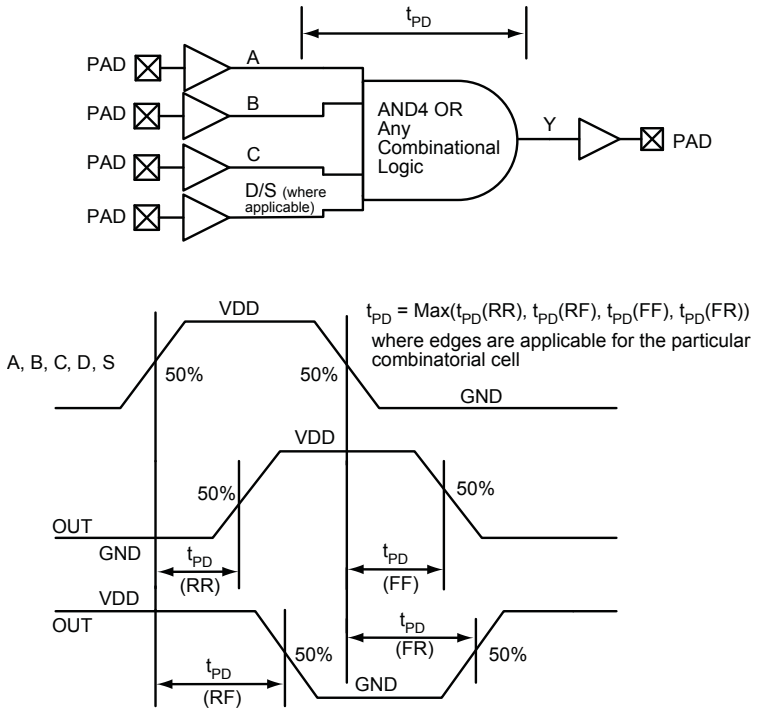

Figure 13 • **LUT-4**

Timing Characteristics

Table 112 • **Combinatorial Cell Propagation Delays**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Combinatorial Cell	Equation	Parameter	Speed Grade –1	Units
INV	Y = !A	t_{PD}	0.106	ns
AND2	Y = A · B	t_{PD}	0.17	ns
NAND2	Y = !(A · B)	t_{PD}	0.157	ns
OR2	Y = A + B	t_{PD}	0.17	ns
NOR2	Y = !(A + B)	t_{PD}	0.157	ns
XOR2	Y = A ⊕ B	t_{PD}	0.17	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.236	ns
AND3	Y = A · B · C	t_{PD}	0.217	ns
AND4	Y = A · B · C · D	t_{PD}	0.384	ns

Table 119 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1Kx18
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tsrstsu	Synchronous Reset Setup Time	0.233	–	ns
tsrsthd	Synchronous Reset Hold Time	0.037	–	ns
twesu	Write Enable Setup Time	0.402	–	ns
twehd	Write Enable Hold Time	0.25	–	ns
Fmax	Maximum Frequency	–	300	MHz

Table 120 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2Kx9
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tcy	Clock Period	3.333	–	ns
tclkmpwh	Clock Minimum Pulse Width High	1.5	–	ns
tclkmpwl	Clock Minimum pulse Width Low	1.5	–	ns
tplcy	Pipelined Clock Period	3.333	–	ns
tplclkmpwh	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
tplclkmpwl	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.346	ns
	Read Access Time without Pipeline Register	–	2.346	ns
	Access Time with Feed-Through Write Timing	–	1.578	ns
taddrsu	Address Setup Time	0.49	–	ns
taddrhd	Address Hold Time	0.282	–	ns
tdsu	Data Setup Time	0.346	–	ns
tdhd	Data Hold Time	0.084	–	ns
tblksu	Block Select Setup Time	0.214	–	ns
tblkhd	Block Select Hold Time	0.223	–	ns
tblk2q	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	1.578	ns
tblkmpw	Block Select Minimum Pulse Width	0.218	–	ns
trdesu	Read Enable Setup Time	0.5	–	ns
trdehd	Read Enable Hold Time	0.073	–	ns
trdplesu	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
trdplehd	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
tr2q	Asynchronous Reset to Output Propagation Delay	–	1.569	ns

Table 124 • RAM1K18 – Two-Port Mode for Depth × Width Configuration 512x36
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
twehd	Write Enable Hold Time	0.25	–	ns
Fmax	Maximum Frequency	–	300	MHz

11.2 FPGA Fabric Micro SRAM (uSRAM)

Table 125 • uSRAM (RAM64x18) in 64x18 Mode
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tcy	Read Clock Period	4	–	ns
tclkmpwh	Read Clock Minimum Pulse Width High	1.8	–	ns
tclkmpwl	Read Clock Minimum pulse Width Low	1.8	–	ns
tplcy	Read Pipe-line clock period	4	–	ns
tplclkmpwh	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
tplclkmpwl	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.738	ns
taddrsu	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	1.916	–	ns
taddrhd	Read Address Hold Time in Synchronous Mode	0.094	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.803	–	ns
trdensu	Read Enable Setup Time	0.287	–	ns
trdenhd	Read Enable Hold Time	0.059	–	ns
tblksu	Read Block Select Setup Time	1.898	–	ns
tblkhd	Read Block Select Hold Time	-0.671	–	ns
tblk2q	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.102	ns
trstrem	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
trstrec	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
tr2q	Read Asynchronous Reset to Output Propagation Delay (with Pipe-Line Register Enabled)	–	0.869	ns

Table 125 • **uSRAM (RAM64x18) in 64x18 Mode**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tsrstsu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.062	–	ns
tccy	Write Clock Period	4	–	ns
tcclkmpwh	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclkmpwl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblkcsu	Write Block Setup Time	0.417	–	ns
tblkchd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.119	–	ns
tdinchd	Write Input Data hold Time	0.155	–	ns
taddrcsu	Write Address Setup Time	0.091	–	ns
taddrchd	Write Address Hold Time	0.132	–	ns
twecsu	Write Enable Setup Time	0.41	–	ns
twechd	Write Enable Hold Time	-0.027	–	ns
fmax	Maximum Frequency	–	250	MHz

Table 126 • **uSRAM (RAM64x16) in 64x16 Mode**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tcy	Read Clock Period	4	–	ns
tclkmpwh	Read Clock Minimum Pulse Width High	1.8	–	ns
tclkmpwl	Read Clock Minimum pulse Width Low	1.8	–	ns
tplcy	Read Pipe-line clock period	4	–	ns
tplclkmpwh	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
tplclkmpwl	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.738	ns
taddrsu	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	1.916	–	ns
taddrhd	Read Address Hold Time in Synchronous Mode	0.094	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.803	–	ns
trdensu	Read Enable Setup Time	0.287	–	ns

Table 129 • uSRAM (RAM256x4) in 256x4 Mode
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
trdenhd	Read Enable Hold Time	0.059	–	ns
tblksu	Read Block Select Setup Time	1.898	–	ns
tblkhd	Read Block Select Hold Time	-0.671	–	ns
tblk2q	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.166	ns
trstrem	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
trstrec	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
tr2q	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.863	ns
tsrstsu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.062	–	ns
tccy	Write Clock Period	4	–	ns
tcclkmpwh	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclkmpwl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblkcsu	Write Block Setup Time	0.417	–	ns
tblkchd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.104	–	ns
tdinchd	Write Input Data hold Time	0.142	–	ns
taddrcsu	Write Address Setup Time	0.091	–	ns
taddrchd	Write Address Hold Time	0.253	–	ns
twecsu	Write Enable Setup Time	0.41	–	ns
twechd	Write Enable Hold Time	-0.027	–	ns
fmax	Maximum Frequency	–	250	MHz

Table 130 • uSRAM (RAM512x2) in 512x2 Mode
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tcy	Read Clock Period	4	–	ns
tclkmpwh	Read Clock Minimum Pulse Width High	1.8		ns

15. Clock Conditioning Circuits (CCC)

Table 139 • **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification**
Military Worst-Case Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Conditions	Min	Typ	Max	Units	Notes
Clock conditioning circuitry input frequency f_{IN_CCC}	All CCC	1	–	200	MHz	–
	32 kHz Capable CCC	0.032		200	MHz	–
Clock conditioning circuitry output frequency f_{OUT_CCC}	–	0.078	–	400	MHz	1
PLL VCO frequency	–	500	–	1000	MHz	2
Delay increments in programmable delay blocks	–	–	75	100	ps	–
Number of programmable values in each programmable delay block	–	–	–	64	–	–
Acquisition time	–	–	70	100	µs	–
Input Duty Cycle (Reference Clock)	Internal Feedback					
	1 MHz ≤ f_{IN_CCC} ≤ 25 MHz	10	–	90	%	–
	25 MHz ≤ f_{IN_CCC} ≤ 100 MHz	25	–	75	%	–
	100 MHz ≤ f_{IN_CCC} ≤ 150 MHz	35	–	65	%	–
	150 MHz ≤ f_{IN_CCC} ≤ 200 MHz	45	–	55	%	–
	External Feedback (CCC, FPGA, Off-chip)					
	1 MHz ≤ f_{IN_CCC} ≤ 25 MHz	25	–	75	%	–
	25 MHz ≤ f_{IN_CCC} ≤ 35 MHz	35	–	65	%	–
	35 MHz ≤ f_{IN_CCC} ≤ 50 MHz	45	–	55	%	–
Output duty cycle	010, 025, and 050 Devices	46	–	52	%	–
	090 and 150 Devices	44	–	52	%	–
Spread Spectrum Characteristics						
Modulation frequency range	–	25	35	50	kHz	–
Modulation depth range	–	0	–	1.5	%	–
Modulation depth control	–	–	0.5	–	%	–

Notes:

1. *The minimum output clock frequency is limited by the PLL. For more information refer to the UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide.*
2. *The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance will be limited by the CCC output frequency.*

19. Mathblock Timing Characteristics

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. Each IGLOO2 and SmartFusion2 SoC mathblock supports 18x18 signed multiplication, dot product, and built-in addition, subtraction, and accumulation units to combine multiplication results efficiently.

Table 145 • **Mathblocks With All Registers Used**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Mathblock With All Registers Used		Speed Grade –1		
Parameter	**Description**	**Min**	**Max**	**Units**
TMISU	Input, Control Register Setup time	0.149	–	ns
TMIHD	Input, Control Register Hold time	0.08	–	ns
TMOCDINSU	CDIN Input Setup time	1.68	–	ns
TMOCDINHD	CDIN Input Hold time	-0.419	–	ns
TMSRSTENSU	Synchronous Reset/Enable Setup time	0.185	–	ns
TMSRSTENHD	Synchronous Reset/Enable Hold time	0.011	–	ns
TMARSTREM	Asynchronous Reset Removal time	0	–	ns
TMARSTREC	Asynchronous Reset Recovery time	0.088	–	ns
TMOCQ	Output Register Clock to Out delay	–	0.232	ns
TMCLKMP	CLK Minimum period	2.245	–	ns

Table 146 • **Mathblock With Input Bypassed and Output Registers Used**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Mathblock With Input Bypassed and Output Registers Used		Speed Grade –1		
Parameter	**Description**	**Min**	**Max**	**Units**
TMOSU	Output Register Setup time	2.294	–	ns
TMOHD	Output Register Hold time	-0.444	–	ns
TMOCDINSU	CDIN Input Setup time	1.68	–	ns
TMOCDINHD	CDIN Input Hold time	-0.419	–	ns
TMSRSTENSU	Synchronous Reset/Enable Setup time	0.115	–	ns
TMSRSTENHD	Synchronous Reset/Enable Hold time	0.011	–	ns
TMARSTREM	Asynchronous Reset Removal time	0	–	ns
TMARSTREC	Asynchronous Reset Recovery time	0.014	–	ns
TMOCQ	Output Register Clock to Out delay	–	0.232	ns
TMCLKMP	CLK Minimum period	2.179	–	ns

23. PCIe Electrical and Timing AC and DC Characteristics

PCIe® is a high speed, packet-based, point-to-point, low pin count, serial interconnect bus. The IGLOO2 and SmartFusion2 SoC FPGAs has up to four hard high-speed serial interface blocks. Each SERDES block contains a PCIe system block. The PCIe system is connected to the SERDES block.

Table 152 • **Transmitter Parameters**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Min	Typ	Max	Units
VTX-DIFF-PP	Differential swing PCIe Gen1	0.8	–	1.2	V
VTX-CM-AC-P	Output common mode voltage PCIe Gen1	–	–	20	mV
VTX-RISE-FALL	Rise and fall time (20% to 80%) PCIe Gen1	0.125	–	–	UI
ZTX-DIFF-DC	Output impedance – differential	80	–	120	Ω
LTX-SKEW	Lane-to-lane TX skew within a SERDES block PCIe Gen1	–	–	500 ps + 2 UI	ps
RLTX-DIFF	Return loss differential mode PCIe Gen1	–10	–	–	dB
RLTX-CM	Return loss common mode PCIe Gen1	–6	–	–	dB
TX-LOCK-RST	Transmit PLL lock time from reset	–	–	10	µs

Table 153 • **Receiver Parameters**
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Min	Typ	Max	Units
VRX-DIFF-PP-CC	Input levels PCIe Gen1	0.175	–	1.2	V
VRX-CM-DC-P	Input common mode range (DC coupled) Note: PCIe standard mandates AC coupling	NA	NA	NA	–
VRX-CM-AC-P	Input common mode range (AC coupled)	–	–	150	mV
VRX-DIFF-PP-CC	Differential input sensitivity Gen1	0.175	–	–	mV
ZRX-DIFF-DC	Differential input termination	80	100	120	Ω
REXT	External calibration resistor	1,188	1,200	1,212	Ω
CDR-LOCK-RST	CDR relock time from reset	–	–	15	µs
RLRX-DIFF	Return loss differential mode PCIe Gen1	–10	–	–	dB
RLRX-CM	Return loss common mode PCIe Gen1	–6	–	–	dB
	CID limit (set by 8B/10B coding, not the receiver PLL)	–	–	4	UI
VRX-IDLE-DET-DIFF-PP	Signal detect limit	65	–	175	mV

Table 154 • **SERDES Reference Clock AC Specifications**
Worst-Case Military Conditions: T_J = 125°C, Worst-Case VDD = 1.14V

Symbols	Description	Min	Typ	Max	Units
FREFCLK	Reference Clock Frequency	100	–	160	MHz
TRISE	Reference Clock Rise Time	0.6	–	4	V/ns
TFALL	Reference Clock Fall Time	0.6	–	4	V/ns
TCYC	Reference Clock Duty Cycle	40	–	60	%
Mmrefclk	Reference Clock Mismatch	-300	–	300	ppm
SSCref	Reference Spread Spectrum Clock	0	–	5000	ppm