



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I ² C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 150K Logic Modules
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s150t-1fc1152m

5. Power Consumption

5.1 Quiescent Supply Current

Table 8 • Quiescent Supply Current Characteristics

Power Supplies/Blocks	Modes and Configurations		Notes
	Non-Flash*Freeze Mode	Flash*Freeze Mode	
FPGA Core	On	Off	–
VDD / SERDES_[01]_VDD	On	On	1
VPP / VPPNVM	On	On	–
MDDR_PLL_VDDA CCC_XX[01]_PLL_VDDA PLL0_PLL1_MDDR_VDDA FDDR_PLL_VDDA	0 V	0 V	–
SERDES_[01]_PLL_VDDA	0 V	0 V	3
SERDES_[01]_L[0123]_VDDAPLL / VDD_2V5	On	On	3
SERDES_[01]_L[0123]_VDDAIIIO	On	On	3
VDDIx	On	On	2, 4
VREFx	On	On	–
MSSDDR CLK	32 kHz	32 kHz	–
RAM	On	Sleep state	–
HPMS Controller	50 MHz	50 MHz	–
50 MHz Oscillator (enable/disable)	Enabled	Disabled	–
1 MHz Oscillator (enable/disable)	Disabled	Disabled	–
Crystal Oscillator (enable/disable)	Disabled	Disabled	–
Notes: 1. SERDES_[01]_VDD Power Supply is shorted to VDD. 2. VDDIx has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate VDDI Bank supplies. For details on bank power supplies, refer to the “Recommendation for Unused Bank Supplies” table in the AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note. 3. SERDES and DDR blocks to be unused. 4. No Differential (that is to say, LVDS) I/O's or ODT attributes to be used.			

Table 9 • SmartFusion2 and IGLOO2 Quiescent Supply Current – Typical Process

Parameter	Modes	Conditions	010	025	050	090	150	Units
			VDD=1.2 V	VDD=1.2 V	VDD=1.2 V	VDD=1.2 V	VDD=1.2 V	
IDC1	Non-Flash*Freeze	Typical (T _J = 25°C)	6.9	8.9	13.1	15.4	27.5	mA
		Military (T _J = 125°C)	73.0	106.4	180.9	217.5	390.5	mA
IDC2	Flash*Freeze	Typical (T _J = 25°C)	2.6	3.7	5.1	5.1	8.9	mA
		Military (T _J = 125°C)	55.6	74.2	98.5	99.5	161.0	mA

8.4 I/O Speeds

Table 16 • Maximum Data Rate Summary for Worst-Case Military Conditions

Single-Ended I/O	MSIO	MSIOD	DDRIO	Units
PCI 3.3 V	560	–	–	Mbps
LVTTL 3.3 V	540	–	–	Mbps
LVC MOS 3.3 V	540	–	–	Mbps
LVC MOS 2.5 V	360	370	360	Mbps
LVC MOS 1.8 V	260	360	360	Mbps
LVC MOS 1.5 V	140	190	210	Mbps
LVC MOS 1.2 V	100	140	180	Mbps
LPDDR – LVC MOS 1.8 V Mode	–	–	360	Mbps
Voltage-Referenced I/O	MSIO	MSIOD	DDRIO	Units
LPDDR	–	–	360	Mbps
HSTL 1.5 V	–	–	360	Mbps
SSTL 2.5 V	450	480	360	Mbps
SSTL 1.8 V	–	–	600	Mbps
Voltage-Referenced I/O	MSIO	MSIOD	DDRIO	Units
SSTL 1.5 V	–	–	600	Mbps
Differential I/O	MSIO	MSIOD	DDRIO	Units
LVPECL (input only)	810	–	–	Mbps
LVDS 3.3 V	480	480	–	Mbps
LVDS 2.5 V	480	480	–	Mbps
RSDS	460	480	–	Mbps
BLVDS	450	–	–	Mbps
MLVDS	450	–	–	Mbps
Mini-LVDS	460	480	–	Mbps

8.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

8.6.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 21 • LVTTL/LVCMOS 3.3 V DC Voltage Specification (Applicable to MSIO I/O Bank Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units	Notes
LVTTL/LVCMOS 3.3 V Recommended DC Operating Conditions							
VDDI	Supply voltage		3.15	3.3	3.45	V	–
LVTTL/LVCMOS 3.3 V DC Input Voltage Specification							
VIH (DC)	DC input logic High		2.0	–	3.45	V	–
VIL (DC)	DC input logic Low		–0.3	–	0.8	V	–
IIH (DC)	Input current High		–	–	10	μA	–
IIL (DC)	Input current Low		–	–	10	μA	–
LVCMOS 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		2.4	–	–	V	*
VOL	DC output logic Low		–	–	0.4	V	*
LVTTL 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		2.4	–	–	V	–
VOL	DC output logic Low		–	–	0.4	V	–
Note: * The VOH/VOL test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.							

Table 22 • LVTTL/LVCMOS 3.3 V Maximum Switching Speeds (Applicable to MSIO I/O Bank Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
LVTTL/LVCMOS 3.3 V Maximum Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	540	Mbps

Table 23 • LVTTL/LVCMOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO Bank Only)

LVTTL/LVCMOS 3.3 V AC Test Parameter Specifications						
Symbol	Parameters	Conditions	Min	Typ	Max	Units
Vtrip	Measuring/trip point for data path		–	1.4	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

Table 39 • LVCMOS 1.8 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-case Military conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.71\text{ V}$ (continued)

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
12 mA	slow	3.795	3.096	3.773	6.773	6.067	ns
	medium	3.408	2.764	3.389	6.47	5.743	ns
	medium_fast	3.215	2.599	3.194	6.346	5.61	ns
	fast	3.196	2.584	3.175	6.335	5.604	ns
16 mA	slow	3.744	3.035	3.719	6.944	6.207	ns
	medium	3.358	2.712	3.339	6.657	5.868	ns
	medium_fast	3.175	2.546	3.153	6.547	5.751	ns
	fast	3.156	2.531	3.133	6.541	5.747	ns
LVCMOS 1.8 V (for MSIO I/O Bank)							
2 mA	slow	3.957	4.784	5.023	5.643	5.866	ns
4 mA	slow	3.668	4.162	4.485	6.543	6.382	ns
6 mA	slow	3.586	3.994	4.358	7.622	6.941	ns
8 mA	slow	3.616	3.782	4.162	7.988	7.161	ns
10 mA	slow	3.662	3.732	4.121	8.396	7.423	ns
12 mA	slow	3.75	3.615	4.006	8.576	7.543	ns
LVCMOS 1.8 V (for MSIOD I/O Bank)							
2 mA	slow	3.048	3.692	3.898	5.818	5.609	ns
4 mA	slow	2.5	3.088	3.288	6.421	6.121	ns
6 mA	slow	2.225	2.747	2.937	7.18	6.753	ns
8 mA	slow	2.233	2.72	2.904	7.49	6.992	ns
10 mA	slow	2.263	2.577	2.759	7.851	7.253	ns

8.6.5 1.5 V LVCMOS

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-11A.

8.6.5.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 40 • LVCMOS 1.5 V Minimum and Maximum DC Input and Output Levels

Symbols	Parameters	Min	Typ	Max	Units
LVCMOS 1.5 V Recommended DC Operating Conditions					
VDDI	Supply voltage	1.425	1.5	1.575	V
LVCMOS 1.5 V DC Input Voltage Specification					
VIH (DC)	DC input logic High for (MSIOD and DDRIO I/O banks)	$0.65 \times V_{DDI}$	–	1.575	V
VIH (DC)	DC input logic High (for MSIO I/O Bank)	$0.65 \times V_{DDI}$	–	2.75	V
VIL (DC)	DC input logic Low	–0.3	–	$0.35 \times V_{DDI}$	V
IIH (DC)	Input current High	–	–	10	μA
IIL (DC)	Input current Low	–	–	10	μA
LVCMOS 1.5 V DC Output Voltage Specification					
VOH	DC output logic High	$V_{DDI} \times 0.75$	–	–	V
VOL	DC output logic Low	–	–	$V_{DDI} \times 0.25$	V

Table 41 • LVCMOS 1.5 V Maximum AC Switching Speeds

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 1.5 V Maximum AC Switching Speed						
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	210	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	140	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	190	Mbps

Table 42 • LVCMOS 1.5 V AC Test Parameters and Driver Impedance Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 1.5 V AC Calibrated Impedance Option						
Rodt_cal	Supported output driver calibrated impedance (for DDRIO I/O Bank)		–	75, 60, 50, 40	–	Ω
LVCMOS 1.5 V AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	0.75	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

Table 43 • LVCMOS 1.5 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (with Fixed Code)	Min	Max		
2 mA	2 mA	2 mA	VDDI × 0.75	VDDI × 0.25	2	2
4 mA	4 mA	4 mA	VDDI × 0.75	VDDI × 0.25	4	4
6 mA	6 mA	6 mA	VDDI × 0.75	VDDI × 0.25	6	6
8 mA	N/A	8 mA	VDDI × 0.75	VDDI × 0.25	8	8
N/A	N/A	10 mA	VDDI × 0.75	VDDI × 0.25	10	10
N/A	N/A	12 mA	VDDI × 0.75	VDDI × 0.25	12	12

8.6.5.2. AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 44 • LVCMOS 1.5 V AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Military Conditions: $T_J=125^{\circ}\text{C}$, $V_{DD}=1.14\text{ V}$, $V_{DDI}=1.425\text{ V}$

	ODT (On Die Termination)	Speed Grade -1		Units
		t_{PV}	t_{PVS}	
LVCMOS 1.5 V (for DDRIO I/O Bank with Fixed Codes)	none	2.19	2.216	ns
LVCMOS 1.5 V (for MSIO I/O Bank)	none	3.679	3.652	ns
	50	4.151	4.126	ns
	75	3.984	3.953	ns
	150	3.823	3.791	ns
LVCMOS 1.5 V (for MSIOD I/O Bank)	none	3.262	3.229	ns
	50	3.76	3.739	ns
	75	3.555	3.52	ns
	150	3.395	3.359	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 45 • LVCMOS 1.5 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-Case Military Conditions: $T_J=125^{\circ}\text{C}$, $V_{DD}=1.14\text{ V}$, $V_{DDI}=1.425\text{ V}$

Output Drive Selection	Slew Control	Speed Grade -1					Units
		t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
LVCMOS 1.5 V (for DDRIO I/O Bank with Fixed Codes)							
2 mA	slow	5.712	4.796	5.735	5.814	5.138	ns
	medium	5.094	4.274	5.114	5.484	4.779	ns
	medium_fast	4.793	4.013	4.81	5.288	4.625	ns
	fast	4.762	3.98	4.78	5.261	4.615	ns
4 mA	slow	4.966	4.133	4.956	6.763	6.05	ns
	medium	4.412	3.62	4.401	6.433	5.664	ns
	medium_fast	4.145	3.358	4.131	6.249	5.507	ns
	fast	4.116	3.338	4.103	6.238	5.498	ns
6 mA	slow	4.744	3.869	4.728	7.173	6.383	ns
	medium	4.212	3.382	4.195	6.837	6.004	ns
	medium_fast	3.951	3.135	3.93	6.668	5.861	ns
	fast	3.919	3.11	3.899	6.644	5.845	ns

Table 46 • LVCMOS 1.2 V Minimum and Maximum DC Input and Output Levels

IIL (DC)	Input current Low	–	–	10	μA
LVCMOS 1.2 V DC Output Voltage Specification					
VOH	DC output logic High	–	VDDI × 0.75	–	V
VOL	DC output logic Low	–	–	VDDI × 0.25	V

Table 47 • LVCMOS 1.2 V Maximum AC Switching Speeds

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 1.2 V Maximum AC Switching Speed						
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	180	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	100	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	140	Mbps

Table 48 • LVCMOS 1.2 V AC Calibrated Impedance and Test Parameters Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 1.2 V AC Calibrated Impedance Option						
Rodt_cal	Supported output driver calibrated impedance (for DDRIO I/O Bank)		–	75, 60, 50, 40	–	Ω
LVCMOS 1.2 V AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	0.6	–	V
Rent	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF
Cload	Capacitive loading for data path (t _{DP})		–	5	–	pF

Table 49 • LVCMOS 1.2 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (with Fixed Code)	Min	Max		
2 mA	2 mA	2 mA	VDDI × 0.75	VDDI × 0.25	2	2
4 mA	4 mA	4 mA	VDDI × 0.75	VDDI × 0.25	4	4
N/A	N/A	6 mA	VDDI × 0.75	VDDI × 0.25	6	6

Table 56 • HSTL DC Voltage Specification (Applicable to DDRIO I/O Bank Only) (continued)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
VOL	DC output logic Low		–	–	0.4	V
IOH at VOH	Output minimum source DC current		–15.0	–	–	mA
IOL at VOL	Output minimum sink current		15.0	–	–	mA
HSTL DC Differential Voltage Specifications						
VID (DC)	DC input differential voltage		0.2	–	–	V

Table 57 • HSTL AC Specifications (Applicable to DDRIO Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
HSTL AC Differential Voltage Specifications						
VDIFF	AC input differential voltage		0.4	–	–	V
Vx	AC differential cross point voltage		0.68	–	0.9	V
HSTL Maximum AC Switching Speed						
Dmax	Maximum data rate	AC loading: per JEDEC specifications	–	–	360	Mbps
HSTL Impedance Specification						
Rref	Supported output driver calibrated impedance (for DDRIO I/O Bank)	Reference resistance = 191 Ω	–	25.5, 47.8	–	Ω
RTT	Effective impedance value (ODT for DDRIO I/O Bank only)	Reference resistance = 191 Ω	–	47.8	–	Ω
HSTL AC Test Parameters Specification						
Vtrip	Measuring/trip point for data path		–	0.75	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF
Rtt_test	Reference resistance for data test path for HSTL15 Class I (t_{DP})		–	50	–	Ω
Rtt_test	Reference resistance for data test path for HSTL15 Class II (t_{DP})		–	25	–	Ω
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

8.7.1.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 58 • HSTL15 AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Military Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.425\text{ V}$

	ODT (On Die Termination)	t _{PY}	Units
		Speed Grade –1	
HSTL (for DDRIO I/O Bank with Fixed Code)			
Pseudo-Differential	None	1.673	ns
True-Differential	None	1.693	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 59 • HSTL 15 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.425\text{ V}$

	Speed Grade -1					Units
	t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
HSTL Class I (for DDRIO I/O Bank)						
Single Ended	2.922	2.91	2.904	3.225	3.218	ns
Differential	2.907	2.757	2.755	2.662	2.66	ns
HSTL Class II (for DDRIO I/O Bank)						
Single Ended	2.817	2.735	2.735	2.644	2.644	ns
Differential	2.827	2.81	2.803	3.205	3.197	ns

8.7.2 Stub-Series Terminated Logic

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in IGLOO2 and SmartFusion2 SoC FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. IGLOO2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

8.7.3 Stub-Series Terminated Logic 2.5 V (SSTL2)

SSTL2 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs and also comply with reduced and full drive of double data rate (DDR) standards. IGLOO2 and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

8.7.3.1 Minimum and Maximum DC Input and Output Levels Specification

Table 60 • DDR1/SSTL2 Minimum and Maximum DC Input and Output Levels

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
VDDI	Supply voltage		2.375	2.5	2.625	V
VTT	Termination voltage		1.164	1.250	1.339	V
VREF	Input reference voltage		1.164	1.250	1.339	V
SSTL2 DC Input Voltage Specification						
VIH (DC)	DC input logic High	$V_{REF} + 0.15$	–	–	2.625	V
VIL (DC)	DC input logic Low	–0.3	–	–	$V_{REF} - 0.15$	V
IIH (DC)	Input current High	–	–	–	10	μA
IIL (DC)	Input current Low	–	–	–	10	μA
SSTL2 DC Output Voltage Specification						
SSTL2 Class I (DDR Reduced Drive)						
VOH	DC output logic High	$V_{TT} + 0.608$	–	–	–	V
VOL	DC output logic Low	–	–	–	$V_{TT} - 0.608$	V
IOH at VOH	Output minimum source DC current	8.1	–	–	–	mA

8.7.3.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 62 • DDR1/SSTL2 AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	ODT (On Die Termination)	Speed Grade –1	Units
		t _{PY}	
SSTL2 (DDRIO I/O Bank)			
Pseudo-Differential	None	1.613	ns
True-Differential	None	1.647	ns
SSTL2 (MSIO I/O Bank)			
Pseudo-Differential	None	3.083	ns
True-Differential	None	3.028	ns
SSTL2 (MSIOD I/O Bank)			
Pseudo-Differential	None	2.721	ns
True-Differential	None	2.71	ns

Table 63 • DDR1/SSTL2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	Speed Grade -1					Units
	t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
SSTL2 Class I						
DDRIO I/O Bank						
Single Ended	2.457	2.145	2.137	2.302	2.293	ns
Differential	2.454	2.38	2.375	2.589	2.584	ns
MSIO I/O Bank						
Single Ended	2.283	2.255	2.243	2.286	2.273	ns
Differential	2.434	2.702	2.691	2.39	2.381	ns
MSIOD I/O Bank						
Single Ended	1.646	1.59	1.589	1.82	1.818	ns
Differential	1.774	1.93	1.926	2.012	2.007	ns
SSTL2 Class II						
DDRIO I/O Bank						
Single Ended	2.317	2.06	2.053	2.229	2.221	ns
Differential	2.32	2.213	2.21	2.57	2.565	ns

Table 63 • DDR1/SSTL2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$ (continued)

	Speed Grade -1					Units
	t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
MSIO I/O Bank						
Single Ended	2.563	2.208	2.19	2.205	2.187	ns
Differential	2.703	2.566	2.555	2.363	2.353	ns

8.7.4 Stub-Series Terminated Logic 1.8 V (SSTL18)

SSTL18 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR2) standard. IGLOO2 and SmartFusion2 SoC FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

8.7.4.1 Minimum and Maximum Input and Output Levels Specification

Table 64 • DDR2/SSTL18 AC/DC Minimum and Maximum Input and Output Levels Specification

Symbols	Parameters	Conditions	Min	Typ	Max	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.71	1.8	1.89	V	–
VTT	Termination voltage		0.838	0.900	0.964	V	–
VREF	Input reference voltage		0.838	0.900	0.964	V	–
SSTL18 DC Input Voltage Specification							
VIH (DC)	DC input logic High		$V_{REF} + 0.125$	–	1.89	V	–
VIL (DC)	DC input logic Low		–0.3	–	$V_{REF} - 0.125$	V	–
IIH (DC)	Input current High		–	–	10	μA	–
IIL (DC)	Input current Low		–	–	10	μA	–
SSTL18 DC Output Voltage Specification							
SSTL18 Class I (DDR2 Reduced Drive)							
VOH	DC output logic High		$V_{TT} + 0.603$	–	–	V	–
VOL	DC output logic Low		–	–	$V_{TT} - 0.603$	V	–
IOH at VOH	Output minimum source DC current (DDRIO I/O Bank only)		6.0	–	–	mA	–
IOL at VOL	Output minimum sink current (DDRIO I/O Bank only)		–6.0	–	–	mA	–
SSTL18 Class II (DDR2 Full Drive)							
VOH	DC output logic High		$V_{TT} + 0.603$	–	–	V	–
VOL	DC output logic Low		–	–	$V_{TT} - 0.603$	V	–
IOH at VOH	Output minimum source DC current (DDRIO I/O Bank only)		12.0	–	–	mA	–
Note: *To meet JEDEC Electrical Compliance, use DDR2 Full Drive Transmitter.							*

8.7.4.2. AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 66 • DDR2/SSTL18 AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.71\text{ V}$

	On-Die Termination (ODT)	Speed Grade -1	Units
		t _{PY}	
SSTL18 (for DDRIO I/O Bank with Fixed Codes)			
Pseudo differential	None	1.633	ns
True differential	None	1.65	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 67 • DDR2/SSTL18 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.71\text{ V}$

	Speed Grade -1					Units
	t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
SSTL18 Class I (for DDRIO I/O Bank)						
Single Ended	2.67	3.078	3.072	2.489	2.484	ns
Differential	2.645	2.431	2.434	2.396	2.398	ns
SSTL18 Class II (for DDRIO I/O Bank)						
Single Ended	2.564	2.973	2.965	2.45	2.444	ns
Differential	2.532	2.401	2.398	2.368	2.365	ns

8.7.5 Stub-Series Terminated Logic 1.5 V (SSTL15)

SSTL15 Class I and Class II are supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR3) standard. IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

8.7.5.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 68 • DDR3 SSTL15 DC Voltage Specification (for DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
VDDI	Supply voltage		1.425	1.5	1.575	V
VTT	Termination voltage		0.698	0.750	0.803	V
VREF	Input reference voltage		0.698	0.750	0.803	V
SSTL15 DC Input Voltage Specification						
VIH(DC)	DC input logic High		$V_{REF} + 0.1$	–	1.575	V
VIL(DC)	DC input logic Low		–0.3	–	$V_{REF} - 0.1$	V
IIH (DC)	Input current High		–	–	10	μA
IIL (DC)	Input current Low		–	–	10	μA

8.8.2 B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

8.8.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 89 • B-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Bus-LVDS Recommended DC Operating Conditions						
VDDI	Supply voltage		2.375	2.5	2.625	V
Bus-LVDS DC Input Voltage Specification						
VI	DC input voltage		0	–	2.925	V
IIH (DC)	Input current High		–	–	10	μA
IIL (DC)	Input current Low		–	–	10	μA
Bus-LVDS DC Output Voltage Specification (for MSIO I/O Bank only)						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
Bus-LVDS Differential Voltage Specification						
VOD	Differential output voltage swing (for MSIO I/O Bank only)		65	–	460	mV
VOCM	Output common mode voltage (for MSIO I/O Bank only)		1.1	–	1.5	V
VICM	Input common mode voltage		0.05	–	2.4	V
VID	Input differential voltage		0.1	–	VDDI	V

Table 90 • B-LVDS AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Bus-LVDS Maximum AC Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	450	Mbps
Bus-LVDS Impedance Specifications						
Rt	Termination resistance		–	27	–	Ω
Bus-LVDS AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF

8.8.5.2. AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 103 • RSDS AC Switching Characteristics for Receiver (Input Buffers)

Worst-case Military conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	On-Die Termination (ODT)	Speed Grade -1	Units
		t_{PY}	
RSDS (for MSIO I/O Bank)	None	3.112	ns
	100	3.108	ns
RSDS (for MSIOD I/O Bank)	None	2.832	ns
	100	2.821	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 104 • RSDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-case Military conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	Speed Grade -1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
RSDS (for MSIO I/O Bank)	2.256	2.484	2.472	2.111	2.096	ns
RSDS (for MSIOD I/O Bank)						
No pre-emphasis	1.661	1.648	1.645	1.675	1.665	ns
Min pre-emphasis	1.651	1.84	1.833	1.988	1.964	ns
Med pre-emphasis	1.577	1.868	1.859	2.019	1.993	ns
Max pre-emphasis	1.555	1.894	1.883	2.047	2.018	ns

8.8.6 LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO2 and SmartFusion2 SoC FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

8.8.6.1 Minimum and Maximum Input and Output Levels

Table 105 • LVPECL DC Voltage Specification (Applicable to MSIO I/O Banks Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
VDDI	Supply voltage		3.15	3.3	3.45	V
LVPECL DC Input Voltage Specification						
VI	DC input voltage		0	—	3.45	V
LVPECL Differential Voltage Specification						
VICM	Input common mode voltage		0.3		2.8	V
VIDIFF	Input differential voltage		100	300	1,000	mV

Table 121 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4Kx4
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade –1		
		Min	Max	Units
trdesu	Read Enable Setup Time	0.532	–	ns
trdehd	Read Enable Hold Time	0.073	–	ns
trdple su	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
trdplehd	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
tr2q	Asynchronous Reset to Output Propagation Delay	–	1.562	ns
trstrem	Asynchronous Reset Removal Time	0.522	–	ns
trstrec	Asynchronous Reset Recovery Time	0.005	–	ns
trstmpw	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
tplrstrem	Pipelined Register Asynchronous Reset Removal Time	-0.288	–	ns
tplrstrec	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
tplrstmpw	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
tsrst su	Synchronous Reset Setup Time	0.233	–	ns
tsrsthd	Synchronous Reset Hold Time	0.037	–	ns
twesu	Write Enable Setup Time	0.473	–	ns
twehd	Write Enable Hold Time	0.05	–	ns
Fmax	Maximum Frequency	–	300	MHz

Table 122 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8Kx2
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tcy	Clock Period	3.333	–	ns
tclkmpwh	Clock Minimum Pulse Width High	1.5	–	ns
tclkmpwl	Clock Minimum pulse Width Low	1.5	–	ns
tpcy	Pipelined Clock Period	3.333	–	ns
tpclkmpwh	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
tpclkmpwl	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.332	ns
	Read Access Time without Pipeline Register	–	2.346	ns
	Access Time with Feed-Through Write Timing	–	1.56	ns
taddr su	Address Setup Time	0.631	–	ns
taddrhd	Address Hold Time	0.282	–	ns

Table 124 • RAM1K18 – Two-Port Mode for Depth × Width Configuration 512x36
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
twehd	Write Enable Hold Time	0.25	–	ns
Fmax	Maximum Frequency	–	300	MHz

11.2 FPGA Fabric Micro SRAM (uSRAM)

Table 125 • uSRAM (RAM64x18) in 64x18 Mode
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade –1		Units
		Min	Max	
tcy	Read Clock Period	4	–	ns
tclkmpwh	Read Clock Minimum Pulse Width High	1.8	–	ns
tclkmpwl	Read Clock Minimum pulse Width Low	1.8	–	ns
tpcy	Read Pipe-line clock period	4	–	ns
tpclkmpwh	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
tpclkmpwl	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.738	ns
taddrsu	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	1.916	–	ns
taddrhd	Read Address Hold Time in Synchronous Mode	0.094	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.803	–	ns
trdensu	Read Enable Setup Time	0.287	–	ns
trdenhd	Read Enable Hold Time	0.059	–	ns
tblksu	Read Block Select Setup Time	1.898	–	ns
tblkhd	Read Block Select Hold Time	-0.671	–	ns
tblk2q	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.102	ns
trstrem	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
trstrec	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
tr2q	Read Asynchronous Reset to Output Propagation Delay (with Pipe-Line Register Enabled)	–	0.869	ns

Table 126 • uSRAM (RAM64x16) in 64x16 Mode
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
trdenhd	Read Enable Hold Time	0.059	–	ns
tblksu	Read Block Select Setup Time	1.898	–	ns
tblkhd	Read Block Select Hold Time	-0.671	–	ns
tblk2q	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.102	ns
trstrem	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
trstrec	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
tr2q	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.866	ns
tsrstsu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.062		ns
tccy	Write Clock Period	4	–	ns
tcclkmpwh	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclkmpwl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblkcsu	Write Block Setup Time	0.417	–	ns
tblkchd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.119	–	ns
tdinchd	Write Input Data hold Time	0.155	–	ns
taddrcsu	Write Address Setup Time	0.091	–	ns
taddrchd	Write Address Hold Time	0.132	–	ns
twecsu	Write Enable Setup Time	0.41	–	ns
twechd	Write Enable Hold Time	-0.027	–	ns
fmax	Maximum Frequency	–	250	MHz

Table 127 • uSRAM (RAM128x9) in 128x9 Mode
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
tcy	Read Clock Period	4	–	ns
tcclkmpwh	Read Clock Minimum Pulse Width High	1.8	–	ns

Table 127 • uSRAM (RAM128x9) in 128x9 Mode
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
tclcmpwl	Read Clock Minimum pulse Width Low	1.8	–	ns
tplcy	Read Pipe-line clock period	4	–	ns
tplclkmpwh	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
tplclkmpwl	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.776	ns
taddrsu	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	1.959	–	ns
taddrhd	Read Address Hold Time in Synchronous Mode	0.125	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.704	–	ns
trdensu	Read Enable Setup Time	0.287	–	ns
trdenhd	Read Enable Hold Time	0.059	–	ns
tblksu	Read Block Select Setup Time	1.898	–	ns
tblkhd	Read Block Select Hold Time	-0.671	–	ns
tblk2q	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.14	ns
trstrem	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
trstrec	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
tr2q	Read Asynchronous Reset to Output Propagation Delay (with Pipe-Line Register Enabled)	–	0.865	ns
tsrstsu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.062	–	ns
tccy	Write Clock Period	4	–	ns
tcclcmpwh	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclcmpwl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblksu	Write Block Setup Time	0.417	–	ns
tblkchd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.104	–	ns
tdinchd	Write Input Data hold Time	0.142	–	ns
taddrcsu	Write Address Setup Time	0.091	–	ns

Table 130 • uSRAM (RAM512x2) in 512x2 Mode
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
tclcmpwl	Read Clock Minimum pulse Width Low	1.8	–	ns
tplcy	Read Pipe-line clock period	4	–	ns
tplclkmpwh	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
tplclkmpwl	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.824	ns
taddrsu	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	2.023	–	ns
taddrhd	Read Address Hold Time in Synchronous Mode	0.141	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.599	–	ns
trdensu	Read Enable Setup Time	0.287	–	ns
trdenhd	Read Enable Hold Time	0.059	–	ns
tblksu	Read Block Select Setup Time	1.898	–	ns
tblkhd	Read Block Select Hold Time	-0.671	–	ns
tblk2q	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.219	ns
trstrem	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
trstrec	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
tr2q	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.862	ns
tsrstsu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.062	–	ns
tccy	Write Clock Period	4	–	ns
tcclcmpwh	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclcmpwl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblkcsu	Write Block Setup Time	0.417	–	ns
tblkchd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.104	–	ns
tdinchd	Write Input Data hold Time	0.142	–	ns
taddrcsu	Write Address Setup Time	0.091	–	ns

18. System Controller SPI Characteristics

Table 143 • System Controller SPI Characteristics
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Symbol	Description	Conditions	All Devices/Speed Grades			Units	Notes
			Min	Typ	Max		
sp1	SC_SPI_SCK minimum period	–	20	–	–	ns	–
sp2	SC_SPI_SCK minimum pulse width high	–	10	–	–	ns	–
sp3	SC_SPI_SCK minimum pulse width low	–	10	–	–	ns	–
sp4	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS rise time (10%-90%) 1	I/O Configuration: LVTTTL 3.3V- 20mA AC Loading: 35pF Test Conditions: Typical Voltage, 25C	–	1.239	–	ns	*
sp5	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS fall time (10%-90%) 1	I/O Configuration: LVTTTL 3.3V- 20mA AC Loading: 35pF Test Conditions: Typical Voltage, 25C	–	1.245	–	ns	*
sp6	Data from master (SC_SPI_SDO) setup time	–	160	–	–	ns	–
sp7	Data from master (SC_SPI_SDO) hold time	–	160	–	–	ns	–
sp8	SC_SPI_SDI setup time	–	20	–	–	ns	–
sp9	SC_SPI_SDI hold time	–	20	–	–	ns	–
Note: *For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models . Use the supported I/O Configurations for the System Controller SPI in Table 144.							

Table 144 • Supported I/O Configurations for System Controller SPI (for MSIO Bank Only)

Voltage Supply	I/O Drive Configuration	Units
3.3 V	20	mA
2.5 V	16	mA
1.8 V	12	mA
1.5 V	8	mA
1.2 V	4	mA