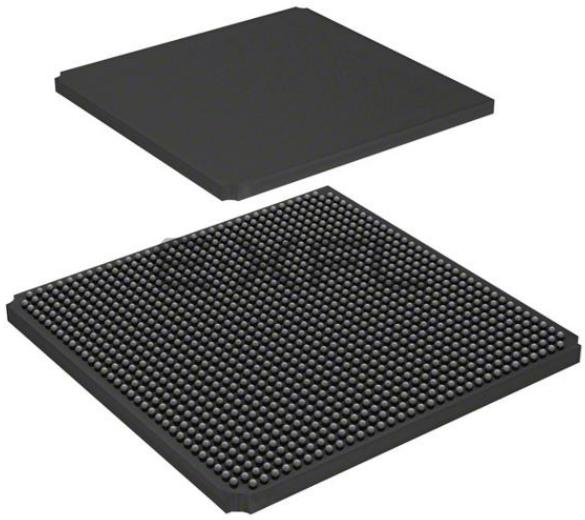

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 150K Logic Modules
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s150t-1fcg1152m

List of Tables

8.6.4.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 38 • LVCMOS 1.8 V AC Switching Characteri stics for Receiver (Input Buffers)
Worst-case Military conditions: T J = 125°C, VDD = 1.14 V, VDDI = 1.71 V

	ODT (On Die Termination)	Speed Grade –1		Units
		t_{PY}	t_{PYS}	
LVCMOS 1.8 V (for DDRIO I/O Bank with Fixed Codes)	None	2.071	2.213	ns
LVCMOS 1.8 V (for MSIO I/O Bank)	None	3.185	3.171	ns
	50	3.394	3.397	ns
	75	3.322	3.316	ns
	150	3.252	3.239	ns
LVCMOS 1.8 V (for MSIOD I/O Bank)	None	2.827	2.813	ns
	50	3.043	3.053	ns
	75	2.968	2.963	ns
	150	2.898	2.886	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 39 • LVCMOS 1.8 V AC Switching Characteristics fo r Transmitter (Output and Tristate Buffers)
Worst-case Military conditions: T J = 125°C, VDD = 1.14 V, VDDI = 1.71 V

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVCMOS 1.8 V (for DDRIO I/ O Bank with Fixed Codes)							
2 mA	slow	4.681	4.017	4.69	5.388	4.852	ns
	medium	4.211	3.599	4.219	5.058	4.488	ns
	medium_fast	3.978	3.392	3.986	4.874	4.327	ns
	fast	3.953	3.373	3.961	4.858	4.316	ns
4 mA	slow	4.355	3.657	4.346	5.967	5.399	ns
	medium	3.886	3.246	3.879	5.628	5.01	ns
	medium_fast	3.656	3.05	3.647	5.461	4.845	ns
	fast	3.635	3.033	3.626	5.447	4.838	ns
6 mA	slow	4.105	3.422	4.092	6.221	5.599	ns
	medium	3.68	3.05	3.668	5.9	5.257	ns
	medium_fast	3.477	2.867	3.463	5.739	5.118	ns
	fast	3.451	2.849	3.437	5.72	5.104	ns
8 mA	slow	4.015	3.32	3.998	6.458	5.808	ns
	medium	3.59	2.947	3.574	6.129	5.449	ns
	medium_fast	3.383	2.761	3.366	5.963	5.304	ns
	fast	3.357	2.746	3.34	5.954	5.289	ns
10 mA	slow	3.888	3.18	3.864	6.739	6.045	ns
	medium	3.485	2.822	3.467	6.422	5.7	ns
	medium_fast	3.281	2.642	3.26	6.277	5.553	ns
	fast	3.258	2.627	3.238	6.27	5.546	ns

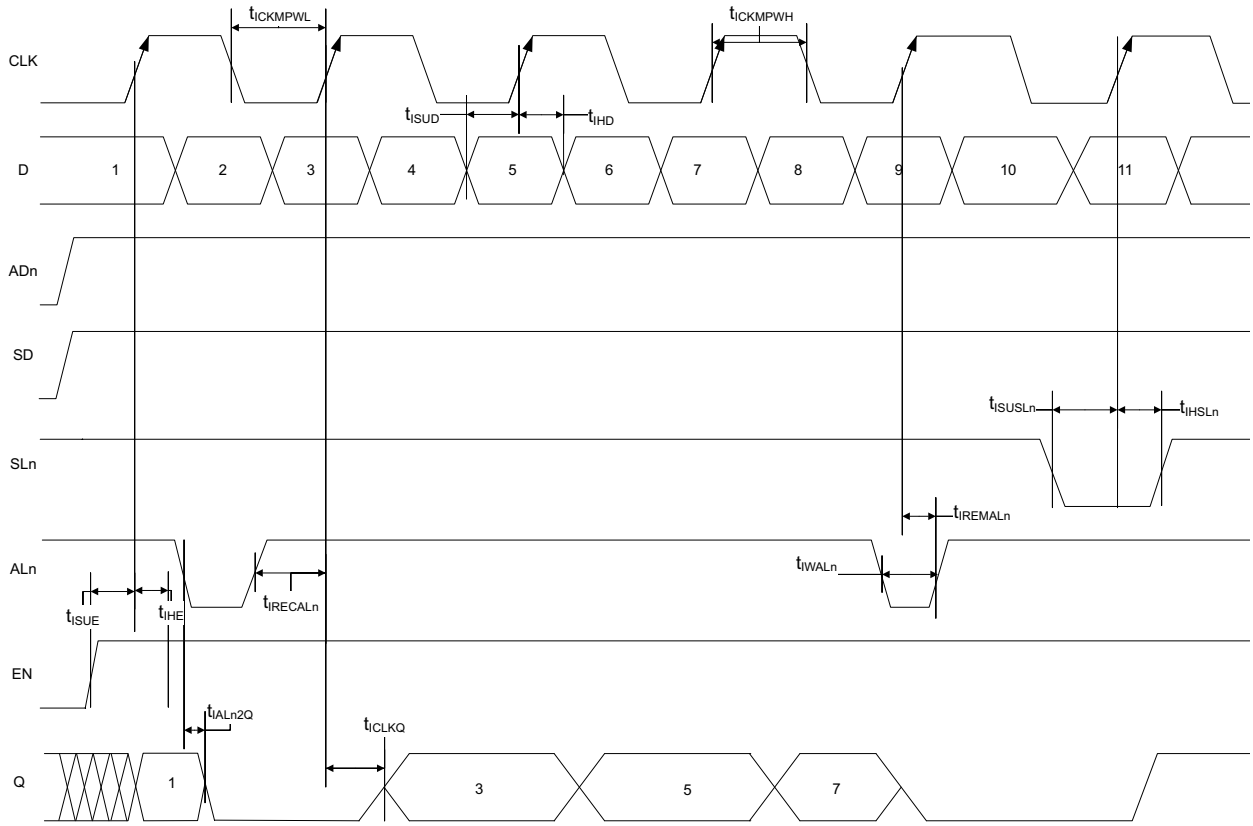

Figure 6 • I/O Register Input Timing Diagram

Table 108 • Input Data Register Propagation Delays
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Measuring Nodes (from, to)*	Speed Grade –1	Units
t_{IBYP}	Bypass Delay of the Input Register	F,G	0.364	ns
t_{ICLKQ}	Clock-to-Q of the Input Register	E,G	0.165	ns
t_{ISUD}	Data Setup Time for the Input Register	A,E	0.369	ns
t_{IHD}	Data Hold Time for the Input Register	A,E	0	ns
t_{ISUE}	Enable Setup Time for the Input Register	B,E	0.475	ns
t_{IHE}	Enable Hold Time for the Input Register	B,E	0	ns
t_{ISUSL}	Synchronous Load Setup Time for the Input Register	D,E	0.475	ns
t_{IHSL}	Synchronous Load Hold Time for the Input Register	D,E	0	ns
t_{IALn2Q}	Asynchronous Clear-to-Q of the Input Register (ADn=1)	C,G	0.648	ns
	Asynchronous Preset-to-Q of the Input Register (ADn=0)	C,G	0.606	ns

Table 140 • IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Conditions/Package Combinations					Units	Notes
CCC Output Peak-to-Peak Period Jitter fOUT_CCC							
010, 050 FG484 Packages	SSO = 0	0 < SSO <= 2	SSO <= 4	SSO <= 8	SSO <= 16		*
20 MHz to 100 MHz	Max(110, – 1% x (1/fOUT_CCC))	Max(150, – 1% x (1/fOUT_CCC))				ps	
100 MHz to 400 MHz	120	150			170	ps	
025 FG484 Package	0 < SSO <=16						*
20 MHz to 74 MHz	– 1% x (1/fOUT_CCC)					ps	
74 MHz to 400 MHz	210					ps	
090 FG484 and 150 FC1152 Packages	0 < SSO <=16						*
20 MHz to 100 MHz	– 1% x (1/fOUT_CCC)					ps	
100 MHz to 400 MHz	150					ps	
Note: *SSO Data is based on LVCMOS 2.5 V MSIO and/or MSIOD Bank I/Os.							

16. JTAG

Table 141 • JTAG 1532
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	-1 Speed Grade					Units
		010	025	050	090	150	
tTCK2Q	Clock to Q (data out)	7.91	7.95	8.15	9.21	8.85	ns
tRSTB2Q	Reset to Q (data out)	6.54	6.27	7.54	7.94	8.99	ns
tDISU	Test Data Input Setup Time	-0.70	-0.70	-0.31	-1.33	-1.02	ns
tDIHD	Test Data Input Hold Time	2.38	2.47	2.13	2.71	2.59	ns
tTMSSU	Test Mode Select Setup Time	-0.86	-1.13	0.26	-1.03	-0.56	ns
tTMDHD	Test Mode Select Hold Time	1.48	1.98	0.21	1.69	1.05	ns
tTRSTREM	ResetB Removal Time	-1.1	-1.38	-0.49	-0.8	-1.07	ns
tTRSTREC	ResetB Recovery Time	-1.1	-1.38	-0.47	-0.8	-1.07	ns
FTCKMAX	TCK Maximum frequency	25	25	25	25	25	MHz

Table 164 SPI Characteristics
Worst-Case Military Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Symbol	Description	Conditions	All Devices/Speed Grades			Unit	Notes
			Min	Typ	Max		
sp9s	SPI_[0|1]_DI hold time	–	3	–	–	ns	2

Notes:
1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models.
2. For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.

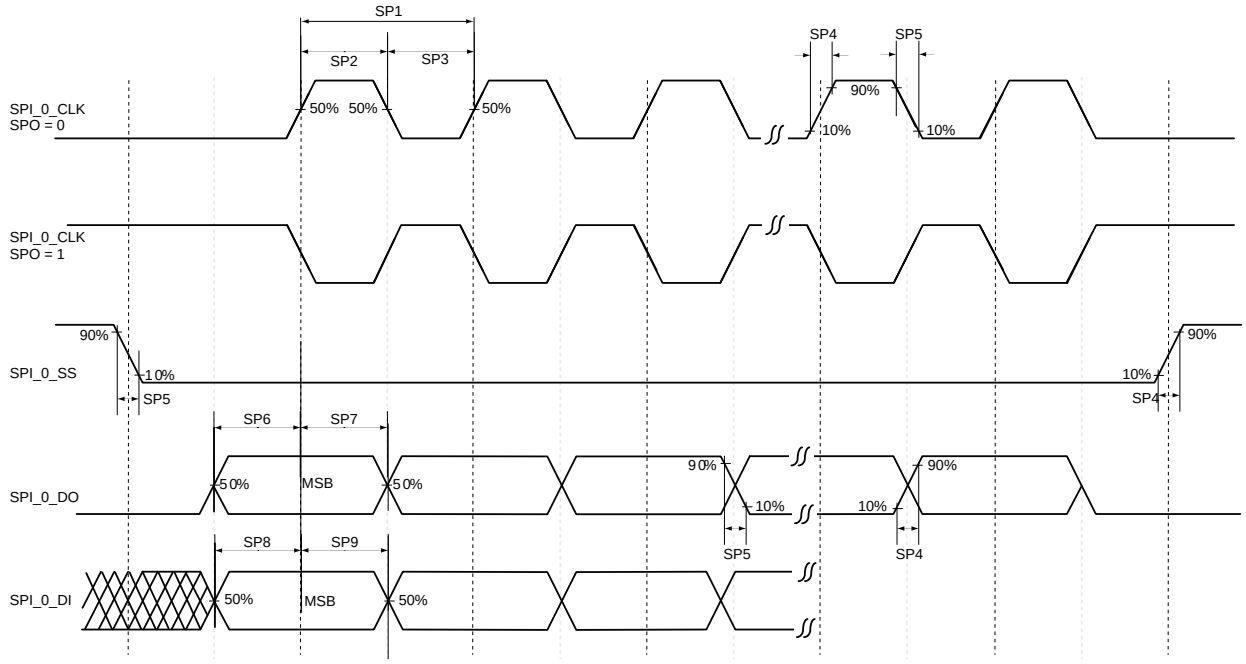

Figure 18 SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)