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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex® -M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I ² C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 150K Logic Modules
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s150ts-1fc1152m

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Table 10 • SmartFusion2 and IGLOO2 Quiescent Supply Current – Worst-Case Process

Parameter	Modes	Conditions	010	025	050	090	150	Units
			VDD=1.26 V	VDD=1.26 V	VDD=1.26 V	VDD=1.26 V	VDD=1.26 V	
IDC1	Non-Flash*Freeze	Military (T _J = 125°C)	151.5	227.4	358.9	443.1	660.4	mA
IDC2	Flash*Freeze	Military (T _J = 125°C)	127.2	144.2	174.6	195.0	236.3	mA

5.2 Programming Currents

The tables below represent programming, verify and Inrush currents for SmartFusion2 SoC and IGLOO2 FPGA devices.

Table 11 • Currents During Program Cycle, 0°C ≤ T_J ≤ 85°C, Typical Process

Power Supplies	Voltage (V)	010	025	050	090	150	Units	Notes
VDD	1.26	53	55	58	42	52	mA	–
VPP	3.46	11	6	10	12	12	mA	–
VPPNVM	3.46	2	2	3	3	–	mA	*
VDDI	2.62	16	17	1	12	81	mA	**
	3.46	31	36	1	17	84	mA	**
Number of banks		8	8	10	9	19	–	–
Notes: * VPP and VPPNVM are internally shorted. ** The current for 050 represents JTAG I/O Bank only.								

Table 12 • Currents During Verify Cycle, 0°C ≤ T_J ≤ 85°C, Typical Process

Power Supplies	Voltage (V)	010	025	050	090	150	Units	Notes
VDD	1.26	53	55	58	41	51	mA	–
VPP	3.46	5	3	15	11	12	mA	–
VPPNVM	3.46	0	0	1	1	–	mA	*
VDDI	2.62	16	17	1	11	81	mA	**
	3.46	32	36	1	17	84	mA	**
Number of banks		8	8	10	9	19	–	–
Notes: * VPP and VPPNVM are internally shorted. ** The current for 050 represents JTAG I/O Bank only.								

Table 13 • Inrush Currents at Power up, –55°C ≤ T_J ≤ 125°C, Typical Process

Power Supplies	Voltage (V)	010	025	050	090	150	Units
VDD	1.26	53	78	57	98	140	mA
VPP	3.46	57	50	180	36	51	mA

Table 15 • Timing Model Parameters (continued)

Index	Parameter	Description	Speed Grade -1	Units	Notes
O	t_{DP}	Propagation Delay of SSTL2, Class I Transmitter on the MSIO Bank	2.283	ns	Refer to page 47 for more information
P	t_{DP}	Propagation Delay of LVCMOS 1.5 V Transmitter, Drive strength of 12mA, fast slew on the DDRIO Bank	3.703	ns	Refer to page 38 for more information

8. User I/O Characteristics

There are three types of I/Os supported in the IGLOO2 FPGA and SmartFusion2 SoC FPGA families: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the “I/Os” section of the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

8.1 Input Buffer and AC Loading

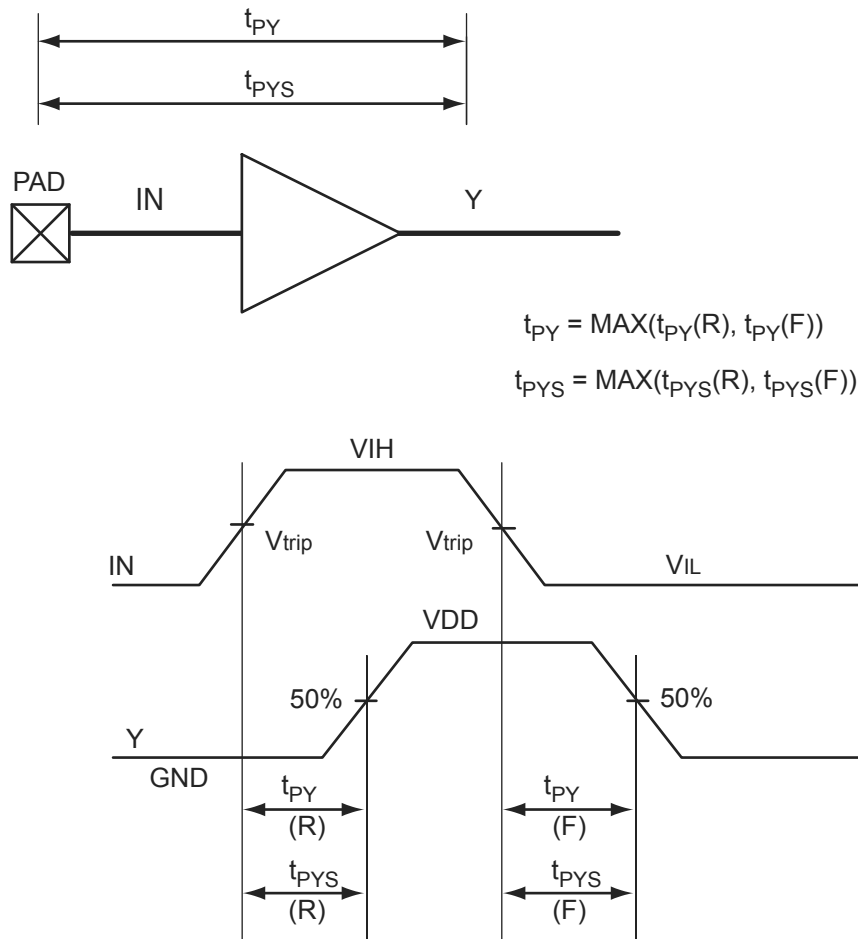


Figure 2 • Input Buffer AC Loading

8.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

8.6.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 21 • LVTTL/LVCMOS 3.3 V DC Voltage Specification (Applicable to MSIO I/O Bank Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units	Notes
LVTTL/LVCMOS 3.3 V Recommended DC Operating Conditions							
VDDI	Supply voltage		3.15	3.3	3.45	V	–
LVTTL/LVCMOS 3.3 V DC Input Voltage Specification							
VIH (DC)	DC input logic High		2.0	–	3.45	V	–
VIL (DC)	DC input logic Low		–0.3	–	0.8	V	–
IIH (DC)	Input current High		–	–	10	μA	–
IIL (DC)	Input current Low		–	–	10	μA	–
LVCMOS 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		2.4	–	–	V	*
VOL	DC output logic Low		–	–	0.4	V	*
LVTTL 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		2.4	–	–	V	–
VOL	DC output logic Low		–	–	0.4	V	–
Note: * The VOH/VOL test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.							

Table 22 • LVTTL/LVCMOS 3.3 V Maximum Switching Speeds (Applicable to MSIO I/O Bank Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
LVTTL/LVCMOS 3.3 V Maximum Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	540	Mbps

Table 23 • LVTTL/LVCMOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO Bank Only)

LVTTL/LVCMOS 3.3 V AC Test Parameter Specifications						
Symbol	Parameters	Conditions	Min	Typ	Max	Units
Vtrip	Measuring/trip point for data path		–	1.4	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

8.7.3.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 62 • DDR1/SSTL2 AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	ODT (On Die Termination)	Speed Grade –1	Units
		t _{PY}	
SSTL2 (DDRIO I/O Bank)			
Pseudo-Differential	None	1.613	ns
True-Differential	None	1.647	ns
SSTL2 (MSIO I/O Bank)			
Pseudo-Differential	None	3.083	ns
True-Differential	None	3.028	ns
SSTL2 (MSIOD I/O Bank)			
Pseudo-Differential	None	2.721	ns
True-Differential	None	2.71	ns

Table 63 • DDR1/SSTL2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	Speed Grade -1					Units
	t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
SSTL2 Class I						
DDRIO I/O Bank						
Single Ended	2.457	2.145	2.137	2.302	2.293	ns
Differential	2.454	2.38	2.375	2.589	2.584	ns
MSIO I/O Bank						
Single Ended	2.283	2.255	2.243	2.286	2.273	ns
Differential	2.434	2.702	2.691	2.39	2.381	ns
MSIOD I/O Bank						
Single Ended	1.646	1.59	1.589	1.82	1.818	ns
Differential	1.774	1.93	1.926	2.012	2.007	ns
SSTL2 Class II						
DDRIO I/O Bank						
Single Ended	2.317	2.06	2.053	2.229	2.221	ns
Differential	2.32	2.213	2.21	2.57	2.565	ns

Table 63 • DDR1/SSTL2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$ (continued)

	Speed Grade -1					Units
	t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
MSIO I/O Bank						
Single Ended	2.563	2.208	2.19	2.205	2.187	ns
Differential	2.703	2.566	2.555	2.363	2.353	ns

8.7.4 Stub-Series Terminated Logic 1.8 V (SSTL18)

SSTL18 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR2) standard. IGLOO2 and SmartFusion2 SoC FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

8.7.4.1 Minimum and Maximum Input and Output Levels Specification

Table 64 • DDR2/SSTL18 AC/DC Minimum and Maximum Input and Output Levels Specification

Symbols	Parameters	Conditions	Min	Typ	Max	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.71	1.8	1.89	V	–
VTT	Termination voltage		0.838	0.900	0.964	V	–
VREF	Input reference voltage		0.838	0.900	0.964	V	–
SSTL18 DC Input Voltage Specification							
VIH (DC)	DC input logic High		$V_{REF} + 0.125$	–	1.89	V	–
VIL (DC)	DC input logic Low		–0.3	–	$V_{REF} - 0.125$	V	–
IIH (DC)	Input current High		–	–	10	μA	–
IIL (DC)	Input current Low		–	–	10	μA	–
SSTL18 DC Output Voltage Specification							
SSTL18 Class I (DDR2 Reduced Drive)							
VOH	DC output logic High		$V_{TT} + 0.603$	–	–	V	–
VOL	DC output logic Low		–	–	$V_{TT} - 0.603$	V	–
IOH at VOH	Output minimum source DC current (DDRIO I/O Bank only)		6.0	–	–	mA	–
IOL at VOL	Output minimum sink current (DDRIO I/O Bank only)		–6.0	–	–	mA	–
SSTL18 Class II (DDR2 Full Drive)							
VOH	DC output logic High		$V_{TT} + 0.603$	–	–	V	–
VOL	DC output logic Low		–	–	$V_{TT} - 0.603$	V	–
IOH at VOH	Output minimum source DC current (DDRIO I/O Bank only)		12.0	–	–	mA	–
Note: *To meet JEDEC Electrical Compliance, use DDR2 Full Drive Transmitter.							*

Table 72 • LPDDR AC/DC Specifications (for DDRIO IO Bank Only)

LPDDR Reduced Drive						
VOH	DC output logic High	$0.9 \times V_{DDI}$	–	–	V	–
VOL	DC output logic Low	–	–	$0.1 \times V_{DDI}$	V	–
IOH at VOH	Output minimum source DC current	0.1	–	–	mA	–
IOL at VOL	Output minimum sink current	–0.1	–	–	mA	–
LPDDR Full Drive						*
VOH	DC output logic High	$0.9 \times V_{DDI}$	–	–	V	–
VOL	DC output logic Low	–	–	$0.1 \times V_{DDI}$	V	–
IOH at VOH	Output minimum source DC current	0.1	–	–	mA	–
IOL at VOL	Output minimum sink current	–0.1	–	–	mA	–
LPDDR DC Differential Voltage Specification						
VID (DC)	DC input differential voltage	$0.4 \times V_{DDI}$	–	–	V	–
Note: *To meet JEDEC Electrical Compliance, use LPDDR Full Drive Transmitter.						

Table 73 • LPDDR Maximum AC Switching Speeds (for DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Dmax	Maximum data rate	AC loading: per JEDEC specifications	–	–	360	Mbps

Table 74 • LPDDR AC Specifications (for DDRIO IO Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LPDDR AC Differential Voltage Specification						
VDIFF (AC)	AC Input differential voltage	–	$0.6 \times V_{DDI}$	–	–	V
Vx (AC)	AC Differential Cross Point Voltage	–	$0.4 \times V_{DDI}$	–	$0.6 \times V_{DDI}$	V
LPDDR Impedance Specifications						
Rref	Supported Output Driver Calibrated Impedance	Reference Resistor = 150Ω	–	20,42	–	Ω
RTT	Effective impedance Value - ODT	Reference Resistor = 150Ω	–	50, 75, 150	–	Ω
LPDDR AC Test Parameters Specifications						
Vtrip	Measuring/Trip Point for Data Path	–	–	0.9	–	V
Rent	Resistance for Enable Path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})	–	–	2k	–	Ω
Cent	Capacitive Loading for Enable Path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})	–	–	5	–	pF
Rtt_test	Reference resistance for Data Test Path for LPDDR (t_{DP})	–	–	50	–	Ω
Cload	Capacitive Loading for Data Path (t_{DP})	–	–	5	–	pF

8.8.1.2 LVDS25 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 85 • LVDS25 Receiver Characteristics

Worst-Case Military Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	On-Die Termination (ODT)	Speed Grade -1	Units
		t_{PY}	
LVDS (for MSIO I/O Bank)	None	3.061	ns
	100	3.057	ns
LVDS (for MSIOD I/O Bank)	None	2.792	ns
	100	2.787	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 86 • LVDS25 Transmitter Characteristics

Worst-Case Military Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	Speed Grade -1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVDS (for MSIO I/O Bank)	2.299	2.602	2.589	2.305	2.32	ns
LVDS (for MSIOD I/O Bank)						
No pre-emphasis	1.656	1.845	1.838	1.992	1.969	ns
Min pre-emphasis	1.583	1.868	1.866	2.018	1.998	ns
Med pre-emphasis	1.559	1.893	1.886	2.045	2.021	ns

8.8.1.3 LVDS33 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 87 • LVDS33 Receiver Characteristics

Worst-Case Military Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 3.15\text{ V}$

	On Die Termination (ODT)	Speed Grade -1	Units
		t_{PY}	
LVDS33 (for MSIO I/O Bank)	None	2.763	ns
	100	2.76	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 88 • LVDS33 Transmitter Characteristics

Worst-Case Military Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 3.15\text{ V}$

	Speed Grade -1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVDS33 (for MSIO I/O Bank)	2.069	2.112	2.106	2.078	2.09	ns

8.8.2 B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

8.8.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 89 • B-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Bus-LVDS Recommended DC Operating Conditions						
VDDI	Supply voltage		2.375	2.5	2.625	V
Bus-LVDS DC Input Voltage Specification						
VI	DC input voltage		0	–	2.925	V
IIH (DC)	Input current High		–	–	10	μA
IIL (DC)	Input current Low		–	–	10	μA
Bus-LVDS DC Output Voltage Specification (for MSIO I/O Bank only)						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
Bus-LVDS Differential Voltage Specification						
VOD	Differential output voltage swing (for MSIO I/O Bank only)		65	–	460	mV
VOCM	Output common mode voltage (for MSIO I/O Bank only)		1.1	–	1.5	V
VICM	Input common mode voltage		0.05	–	2.4	V
VID	Input differential voltage		0.1	–	VDDI	V

Table 90 • B-LVDS AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Bus-LVDS Maximum AC Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	450	Mbps
Bus-LVDS Impedance Specifications						
Rt	Termination resistance		–	27	–	Ω
Bus-LVDS AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF

Table 93 • M-LVDS DC Voltage Specification (continued)

Symbols	Parameters	Conditions	Min	Typ	Max	Units	Notes
VID	Input differential voltage		50	–	2400	mV	–
Note: *Only M-LVDS TYPE I is supported							

Table 94 • M-LVDS AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
M-LVDS Maximum AC Switching Speeds						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	450	Mbps
M-LVDS Impedance Specification						
Rt	Termination resistance	–	–	50	–	Ω
M-LVDS AC Test Parameters Specifications						
VTrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF

8.8.3.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 95 • M-LVDS AC Switching Characteristics for Receiver (Input Buffers)

Worst-case Military conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	On-Die Termination (ODT)	Speed Grade –1	Units
		t_{PY}	
M-LVDS (for MSIO I/O Bank)	None	3.011	ns
	100	3.006	ns
M-LVDS (for MSIOD I/O Bank)	None	2.722	ns
	100	2.725	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 96 • M-LVDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-case Military conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
M-LVDS (for MSIO I/O Bank)	2.78	2.632	2.616	2.447	2.436	ns

Table 106 • LVPECL Maximum AC Switching Speeds (Applicable to MSIO I/O Banks Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVPECL AC Specifications						
Fmax	Maximum data rate (for MSIO I/O Bank)		–	–	810	Mbps

8.8.6.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 107 • LVPECL Receiver Characteristics

Worst-case Military conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 3.15\text{ V}$

	On-Die Termination (ODT)	t _{py}	Units
		Speed Grade –1	
LVPECL (for MSIO I/O Bank)	None	2.71	ns
	100	2.71	ns

8.9 I/O Register Specifications

8.9.1 Input Register

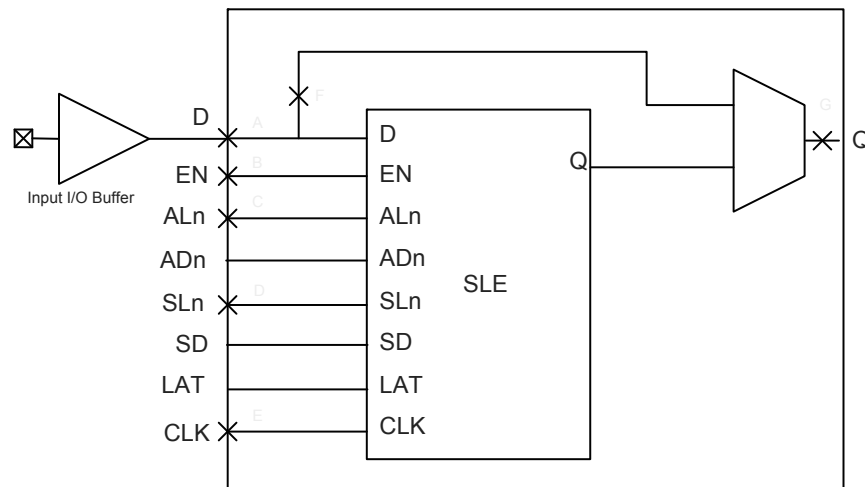


Figure 5 • Timing Model for Input Register

Table 108 • Input Data Register Propagation Delays (continued)
Worst-Case Military Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Measuring Nodes (from, to)*	Speed Grade -1	Units
$t_{IREMALn}$	Asynchronous Load Removal Time for the Input Register	C,E	0	ns
$t_{IRECALn}$	Asynchronous Load Recovery Time for the Input Register	C,E	0.076	ns
t_{IWALn}	Asynchronous Load Minimum Pulse Width for the Input Register	C,C	0.313	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Input Register	E,E	0.078	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Input Register	E,E	0.164	ns

8.9.2 Output/Enable Register

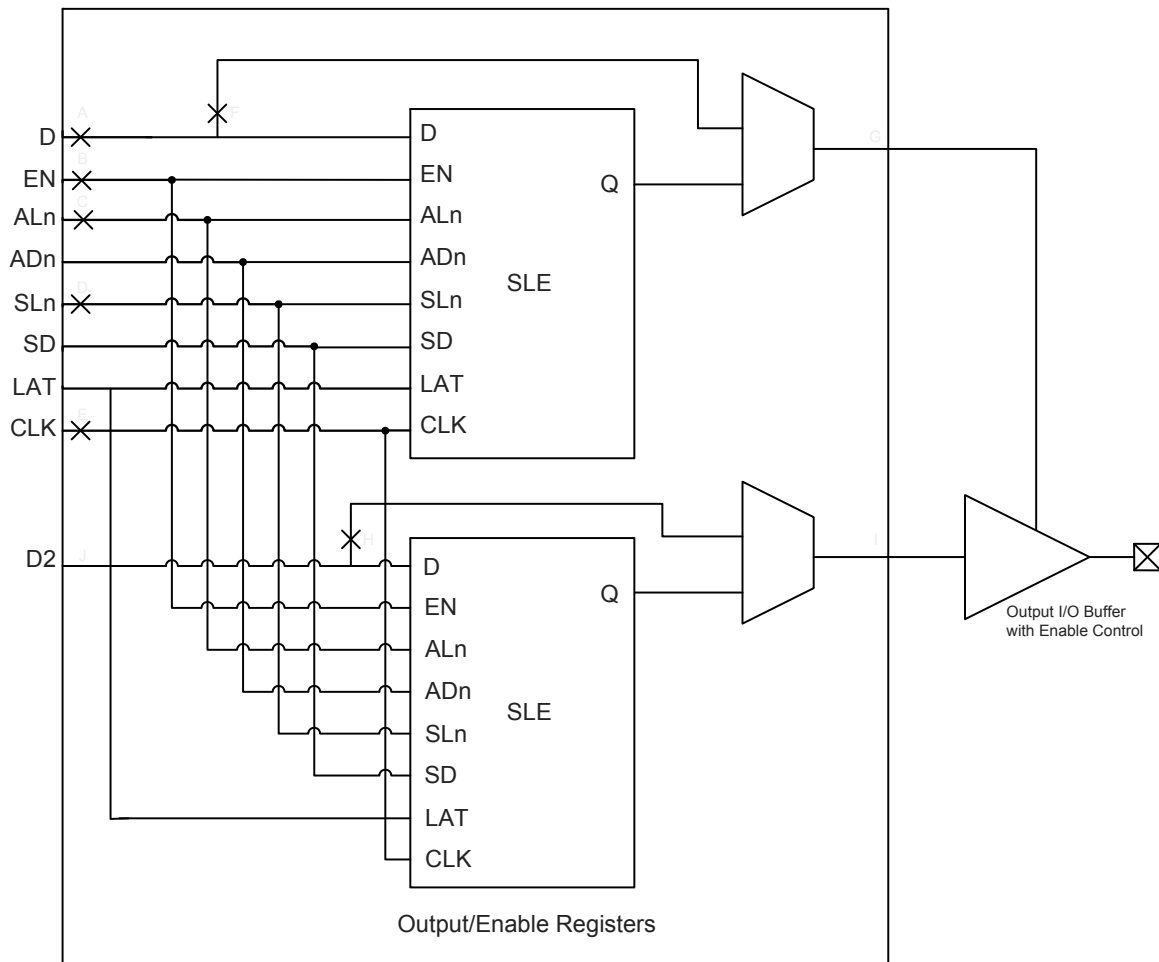


Figure 7 • Timing Model for Output/Enable Register

8.10.3 Timing Characteristics

Table 110 • Input DDR Propagation Delays
Worst-Case Military Conditions: $T_j = 125^{\circ}\text{C}$, $V_{DD}=1.14\text{ V}$

Parameter	Description	Measuring Nodes (from, to)	Speed Grade –1	Units
tDDRICKQ1	Clock-to-Out Out_QR for Input DDR	B,C	0.165	ns
tDDRICKQ2	Clock-to-Out Out_QF for Input DDR	B,D	0.172	ns
tDDRISUD	Data Setup for Input DDR	A,B	0.372	ns
tDDRILD	Data Hold for Input DDR	A,B	0	ns
tDDRISUE	Enable Setup for Input DDR	E,B	0.475	ns
tDDRILHE	Enable Hold for Input DDR	E,B	0	ns
tDDRISUSLn	Synchronous Load Setup for Input DDR	G,B	0.475	ns
tDDRILSLn	Synchronous Load Hold for Input DDR	G,B	0	ns
tDDRIAL2Q1	Asynchronous Load-to-Out QR for Input DDR	F,C	0.606	ns
tDDRIAL2Q2	Asynchronous Load-to-Out QF for Input DDR	F,D	0.558	ns
tDDRIREMAL	Asynchronous Load Removal time for Input DDR	F,B	0	ns
tDDRIRECAL	Asynchronous Load Recovery time for Input DDR	F,B	0.076	ns
tDDRILWAL	Asynchronous Load Minimum Pulse Width for Input DDR	F,F	0.313	ns
tDDRICKMPWH	Clock Minimum Pulse Width High for Input DDR	B,B	0.078	ns
tDDRICKMPWL	Clock Minimum Pulse Width Low for Input DDR	B,B	0.164	ns

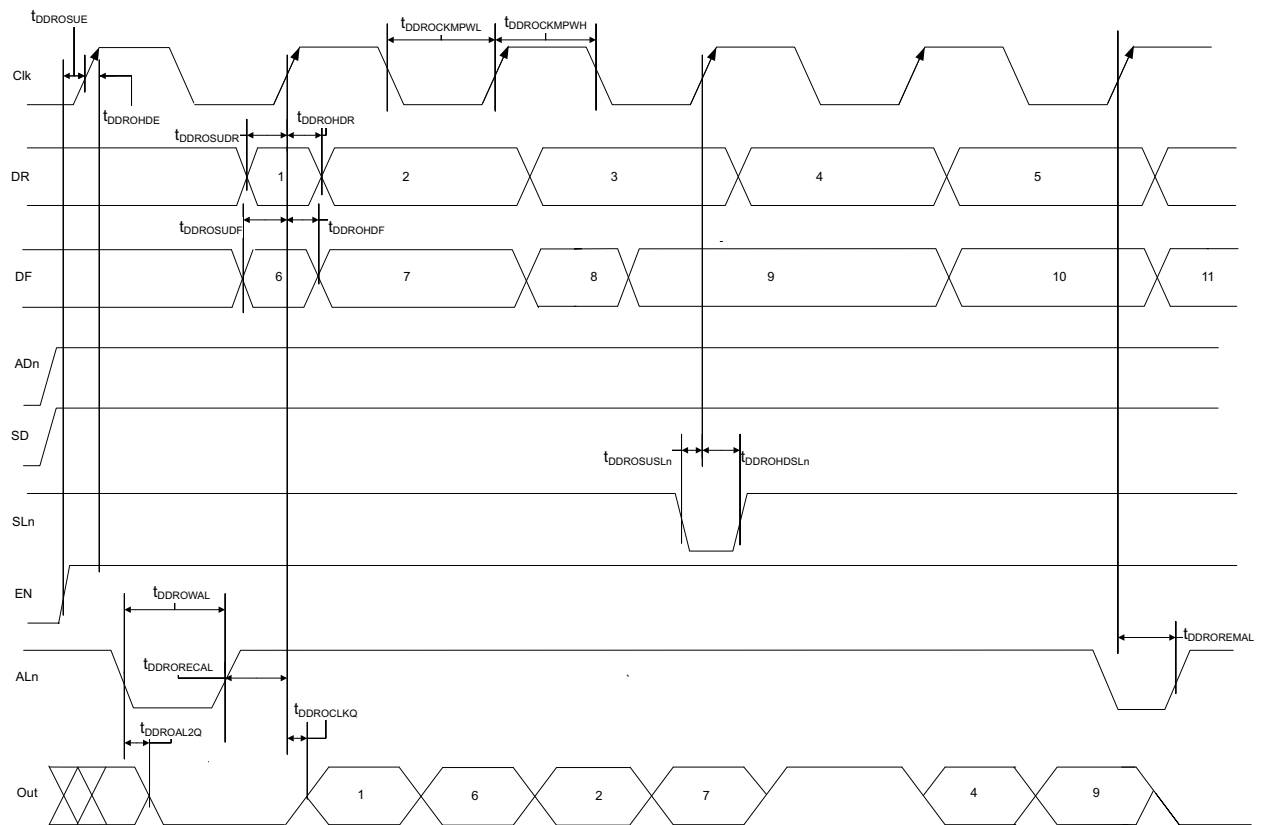


Figure 12 • Output DDR Timing Diagram

8.10.5 Timing Characteristics

Table 111 • Output DDR Propagation Delays
Worst-Case Military Conditions: $T_j = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Measuring Nodes (from, to)	Speed Grade –1	Units
tDDROCLKQ	Clock-to-Out of DDR for Output DDR	E,G	0.272	ns
tDDROSUDF	DF Data Setup for Output DDR	F,E	0.148	ns
tDDROSUDR	DR Data Setup for Output DDR	A,E	0.196	ns
tDDROHDF	DF Data Hold for Output DDR	F,E	0	ns
tDDROHDR	DR Data Hold for Output DDR	A,E	0	ns
tDDROSUE	Enable Setup for Output DDR	B,E	0.433	ns
tDDROHE	Enable Hold for Output DDR	B,E	0	ns
tDDROSUSLn	Synchronous Load Setup for Output DDR	D,E	0.203	ns
tDDROHSLn	Synchronous Load Hold for Output DDR	D,E	0	ns
tDDROAL2Q	Asynchronous Load-to-Out for Output DDR	C,G	0.545	ns
tDDROREMAI	Asynchronous Load Removal time for Output DDR	C,E	0	ns
tDDRORECAL	Asynchronous Load Recovery time for Output DDR	C,E	0.035	ns
tDDROWAL	Asynchronous Load Minimum Pulse Width for Output DDR	C,C	0.266	ns
tDDROCKMPWH	Clock Minimum Pulse Width High for the Output DDR	E,E	0.065	ns
tDDROCKMPWL	Clock Minimum Pulse Width Low for the Output DDR	E,E	0.139	ns

9. Logic Element Specifications

9.1 4-input LUT (LUT-4)

The IGLOO2 and SmartFusion2 SoC FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *SmartFusion2 and IGLOO2 Macro Library Guide*.

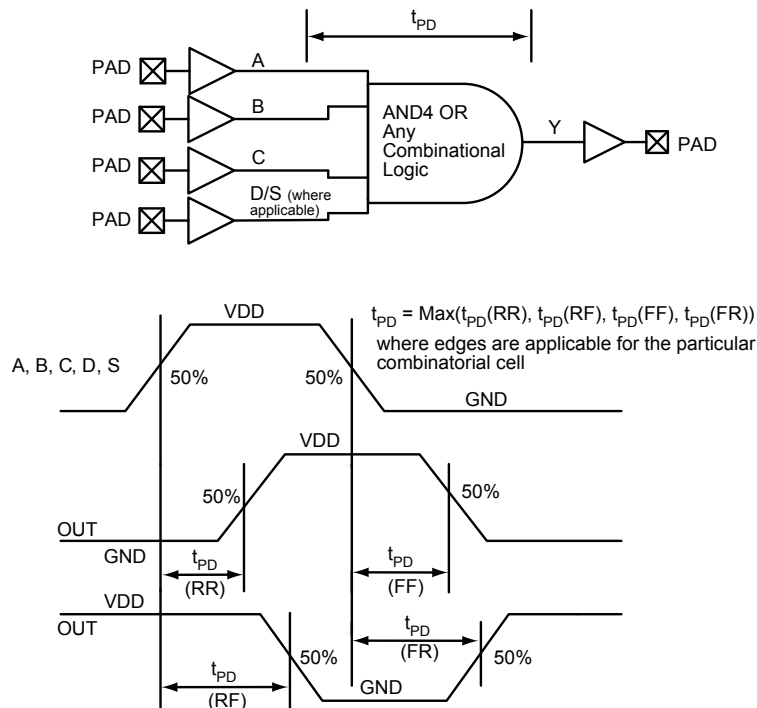


Figure 13 • LUT-4

Timing Characteristics

Table 112 • Combinatorial Cell Propagation Delays

Worst-Case Military Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Combinatorial Cell	Equation	Parameter	Speed Grade -1	Units
INV	$Y = !A$	t_{PD}	0.106	ns
AND2	$Y = A \cdot B$	t_{PD}	0.17	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.157	ns
OR2	$Y = A + B$	t_{PD}	0.17	ns
NOR2	$Y = !(A + B)$	t_{PD}	0.157	ns
XOR2	$Y = A \oplus B$	t_{PD}	0.17	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	0.236	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	0.217	ns
AND4	$Y = A \cdot B \cdot C \cdot D$	t_{PD}	0.384	ns

Table 126 • uSRAM (RAM64x16) in 64x16 Mode
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
trdenhd	Read Enable Hold Time	0.059	–	ns
tblksu	Read Block Select Setup Time	1.898	–	ns
tblkhd	Read Block Select Hold Time	-0.671	–	ns
tblk2q	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.102	ns
trstrem	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
trstrec	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
tr2q	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.866	ns
tsrstsu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.062		ns
tccy	Write Clock Period	4	–	ns
tcclkmpwh	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclkmpwl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblkcsu	Write Block Setup Time	0.417	–	ns
tblkchd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.119	–	ns
tdinchd	Write Input Data hold Time	0.155	–	ns
taddrcsu	Write Address Setup Time	0.091	–	ns
taddrchd	Write Address Hold Time	0.132	–	ns
twecsu	Write Enable Setup Time	0.41	–	ns
twechd	Write Enable Hold Time	-0.027	–	ns
fmax	Maximum Frequency	–	250	MHz

Table 127 • uSRAM (RAM128x9) in 128x9 Mode
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
tcy	Read Clock Period	4	–	ns
tcclkmpwh	Read Clock Minimum Pulse Width High	1.8	–	ns

Table 128 • uSRAM (RAM128x8) in 128x8 Mode
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
tr2q	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.865	ns
tsrstu	Read Synchronous Reset Setup Time	0.279	–	ns
tsrsthd	Read Synchronous Reset Hold Time	0.062	–	ns
tccy	Write Clock Period	4	–	ns
tcclcmpwh	Write Clock Minimum Pulse Width High	1.8	–	ns
tcclcmpwl	Write Clock Minimum Pulse Width Low	1.8	–	ns
tblkcsu	Write Block Setup Time	0.417	–	ns
tblkchd	Write Block Hold Time	0.007	–	ns
tdincsu	Write Input Data setup Time	0.104	–	ns
tdinchd	Write Input Data hold Time	0.142	–	ns
taddrcsu	Write Address Setup Time	0.091	–	ns
taddrchd	Write Address Hold Time	0.24	–	ns
twecsu	Write Enable Setup Time	0.41	–	ns
twechd	Write Enable Hold Time	-0.027	–	ns
fmax	Maximum Frequency	–	250	MHz

Table 129 • uSRAM (RAM256x4) in 256x4 Mode
Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
tcy	Read Clock Period	4	–	ns
tclcmpwh	Read Clock Minimum Pulse Width High	1.8	–	ns
tclcmpwl	Read Clock Minimum pulse Width Low	1.8	–	ns
tpcy	Read Pipe-line clock period	4	–	ns
tpclcmpwh	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
tpclcmpwl	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
tclk2q	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.812	ns
taddrsu	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	1.993	–	ns
taddrhd	Read Address Hold Time in Synchronous Mode	0.125	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.669	–	ns
trdensu	Read Enable Setup Time	0.287	–	ns

Table 147 • Mathblock With Input Register Used and Output in Bypass Mode
 Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Mathblock With Input Register Used and Output in Bypass Mode		Speed Grade -1		Units
Parameter	Description	Min	Max	
TMISU	Input Register Setup time	0.149	–	ns
TMIHD	Input Register Hold time	0.08	–	ns
TMSRSTENSU	Synchronous Reset/Enable Setup time	0.185	–	ns
TMSRSTENHD	Synchronous Reset/Enable Hold time	-0.012	–	ns
TMARSTREM	Asynchronous Reset Removal time	-0.005	–	ns
TMARSTREC	Asynchronous Reset Recovery time	0.088	–	ns
TMICQ	Input Register Clock to Output delay	–	2.52	ns
TMCDIN2Q	CDIN to Output delay	–	1.951	ns

Table 148 • Mathblock With Input and Output in Bypass Mode
 Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Mathblock With Input and Output in Bypass Mode		Speed Grade -1		Units
Parameter	Description	Min	Max	
TMIQ	Input to Output delay	–	2.568	ns
TMCDIN2Q	CDIN to Output delay	–	1.951	ns

20. Flash*Freeze Timing Characteristics

Table 149 • Flash*Freeze Entry and Exit Times
 Military Worst-Case conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Symbols	Parameters	Conditions	Entry/Exit Timing	Units	Notes
TFF_ENTRY	Entry time	eNVM and MSS/HPMS PLL = ON	160	μs	1
		eNVM and MSS/HPMS PLL = OFF	215	μs	1

Table 164 • SPI Characteristics

Worst-Case Military Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Symbol	Description	Conditions	All Devices/Speed Grades			Unit	Notes
			Min	Typ	Max		
sp9s	SPI_[0 1]_DI hold time	—	3	—	—	ns	2

Notes:

- For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website:
<http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models>.
- For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.

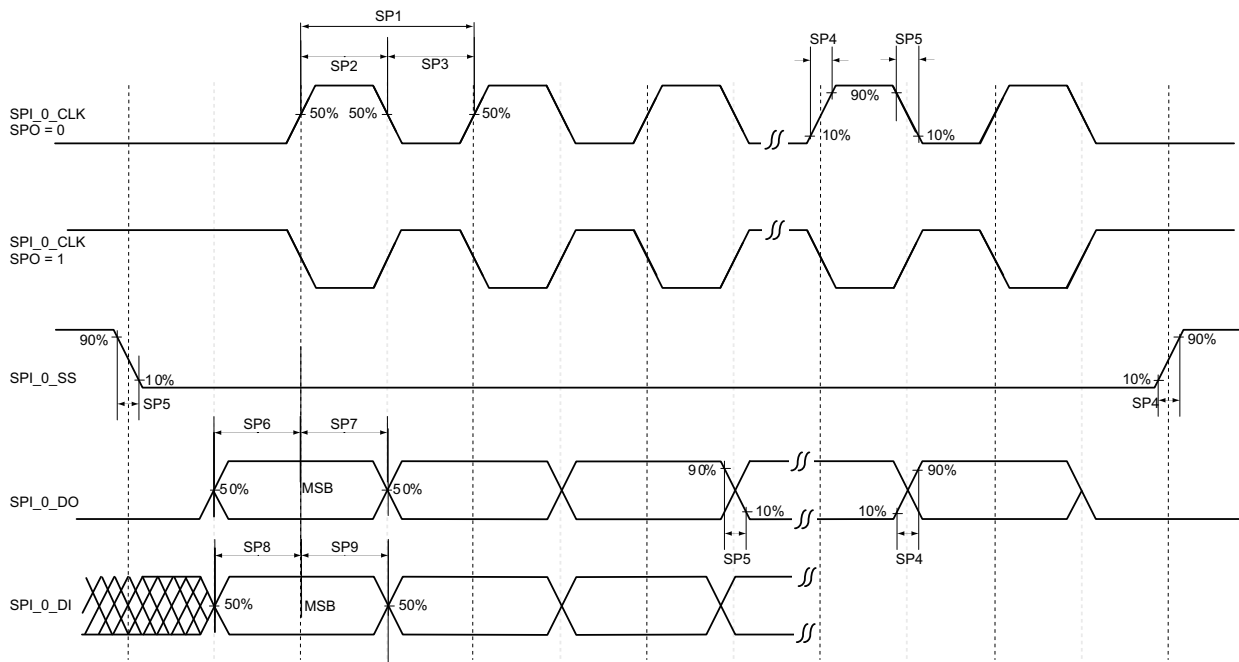


Figure 18 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)