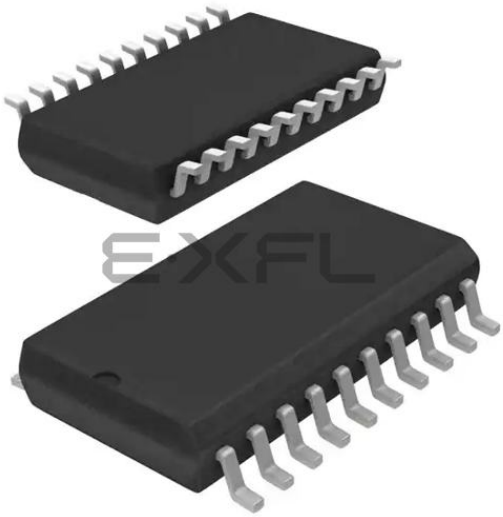

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SAM8RC
Core Size	8-Bit
Speed	12MHz
Connectivity	I²C, UART/USART
Peripherals	LCD, LVD, LVR, PWM, WDT
Number of I/O	22
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	272 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/s3f8s28xzz-sk98

- Timer/Counters
  - One 8-bit basic timer for watchdog function
  - One 16-bit timer(Timer 0) or two 8-bit timers A/B with time interval mode
  - One 16-bit timer/counter (Timer 1) with two operating modes; Interval mode, Capture mode
  - One free running Watchdog Timer with programmable timer-out period. It can be used to generate RESET or release STOP when clocked by Ring Oscillator.

- A/D Converter
  - Thirteen analog input pins (Max.)
  - 12-bit conversion resolution
  - Integrated sample and hold circuitry

- Asynchronous UART
  - Programmable baud rate generator
  - Support serial data transmit/receive operations with 8-bit, 9-bit UART

- Multi-Master IIC-Bus
  - Serial Peripheral Interface
  - Serial, 8-bit Data Transfers
  - Programmable Clock Prescale

- Oscillation Frequency
  - 0.1MHz to 1MHz external low gain (LG) crystal oscillator
  - 0.4MHz to 12MHz external high gain (HG) crystal oscillator
  - Internal RC: 0.5MHz (typ.), 1 MHz (typ.), 2MHz (typ.), 4MHz (typ.), 8MHz (typ.), in VDD = 5V with 1% tolerance
  - On-Chip Ring oscillator with 32kHz frequency for free running Watchdog Timer.
  - Maximum 12MHz CPU clock

- Built-in RESET Circuit (LVR)
  - Low-Voltage check to make system reset
  - V_{LVR} = 1.9/2.3/3.0/3.9V (by Smart Option)

- Low Voltage Detect Circuit (LVD)
  - Programmable detection voltage
  - V_{LVD} = 2.1/2.5/3.2/4.1V
  - En/Disable S/W selectable.

- Operating Temperature Range
  - – 40°C to + 85°C

2.5 System and User Stacks

S3C8 Series microcontrollers use the system stack for subroutine calls and returns and to store data. The PUSH and POP instructions are used to control system stack operations. The S3F8S28/S3F8S24 architecture supports stack operations in the internal register file.

2.5.1 Stack Operations

Return addresses for procedure calls, interrupts and data are stored on the stack. The contents of the PC are saved to stack by a CALL instruction and restored by the RET instruction. When an interrupt occurs, the contents of the PC and the FLAGS registers are pushed to the stack. The IRET instruction then pops these values back to their original locations. The stack address value is always decreased by one before a push operation and increased by one after a pop operation. The stack pointer (SP) always points to the stack frame stored on the top of the stack, as shown in *Figure 2-16*.

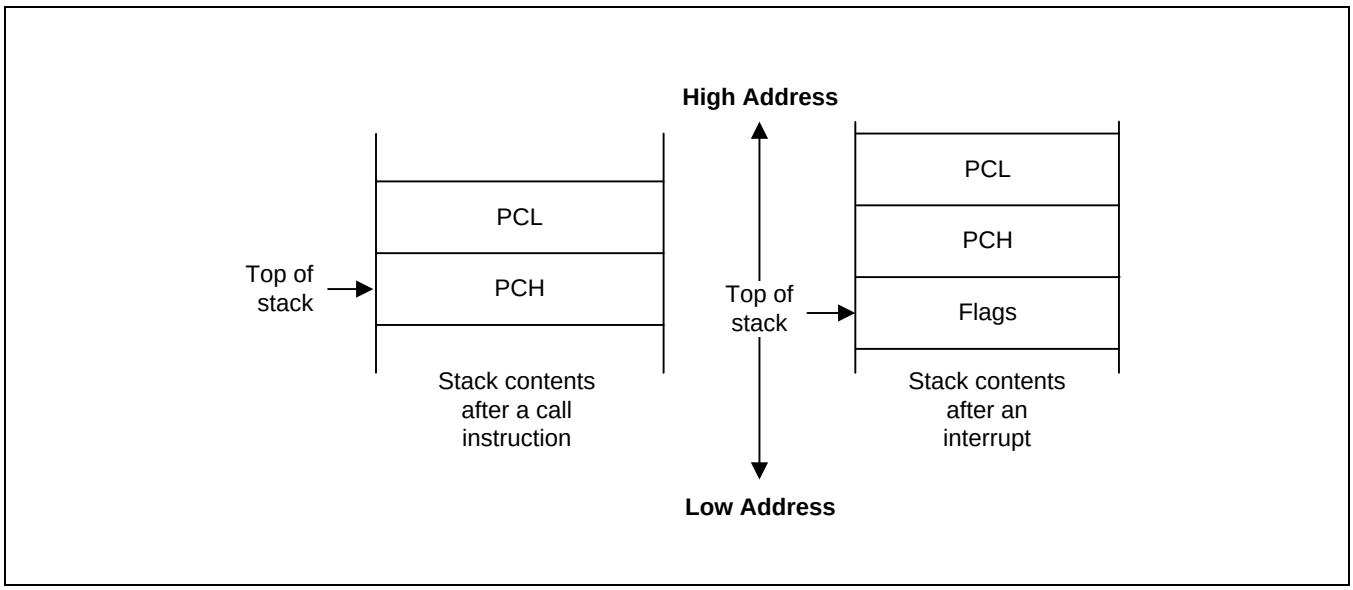


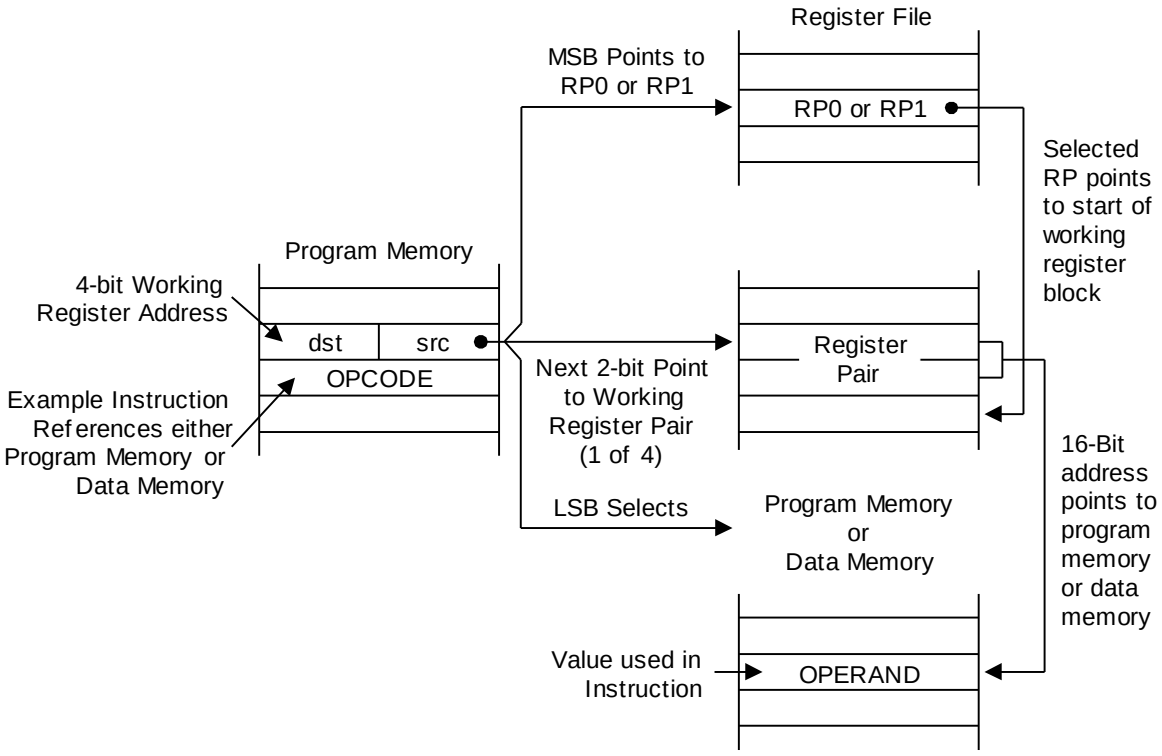
Figure 2-16 Stack Operations

2.5.2 User-Defined Stacks

You can freely define stacks in the internal register file as data storage locations. The instructions PUSHUI, PUSHUD, POPUI, and POPUD support user-defined stack operations.

2.5.3 Stack Pointers (SPL)

Register location D9H contains the 8-bit stack pointer (SPL) that is used for system stack operations. After a reset, the SPL value is undetermined. Because only internal memory 256byte is implemented in The S3F8S28/S3F8S24, the SPL must be initialized to an 8-bit value in the range 00 to FFH.



Sample Instructions:

```
LCD     R5,@RR6      ;  Program memory access
LDE     R3,@RR14     ;  External data memory access
LDE     @RR4, R8     ;  External data memory access
```

Figure 3-6 Indirect Working Register Addressing to Program or Data Memory

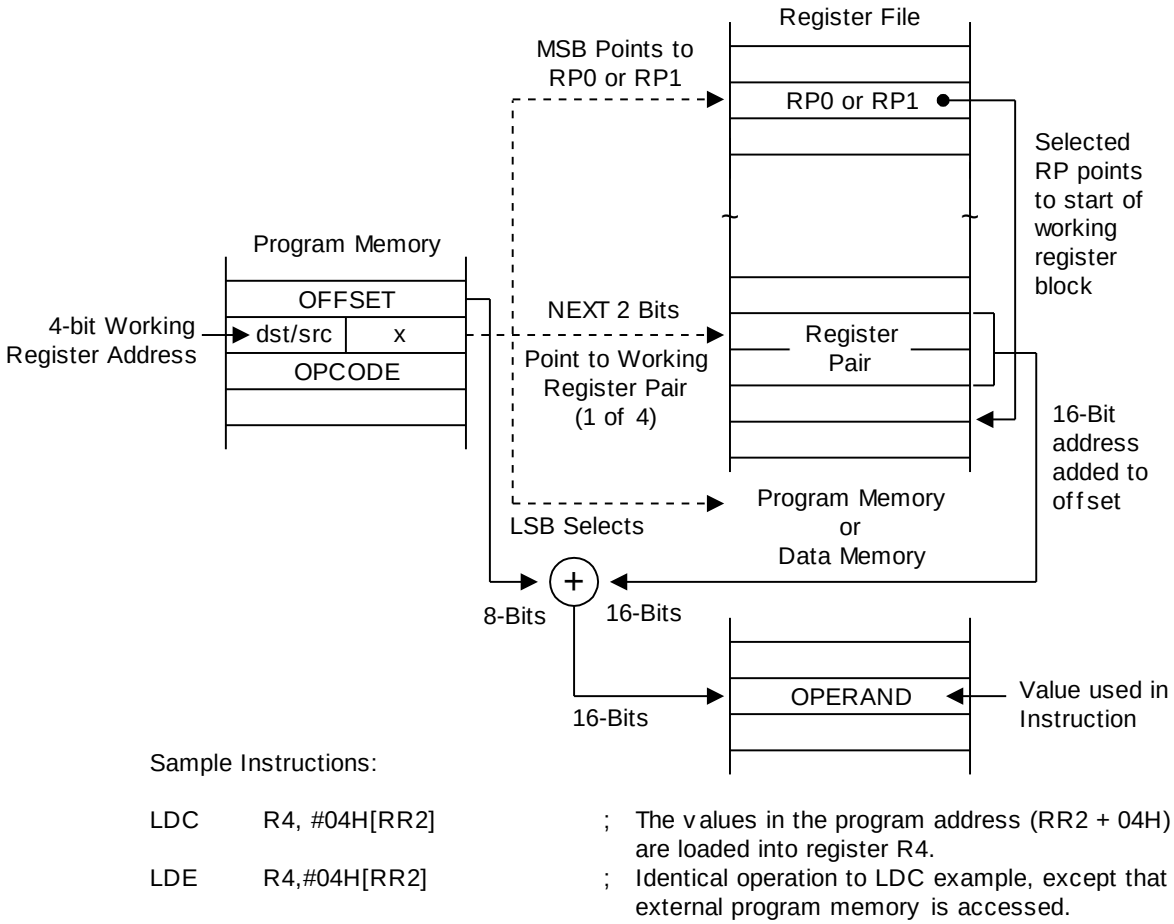


Figure 3-8 Indexed Addressing to Program or Data Memory with Short Offset

4.1.6 FMCON

- Flash Memory Control Register: ECH, SET 1, BANK 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
Reset Value	0	0	0	0	–	–	–	0
Read/Write	RW	RW	RW	RW	–	–	–	RW

.7–.4 Flash Memory Mode Selection Bits

0	1	0	1	Programming mode
1	0	1	0	Sector erase mode
0	1	1	0	Hard lock mode
Other values				Not available

.3–.1

Not used for the S3F8S28/S3F8S24

.0 Flash Operation Start Bit

0	Operation stop
1	Operation start (This bit will be cleared automatically just after the corresponding operator completed).

4.1.7 FMSECH

- Flash Memory Sector Address Register (High Byte): EEH, SET 1, BANK 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
Reset Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

.7–.0 Flash Memory Sector Address Bits (High Byte)

The 15th to 8th bits to select a sector of Flash ROM

NOTE: The high-byte Flash memory sector address pointer value is the higher eight bits of the 16-bit pointer address.

4.1.22 P1CON

- Port 1 Control Register: E9H, SET 1, BANK 0

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
Reset Value	0	0	–	–	0	0	0	0
Read/Write	RW	RW	–	–	RW	RW	RW	RW

.7 Part 1.1 N-channel open-drain Enable Bit

0	Configure P1.1 as a push-pull output
1	Configure P1.1 as a n-channel open-drain output

.6 Port 1.0 N-channel open-drain Enable Bit

0	Configure P1.0 as a push-pull output
1	Configure P1.0 as a n-channel open-drain output

.5

Not used for S3F8S28/S3F8S24

.4 Port 1.2 Configuration Bit

0	Configure P1.2 as a Schmitt trigger input;
1	Configure P1.2 as a open-drain output

.3–.2 Port 1, P1.1 Configuration Bits

0	0	Schmitt trigger input;
0	1	Schmitt trigger input; pull-up enable
1	0	Output
1	1	Schmitt trigger input; pull-down enable

.1–.0 Port 1, P1.0 Configuration Bits

0	0	Schmitt trigger input;
0	1	Schmitt trigger input; pull-up enable
1	0	Output
1	1	Schmitt trigger input; pull-down enable

NOTE: When you use external oscillator, P1.0, P1.1 must be set to output port to prevent current consumption.

4.1.39 SYM

- System Mode Register: DEH, SET 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
Reset Value	0	–	–	x	x	x	0	0
Read/Write	RW	–	–	RW	RW	RW	RW	RW

.7 Tri-state External Interface Control Bit (1)

0	Normal operation (disable tri-state operation)
1	Set external interface lines to high impedance (enable tri-state operation)

.6–.5

Not used for the S3F8S28/S3F8S24

.4–.2 Fast Interrupt Level Selection Bits (2)

0	0	0	IRQ0
0	0	1	IRQ1
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

.1 Fast Interrupt Enable Bit (3)

0	Disable fast interrupt processing
1	Enable fast interrupt processing

.0 Global Interrupt Enable Bit (4)

0	Disable all interrupt processing
1	Enable all interrupt processing

NOTE:

1. Because an external interface is not implemented, SYM.7 must always be "0".
2. You can select only one interrupt level at a time for fast interrupt processing.
3. Setting SYM.1 to "1" enables fast interrupt processing for the interrupt level currently selected by SYM.2 to SYM.4.
4. Following a reset, you must enable global interrupt processing by executing an EI instruction (not by writing a "1" to SYM.0).

6.5.19 CPIJNE (Compare, Increment, and Jump on Non-Equal)

CPIJNE dst, src, RA

Operation: If dst – src "0", PC ← PC + RA
Ir ← Ir + 1
The source operand is compared to (subtracted from) the destination operand. If the result is not "0", the relative address is added to the program counter and control passes to the statement whose address is now in the program counter; otherwise the instruction following the CPIJNE instruction is executed. In either case the source pointer is incremented by one before the next instruction.

Flags: No flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst	Addr Mode src
opc | src | dst | RA	3	12	D2	r	Ir

NOTE: Execution time is 18 cycles if the jump is taken or 16 cycles if it is not taken.

Example: Given: R1 = 02H, R2 = 03H, and Register 03H = 04H:

CPIJNER1, @R2, SKIP → R2 = 04H, PC jumps to SKIP location

Working register R1 contains the value 02H, working register R2 (the source pointer) the value 03H, and general register 03 the value 04H. The statement "CPIJNE R1, @R2, SKIP" subtracts 04H (00000100B) from 02H (00000010B). Because the result of the comparison is non-equal, the relative address is added to the PC and the PC then jumps to the memory location pointed to by SKIP. The source pointer register (R2) is also incremented by one, leaving a value of 04H. (Remember that the memory location must be within the allowed range of + 127 to – 128.)

6.5.49 POPUI (Pop User Stack-Incrementing)

POPUI dst, src

Operation: dst ← src
IR ← IR + 1
The POPUI instruction is used for user-defined stacks in the register file. The contents of the register file location addressed by the user stack pointer are loaded into the destination. The user stack pointer is then incremented.

Flags: No flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst	Addr Mode src
opc | src | dst	3	8	93	R	IR

Example: Given: Register 00H = 01H and Register 01H = 70H:

POPUI 02H, @00H → Register 00H = 02H, Register 01H = 70H, Register 02H = 70H

If general register 00H contains the value 01H and register 01H the value 70H, the statement "POPUI 02H, @00H" loads the value 70H into the destination general register 02H. The user stack pointer (register 00H) is then incremented by one, changing its value from 01H to 02H.

8.2 Power-Down Modes

8.2.1 Stop Mode

Stop mode is invoked by the instruction STOP (OPCODE 7FH). In Stop mode, the operation of the CPU and all peripherals is halted. That is, the on-chip main oscillator stops and the supply current is reduced to less than 4μA except that the LVR (Low Voltage Reset) is enable. All system functions are halted when the clock "freezes", but data stored in the internal register file is retained. Stop mode can be released in one of three ways: by a nRESET signal, by an external interrupt or by Watchdog Timer interrupt.

NOTE: Before execute the STOP instruction, must set the STPCON register as "10100101b".

8.2.2 Sources to Release Stop Mode

Stop mode is released when following sources go active:

- System Reset by external reset pin (nRESET)
- External Interrupt (INT0 to INT7)
- Watchdog Timer Interrupt (WDTINT)

8.2.2.1 Using RESET to Release Stop Mode

Stop mode is released when the nRESET signal is released and returns to High level. All system and peripheral control registers are then Reset to their default values and the contents of all data registers are retained. A Reset operation automatically selects a slow clock (f_{OSC}/16) because CLKCON.3 and CLKCON.4 are cleared to "00B". After the oscillation stabilization interval has elapsed, the CPU executes the system initialization routine by fetching the 16-bit address stored in ROM locations 0100H and 0101H.

8.2.2.2 Using an External Interrupt to Release Stop Mode

External interrupts with an RC-delay noise filter circuit can be used to release Stop mode (Clock-related external interrupts cannot be used). External interrupts INT0 to INT7 in the S3F8S28/S3F8S24 interrupt structure meet this criterion.

Port 0 Pull-up Resistor Enable Register
E5H, Bank 0, R/W; Reset Value: 00H

MSB	.7	.6	.5	.4	.3	.2	.1	.0	LSB

[.7] P0.7 Pull-up Resistor Enable bit
0 = Enable Pull-up Resistor
1 = Disable Pull-up Resistor

[.6] P0.6 Pull-up Resistor Enable bit
0 = Enable Pull-up Resistor
1 = Disable Pull-up Resistor

[.5] P0.5 Pull-up Resistor Enable bit
0 = Enable Pull-up Resistor
1 = Disable Pull-up Resistor

[.4] P0.4 Pull-up Resistor Enable bit
0 = Enable Pull-up Resistor
1 = Disable Pull-up Resistor

[.3] P0.3 Pull-up Resistor Enable bit
0 = Disable Pull-up Resistor
1 = Enable Pull-up Resistor

[.2] P0.2 Pull-up Resistor Enable bit
0 = Disable Pull-up Resistor
1 = Enable Pull-up Resistor

[.1] P0.1 Pull-up Resistor Enable bit
0 = Disable Pull-up Resistor
1 = Enable Pull-up Resistor

[.0] P0.0 Pull-up Resistor Enable bit
0 = Disable Pull-up Resistor
1 = Enable Pull-up Resistor

Figure 9-6 Port 0 Pull-Up Resistor Enable Registers (P0PUR)

9.2.2 Port 1

Port 1, is a 3-bit I/O port with individually configurable pins. It can be used for general I/O port (Schmitt trigger input mode, push-pull output mode or n-channel open-drain output mode). In addition, you can configure a pull-up and pull-down resistor to individual pin using control register settings. It is designed for high-current functions such as LED direct drive. P1.0, P1.1 are used for oscillator input/output by Smart Option. Also, P1.2 is used for RESET pin by Smart Option.

NOTE: When P1.2 is configured as a general I/O port, it can be used only Schmitt trigger input without pull-up or open-drain output.

One control register is used to control port 1: P1CON (E9H).You address port 1 bits directly by writing or reading the port 1 data register, P1 (E1H). When you use external oscillator, P1.0 and P1.1 must be set to output port to prevent current consumption.

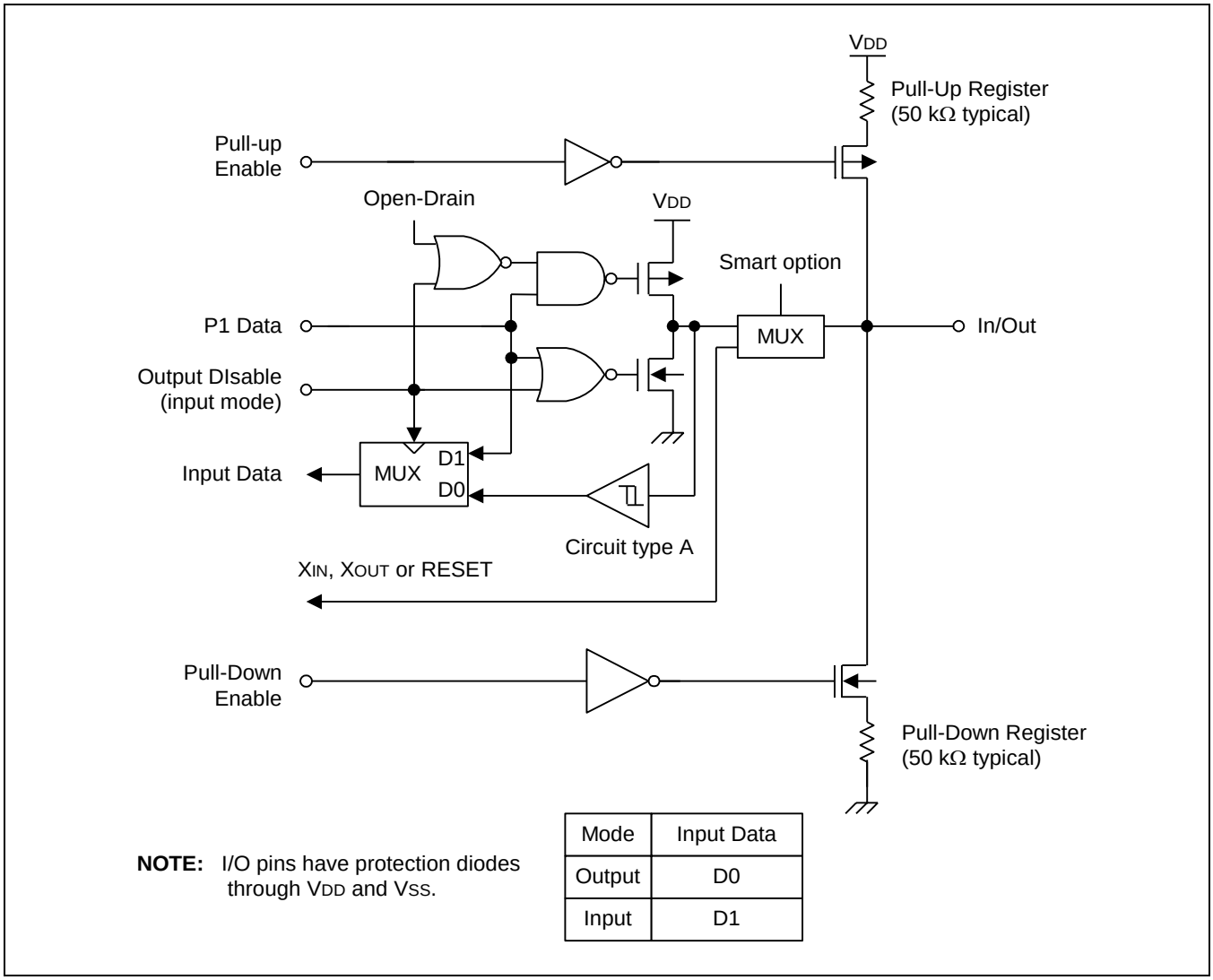
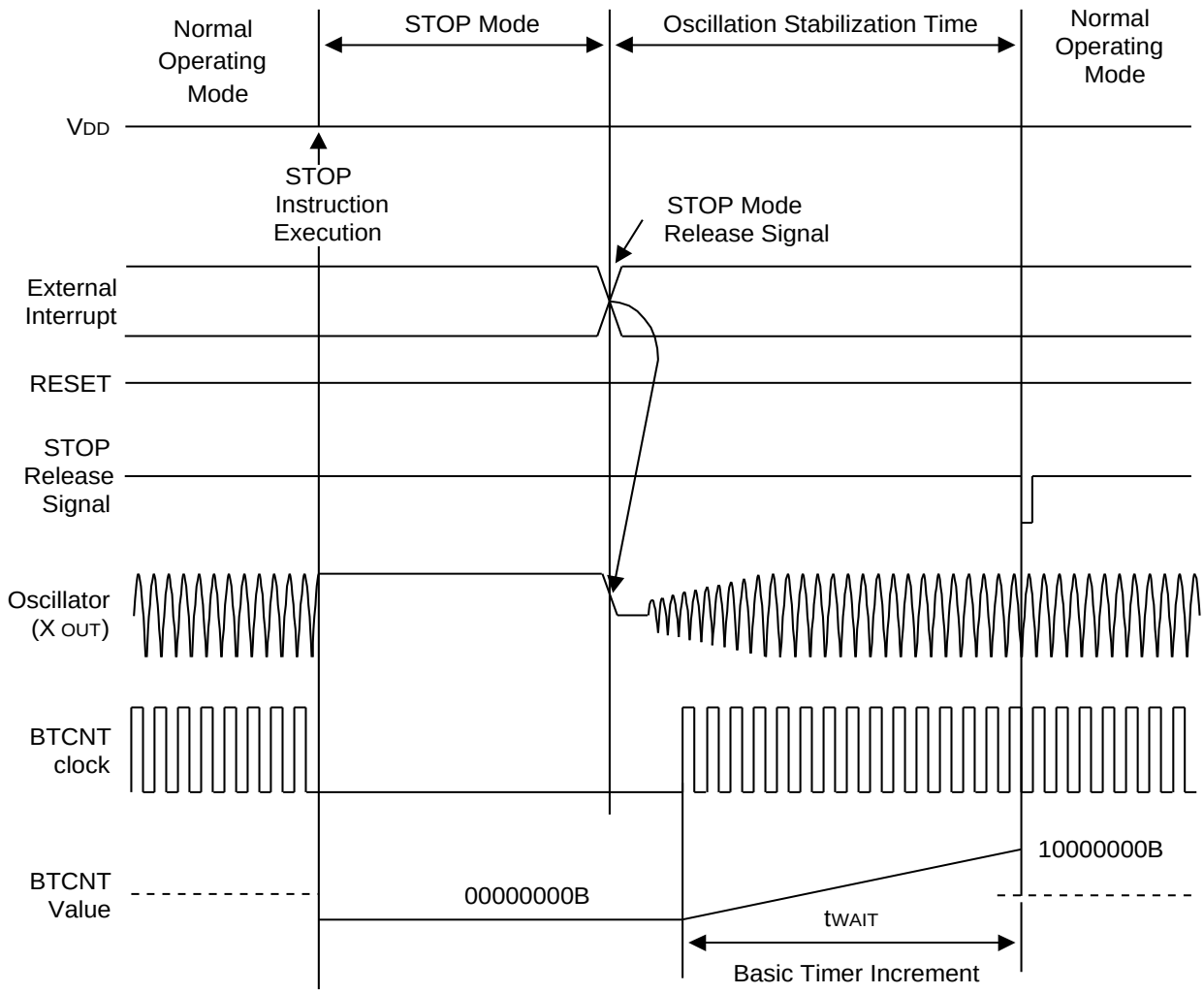


Figure 9-7 Port 1 Circuit Diagram



NOTE: Duration of the oscillator stabilzation wait time, t WAIT , it is released by an interrupt is determined by the setting in basic timer control register, BTCON.

BTCON.3	BTCON.2	t WAIT	t WAIT (When fosc is 10 MHz)
0	0	(4096 x 128)/fosc	52.4 ms
0	1	(1024 x 128)/fosc	13.1 ms
1	0	(128 x 128)/fosc	1.63 ms
1	1	Invalid setting	—

Figure 10-3 Oscillation Stabilization Time on Stop Mode Release

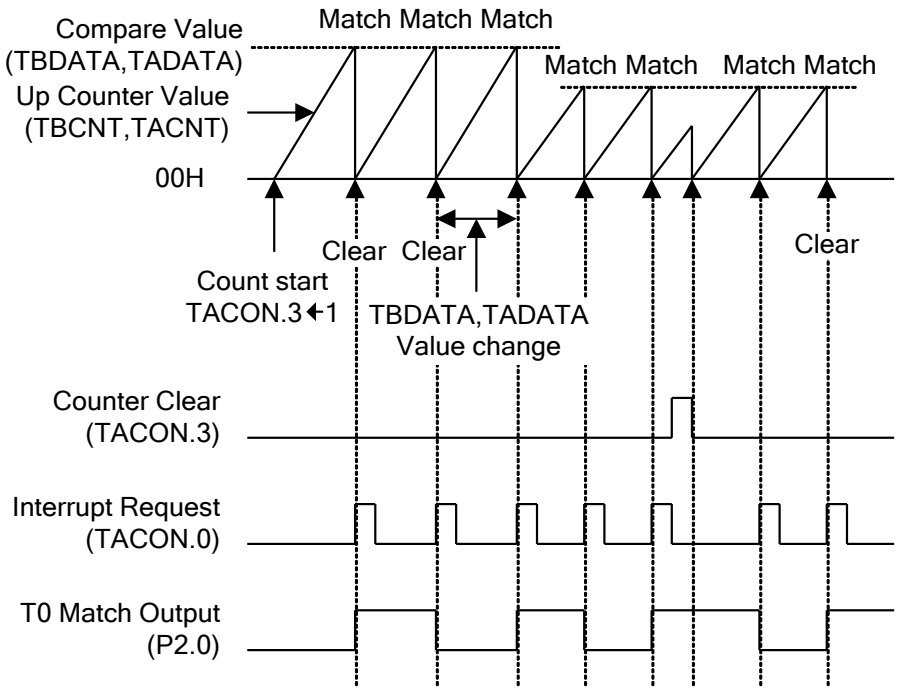


Figure 10-5 Timer 0 Timing Diagram

10.4 Two 8-Bit Timers Mode (Timer A and B)

10.4.1 Overview

The 8-bit timer A and B are the 8-bit general-purpose timers. Timer A and B support interval timer mode using the appropriate TACON and TBCON setting, respectively.

Timer A and Timer B have the following functional components:

- Clock frequency divider with multiplexer
  - fxx divided by 256, 64, 8, or 1 for timer A
  - fxx divided by 256, 64, 8, or 1 for timer B
- 8-bit counter (TACNT, TBCNT), 8-bit comparator, and 8-bit reference data register (TADATA, TBDATA)
- Timer A match interrupt (IRQ1, vector F6H) generation
- Timer A control register, TACON (D2H, read/write)
- Timer B match interrupt (IRQ1, vector F4H) generation
- Timer B control register, TBCON (EEH, read/write)

10.4.2 Function Description

10.4.2.1 Interval Timer Function

The timer A and B module can generate an interrupt: the timer A match interrupt (TAINT) and the timer B match interrupt (TBINT). TAINT belongs to the interrupt level IRQ1, and is assigned a separate vector address, F6H. TBINT belongs to the interrupt level IRQ1 and is assigned a separate vector address, F4H.

The TAINT and TBINT pending condition should be cleared by software after they are serviced.

In interval timer mode, a match signal is generated when the counter value is identical to the values written to the TA or TB reference data registers, TADATA or TBDATA. The match signal generates corresponding match interrupt (TAINT, vector F6H; TBINT, vector F4H) and clears the counter.

If, for example, you write the value 10H to TBDATA, "0" to TACON.7, and 0EH to TBCON, the counter will increment until it reaches 10H. At this point, the TB interrupt request is generated, the counter value is reset, and counting resumes.

13.2.5 PWM Function Description

The PWM output signal toggles to Low level whenever the lower base counter matches the reference value stored in the module's data register (PWM0DATA, PWM1DATA). If the value in the data register is not zero, an overflow of the lower counter causes the PWM output to toggle to High level. In this way, the reference value written to the data register determines the module's base duty cycle.

The value in the extension counter is compared with the extension settings in the extension data bits. This extension counter value, together with extension logic and the PWM module's extension bits, is then used to "stretch" the duty cycle of the PWM output. The "stretch" value is one extra clock period at specific intervals, or cycles (see *Table 13-2*).

If, for example, in 8-bit base + 6-bit extension mode, the value in the extension register is "04H", the 32nd cycle will be one pulse longer than the other 63 cycles. If the base duty cycle is 50%, the duty of the 32nd cycle will therefore be "stretched" to approximately 51% duty. For example, if you write 80H to the extension register, all odd-numbered cycles will be one pulse longer. If you write FCH to the extension register, all cycles will be stretched by one pulse except the 64th cycle. PWM output goes to an output buffer and then to the corresponding PWM output pin. In this way, you can obtain high output resolution at high frequencies.

14.5 Conversion timing

The A/D conversion process requires 1 step (1 clock edge) to convert each bit and 5 clocks to step-up A/D conversion. Therefore, total of 17 clocks are required to complete a 12-bit conversion: With an 10MHz CPU clock frequency, one clock cycle is 1.2μs ($12/f_{OSC}$). If each bit conversion requires 1 clock, the conversion rate is calculated as follows:

- 1 clock/bit × 12-bits + Sample time (5 clock) = 17 clocks
- 17 clock × 1.2μs = 20.4μs at 10MHz, 1 clock time = $12/f_{OSC}$ (assuming ADCON.2–.1 = 01)

17.2 Low Voltage Detector Control Register (LVDCON)

You use the Low Voltage Detector control register, LVDCON, to

- Enable low voltage detector circuit
- Check LVD flag
- Set low voltage detector flag level

LVDCON is located at address F4H, Set1, Bank 1, and is read/write addressable using register addressing mode.

A reset clears LVDCON to "00H". This disable Low Voltage Detector Circuit, set Low voltage detector level as 4.1V.

You can disable LVD at any time during normal operation by writing a "0" to LVDCON.7 for lower power consumption. Write specific value to LVDCON.1–0 to select LVD flag level.

To check a voltage detector result the application program should poll the Flag bit LVDCON.5. When a "1" is detected, VDD level has drop below LVD level.

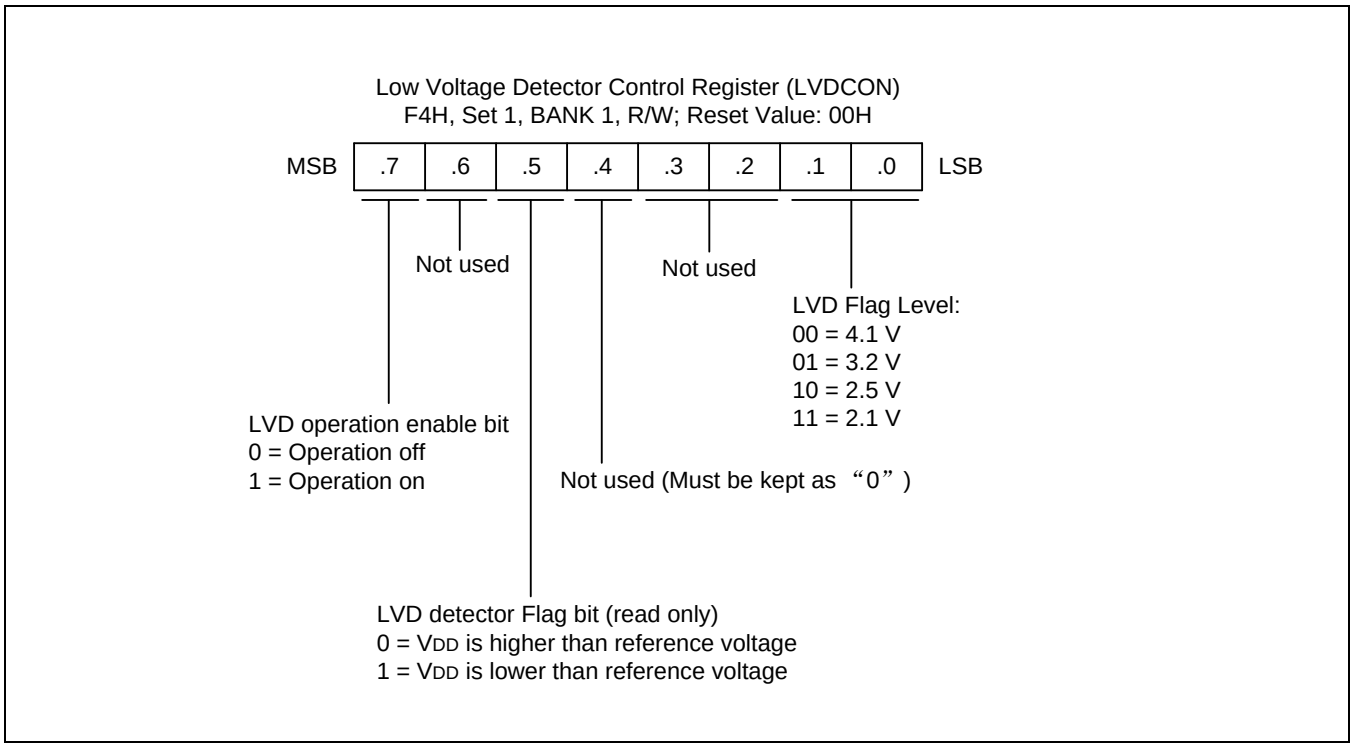


Figure 17-1 LVD Control Register (LVDCON)

18.2 Flash Memory Control Registers (User Program Mode)

18.2.1 Flash Memory Control Register (FMCON)

FMCON register is available only in user program mode to select the Flash memory operation mode; sector erase, byte programming, and to make the Flash memory into a hard lock protection.

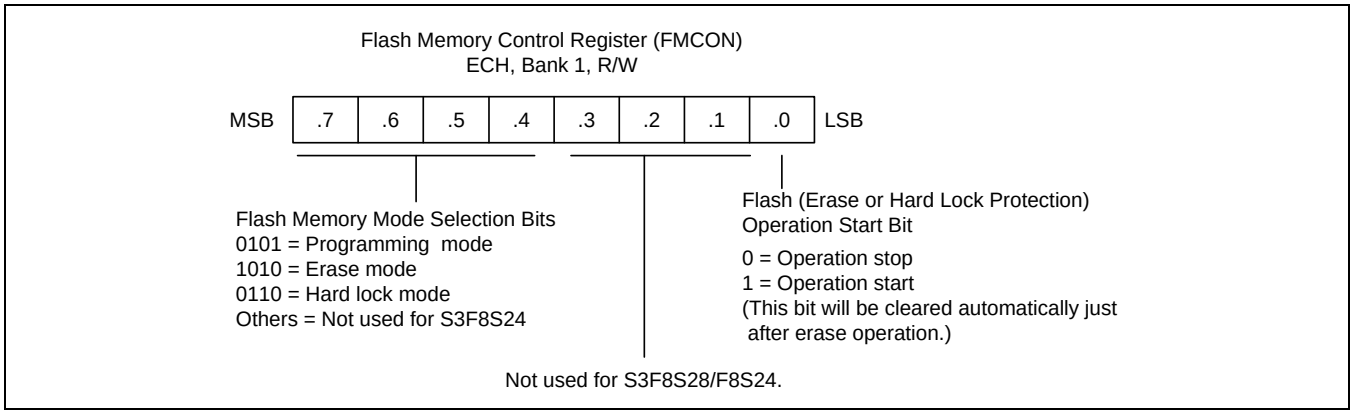


Figure 18-1 Flash Memory Control Register (FMCON)

The bit 0 of FMCON register (FMCON.0) is a bit for the operation start of Erase and Hard Lock Protection. Therefore, operation of Erase and Hard Lock Protection is activated when you set FMCON.0 to "1". If you write FMCON.0 to 1 for erasing, CPU is stopped automatically for erasing time (min.4ms). After erasing time, CPU is restarted automatically. When you read or program a byte data from or into Flash memory, this bit is not needed to manipulate.

18.2.2 Flash Memory User Programming Enable Register (FMUSR)

The FMUSR register is used for a safe operation of the Flash memory. This register will protect undesired erase or program operation from malfunctioning of CPU caused by an electrical noise. After reset, the user-programming mode is disabled, because the value of FMUSR is "00000000B" by reset operation. If necessary to operate the Flash memory, you can use the user programming mode by setting the value of FMUSR to "10100101B". The other value of "10100101B", user program mode is disabled.

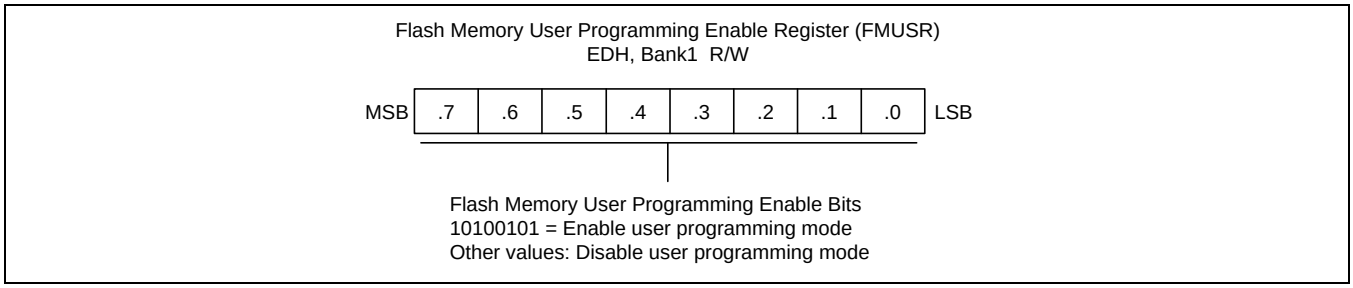
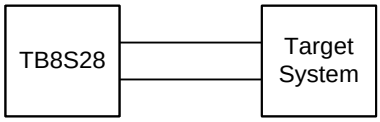
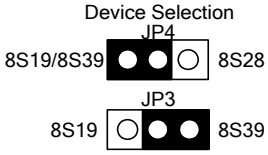
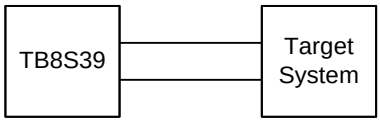
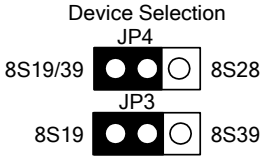
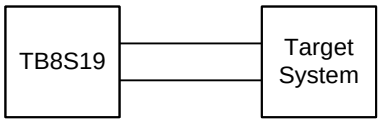


Figure 18-2 Flash Memory User Programming Enable Register (FMUSR)

Table 22-1 Components of TB8S19/8S28/8S39

Symbols	Usage	Description
JP3, JP4	Device Selection	Selection of device: S3F8S19, S3F8S28, S3F8S39
JP8, JP9	Ex.CLK selection	Set external clock connect to S3F8S28/S3F8S24 EVA-chip.
JP12	User's Power selection	Selection of Power to User.
JP2	MODE Selection	Selection of Eva/Main-chip mode of S3F8S28/S3F8S24 EVA-chip
JP1	Emulator selection	Selection of SMDS2/SMDS2+
JP5	Clock Source Selection	Selection of debug with internal/external clock
SW2, SW3	8-pin switch	Smart Option setting for S3F8S28/S3F8S24 EVA-chip
S1	100-pin connector	Connection between emulator and TB8S8S28 target board.
S3	24-pin connector	Connection between target board and user application system
RESET	Push button	Generation low active reset signal to S3F8S28/S3F8S24 EVA-chip
VCC, GND	POWER connector	External power connector for TB8S19/8S28/8S39
IDLE, STOP LED	STOP/IDLE Display	Indicate the status of STOP or IDLE of S3F8S28/F8S24 EVA-chip on TB8S19/8S28/8S39 target board
JP3	PWM selection	Selection of PWM enable/disable

Table 22-2 Device Selection Settings for TB8S19/8S28/8S39

"Device Selection" Settings	Operating Mode	Comments
		Operate with TB8S28
		Operate with TB8S39
		Operate with TB8S19

NOTE: The following symbol in the "8S28" Setting column indicates the electrical short (off) configuration: