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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f415rgt6

Table 2. STM32F415xx and STM32F417xx: features and peripheral counts

Peripherals	STM32F415RG	STM32F415OG	STM32F415VG	STM32F415ZG	STM32F417Vx	STM32F417Zx	STM32F417Ix
GPIOs	51	72	82	114	82	114	140
12-bit ADC Number of channels	3						
	16	13	16	24	16	24	24
12-bit DAC Number of channels	Yes 2						
Maximum CPU frequency	168 MHz						
Operating voltage	1.8 to 3.6 V(3)						
Operating temperatures	Ambient temperatures: –40 to +85 °C /–40 to +105 °C						
	Junction temperature: –40 to + 125 °C						
Package	LQFP64	WLCSP90	LQFP100	LQFP144	LQFP100	LQFP144	UFBGA176 LQFP176

1. For the LQFP100 and WLCSP90 packages, only FSMC Bank1 or Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the device operates in reduced temperature range, and with the use of an external power supply supervisor (refer to *Section : Internal reset OFF*).

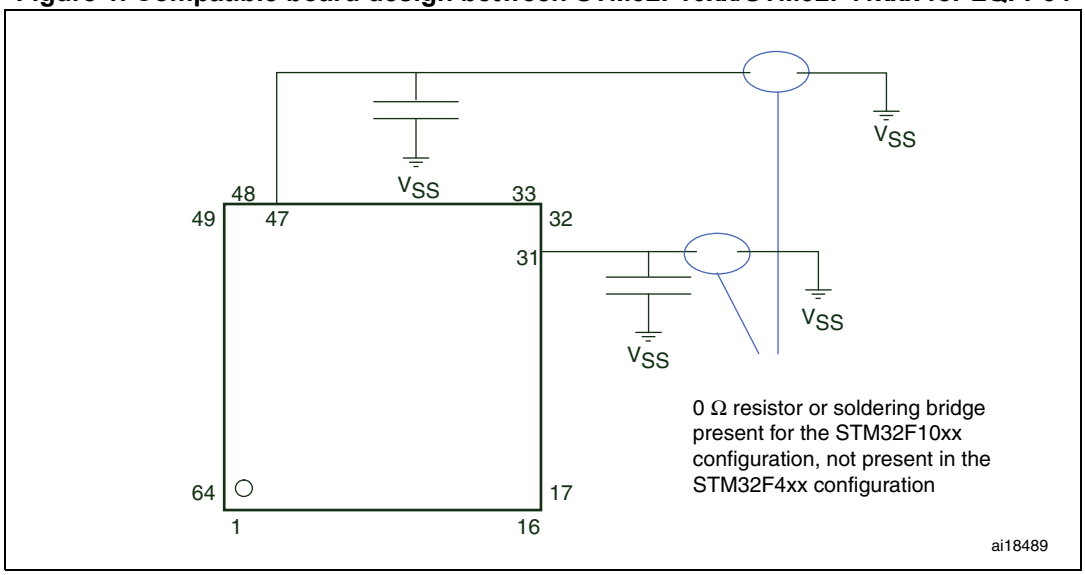
2.1 Full compatibility throughout the family

The STM32F415xx and STM32F417xx are part of the STM32F4 family. They are fully pin-to-pin, software and feature compatible with the STM32F2xx devices, allowing the user to try different memory densities, peripherals, and performances (FPU, higher frequency) for a greater degree of freedom during the development cycle.

The STM32F415xx and STM32F417xx devices maintain a close compatibility with the whole STM32F10xxx family. All functional pins are pin-to-pin compatible. The STM32F415xx and STM32F417xx, however, are not drop-in replacements for the STM32F10xxx devices: the two families do not have the same power scheme, and so their power pins are different. Nonetheless, transition from the STM32F10xxx to the STM32F41xxx family remains simple as only a few pins are impacted.

Figure 4, *Figure 3*, *Figure 2*, and *Figure 1* give compatible board designs between the STM32F41xxx, STM32F2, and STM32F10xxx families.

Figure 1. Compatible board design between STM32F10xx/STM32F41xxx for LQFP64



SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

2.2.22 Inter-integrated circuit interface (I²C)

Up to three I²C bus interfaces can operate in multimaster and slave modes. They can support the Standard-mode (up to 100 kHz) and Fast-mode (up to 400 kHz). They support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.2.23 Universal synchronous/asynchronous receiver transmitters (USART)

The STM32F415xx and STM32F417xx embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART6) and two universal asynchronous receiver transmitters (UART4 and UART5).

These six interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to communicate at speeds of up to 10.5 Mbit/s. The other available interfaces communicate at up to 5.25 Mbit/s.

USART1, USART2, USART3 and USART6 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 7. STM32F41xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
	D9			L4	48	BYPASS_REG	I	FT	-	-	-
19	E4	28	39	K4	49	V_{DD}	S	-	-	-	-
20	J9	29	40	N4	50	PA4	I/O	TTa	(4)	SPI1_NSS / SPI3_NSS / USART2_CK / DCMI_HSYNC / OTG_HS_SOF/ I2S3_WS/ EVENTOUT	ADC12_IN4 /DAC_OUT1
21	G8	30	41	P4	51	PA5	I/O	TTa	(4)	SPI1_SCK/ OTG_HS_ULPI_CK / TIM2_CH1_ETR/ TIM8_CH1N/ EVENTOUT	ADC12_IN5/DAC_ OUT2
22	H8	31	42	P3	52	PA6	I/O	FT	(4)	SPI1_MISO / TIM8_BKIN/TIM13_CH1 / DCMI_PIXCLK / TIM3_CH1 / TIM1_BKIN/ EVENTOUT	ADC12_IN6
23	J8	32	43	R3	53	PA7	I/O	FT	(4)	SPI1_MOSI/ TIM8_CH1N / TIM14_CH1/TIM3_CH2/ ETH_MII_RX_DV / TIM1_CH1N / ETH_RMII_CRS_DV/ EVENTOUT	ADC12_IN7
24	-	33	44	N5	54	PC4	I/O	FT	(4)	ETH_RMII_RX_D0 / ETH_MII_RX_D0/ EVENTOUT	ADC12_IN14
25	-	34	45	P5	55	PC5	I/O	FT	(4)	ETH_RMII_RX_D1 / ETH_MII_RX_D1/ EVENTOUT	ADC12_IN15
26	G7	35	46	R5	56	PB0	I/O	FT	(4)	TIM3_CH3 / TIM8_CH2N/ OTG_HS_ULPI_D1/ ETH_MII_RXD2 / TIM1_CH2N/ EVENTOUT	ADC12_IN8
27	H7	36	47	R4	57	PB1	I/O	FT	(4)	TIM3_CH4 / TIM8_CH3N/ OTG_HS_ULPI_D2/ ETH_MII_RXD3 / TIM1_CH3N/ EVENTOUT	ADC12_IN9
28	J7	37	48	M6	58	PB2/BOOT1 (PB2)	I/O	FT	-	EVENTOUT	-

Table 7. STM32F41xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
33	J3	51	73	P12	92	PB12	I/O	FT	-	SPI2_NSS / I2S2_WS / I2C2_SMBA/ USART3_CK/ TIM1_BKIN / CAN2_RX / OTG_HS_ULPI_D5/ ETH_RMII_TXD0 / ETH_MII_TXD0/ OTG_HS_ID/ EVENTOUT	-
34	J1	52	74	P13	93	PB13	I/O	FT	-	SPI2_SCK / I2S2_CK / USART3_CTS/ TIM1_CH1N /CAN2_TX / OTG_HS_ULPI_D6 / ETH_RMII_TXD1 / ETH_MII_TXD1/ EVENTOUT	OTG_HS_VBUS
35	J2	53	75	R14	94	PB14	I/O	FT	-	SPI2_MISO/ TIM1_CH2N / TIM12_CH1 / OTG_HS_DM/ USART3_RTS / TIM8_CH2N/I2S2ext_SD/ EVENTOUT	-
36	H1	54	76	R15	95	PB15	I/O	FT	-	SPI2_MOSI / I2S2_SD/ TIM1_CH3N / TIM8_CH3N / TIM12_CH2 / OTG_HS_DP/ EVENTOUT	RTC_REFIN
-	H2	55	77	P15	96	PD8	I/O	FT	-	FSMC_D13 / USART3_TX/ EVENTOUT	-
-	H3	56	78	P14	97	PD9	I/O	FT	-	FSMC_D14 / USART3_RX/ EVENTOUT	-
-	G3	57	79	N15	98	PD10	I/O	FT	-	FSMC_D15 / USART3_CK/ EVENTOUT	-
-	G1	58	80	N14	99	PD11	I/O	FT	-	FSMC_CLE / FSMC_A16/USART3_CTS/ EVENTOUT	-
-	G2	59	81	N13	100	PD12	I/O	FT	-	FSMC_ALE/ FSMC_A17/TIM4_CH1 / USART3_RTS/ EVENTOUT	-

Table 7. STM32F41xxx pin and ball definitions (continued)

Pin number						Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176						
-	A4	85	118	D10	146	PD4	I/O	FT	-	FSMC_NOE/ USART2_RTS/ EVENTOUT	-
-	C6	86	119	C11	147	PD5	I/O	FT	-	FSMC_NWE/USART2_TX/ EVENTOUT	-
-	-	-	120	D8	148	V_{SS}	S	-	-	-	-
-	-	-	121	C8	149	V_{DD}	S	-	-	-	-
-	B5	87	122	B11	150	PD6	I/O	FT	-	FSMC_NWAIT/ USART2_RX/ EVENTOUT	-
-	A5	88	123	A11	151	PD7	I/O	FT	-	USART2_CK/FSMC_NE1/ FSMC_NCE2/ EVENTOUT	-
-	-	-	124	C10	152	PG9	I/O	FT	-	USART6_RX / FSMC_NE2/FSMC_NCE3/ EVENTOUT	-
-	-	-	125	B10	153	PG10	I/O	FT	-	FSMC_NCE4_1/ FSMC_NE3/ EVENTOUT	-
-	-	-	126	B9	154	PG11	I/O	FT	-	FSMC_NCE4_2 / ETH_MII_TX_EN/ ETH _RMII_TX_EN/ EVENTOUT	-
-	-	-	127	B8	155	PG12	I/O	FT	-	FSMC_NE4 / USART6_RTS/ EVENTOUT	-
-	-	-	128	A8	156	PG13	I/O	FT	-	FSMC_A24 / USART6_CTS /ETH_MII_TXD0/ ETH_RMII_TXD0/ EVENTOUT	-
-	-	-	129	A7	157	PG14	I/O	FT	-	FSMC_A25 / USART6_TX /ETH_MII_TXD1/ ETH_RMII_TXD1/ EVENTOUT	-
-	E8	-	130	D7	158	V_{SS}	S	-	-	-	-
-	F7	-	131	C7	159	V_{DD}	S	-	-	-	-
-	-	-	132	B7	160	PG15	I/O	FT	-	USART6_CTS / DCMI_D13/ EVENTOUT	-

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/SPI2/I2S2/I2S2ext	SPI3/I2Sext/I2S3	USART1/2/3/I2S3ext	UART4/5/USART6	CAN1/2 TIM12/13/14	OTG_FS/OTG_HS	ETH	FSMC/SDIO/OTG_FS	DCMI		
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	FSMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	-	FSMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	-	FSMC_A2	-	-	EVENTOUT
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A3	-	-	EVENTOUT
	PF4	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A4	-	-	EVENTOUT
	PF5	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A5	-	-	EVENTOUT
	PF6	-	-	-	TIM10_CH1	-	-	-	-	-	-	-	-	FSMC_NIORD	-	-	EVENTOUT
	PF7	-	-	-	TIM11_CH1	-	-	-	-	-	-	-	-	FSMC_NREG	-	-	EVENTOUT
	PF8	-	-	-	-	-	-	-	-	-	TIM13_CH1	-	-	FSMC_NIOWR	-	-	EVENTOUT
	PF9	-	-	-	-	-	-	-	-	-	TIM14_CH1	-	-	FSMC_CD	-	-	EVENTOUT
	PF10	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_INTR	-	-	EVENTOUT
	PF11	-	-	-	-	-	-	-	-	-	-	-	-		DCMI_D12	-	EVENTOUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A6	-	-	EVENTOUT
	PF13	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A7	-	-	EVENTOUT
	PF14	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A8	-	-	EVENTOUT
	PF15	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A9	-	-	EVENTOUT

Additional current consumption

The MCU is placed under the following conditions:

- All I/O pins are configured in analog mode.
- The Flash memory access time is adjusted to f_{HCLK} frequency.
- The voltage scaling is adjusted to f_{HCLK} frequency as follows:
  - Scale 2 for $f_{HCLK} \leq 144$ MHz
  - Scale 1 for 144 MHz < $f_{HCLK} \leq 168$ MHz.
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
- The HSE crystal clock frequency is 25 MHz.
- T_A= 25 °C.

Table 26. Typical current consumption in Run mode, code with data processing running from Flash memory, regulator ON (ART accelerator enabled except prefetch), V_{DD} = 1.8 V(1)

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ. at T_A = 25 °C	Unit
IDD	Supply current in Run mode	All peripheral disabled	160	36.2	mA
			144	29.3	
			120	24.7	
			90	19.3	
			60	13.4	
			30	7.7	
			25	6.0	

1. When peripherals are enabled, the power consumption corresponding to the analog part of the peripherals (such as ADC or DAC) is not included.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 48: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to

Table 27. Switching output I/O current consumption

Symbol	Parameter	Conditions(1)	I/O toggling frequency (f_{SW})	Typ	Unit
I_{DDIO}	I/O switching current	V_{DD} = 3.3 V(2) C = C_{INT}	2 MHz	0.02	mA
			8 MHz	0.14	
			25 MHz	0.51	
			50 MHz	0.86	
			60 MHz	1.30	
		V_{DD} = 3.3 V C_{EXT} = 0 pF C = C_{INT} + C_{EXT}+ C_S	2 MHz	0.10	
			8 MHz	0.38	
			25 MHz	1.18	
			50 MHz	2.47	
			60 MHz	2.86	
		V_{DD} = 3.3 V C_{EXT} = 10 pF C = C_{INT} + C_{EXT}+ C_S	2 MHz	0.17	
			8 MHz	0.66	
			25 MHz	1.70	
			50 MHz	2.65	
			60 MHz	3.48	
		V_{DD} = 3.3 V C_{EXT} = 22 pF C = C_{INT} + C_{EXT}+ C_S	2 MHz	0.23	
			8 MHz	0.95	
			25 MHz	3.20	
			50 MHz	4.69	
			60 MHz	8.06	
		V_{DD} = 3.3 V C_{EXT} = 33 pF C = C_{INT} + C_{EXT}+ C_S	2 MHz	0.30	
			8 MHz	1.22	
			25 MHz	3.90	
			50 MHz	8.82	
			60 MHz	-(3)	

1. C_S is the PCB board capacitance including the pad pin. C_S = 7 pF (estimated value).
2. This test is performed by cutting the LQFP package pin (pad removal).
3. At 60 MHz, C maximum load is specified 30 pF.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 28*. The MCU is placed under the following conditions:

- At startup, all I/O pins are configured as analog pins by firmware.
- All peripherals are disabled unless otherwise mentioned
- The code is running from Flash memory and the Flash memory access time is equal to 5 wait states at 168 MHz.
- The code is running from Flash memory and the Flash memory access time is equal to 4 wait states at 144 MHz, and the power scale mode is set to 2.
- The ART accelerator is ON.
- The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with one peripheral clocked on (with only the clock applied)
- When the peripherals are enabled: HCLK is the system clock, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
- The typical values are obtained for V_{DD} = 3.3 V and T_A= 25 °C, unless otherwise specified.

Table 28. Peripheral current consumption

Peripheral		I_{DD}(Typ)(1)		Unit
		Scale1 (up t 168 MHz)	Scale2 (up to 144 MHz)	
AHB1 (up to 168 MHz)	GPIOA	2.70	2.40	µA/MHz
	GPIOB	2.50	2.22	
	GPIOC	2.54	2.28	
	GPIOD	2.55	2.28	
	GPIOE	2.68	2.40	
	GPIOF	2.53	2.28	
	GPIOG	2.51	2.22	
	GPIOH	2.51	2.22	
	GPIOI	2.50	2.22	
	OTG_HS+ULPI	28.33	25.38	
	CRC	0.41	0.40	
	BKPSRAM	0.63	0.58	
	DMA1	37.44	33.58	
	DMA2	37.69	33.93	
	ETH_MAC ETH_MAC_TX ETH_MAC_RX ETH_MAC_PTP	20.43	18.39	

A device reset allows normal operations to be resumed.

The test results are given in *Table 43*. They are based on the EMS levels and classes defined in application note AN1709.

Table 43. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP176, T_A = +25 °C, f_{HCLK} = 168 MHz, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP176, T_A = +25 °C, f_{HCLK} = 168 MHz, conforms to IEC 61000-4-2	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 48. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{HYS}	FT, TTa and NRST I/O input hysteresis		1.7 V ≤V_{DD} ≤3.6 V	10%V_{DD}(3)	-	-	V
	BOOT0 I/O input hysteresis		1.75 V ≤V_{DD} ≤3.6 V -40 °C≤T_A ≤105 °C	0.1	-	-	
			1.7 V ≤V_{DD} ≤3.6 V 0 °C≤T_A ≤105 °C				
I_{lkg}	I/O input leakage current (4)		V_{SS} ≤V_{IN} ≤V_{DD}	-	-	±1	µA
	I/O FT input leakage current (5)		V_{IN} = 5 V	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(6)	All pins except for PA10 and PB12 (OTG_FS_ID, OTG_HS_ID)	V_{IN} = V_{SS}	30	40	50	kΩ
		PA10 and PB12 (OTG_FS_ID, OTG_HS_ID)	-	7	10	14	
R_{PD}	Weak pull-down equivalent resistor(7)	All pins except for PA10 and PB12	V_{IN} = V_{DD}	30	40	50	
		PA10 and PB12	-	7	10	14	
C_{IO}(8)	I/O pin capacitance			-	5	-	pF

1. Guaranteed by design.
2. Tested in production.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 47: I/O current injection susceptibility*
5. To sustain a voltage higher than V_{DD} + 0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to *Table 47: I/O current injection susceptibility*.
6. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ±3mA. When using the PC13 to PC15 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 12*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 12*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 49* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*. All I/Os are CMOS and TTL compliant.

Table 49. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(2)	Output low level voltage	CMOS port I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage		V_{DD}–0.4	-	
V_{OL} (2)	Output low level voltage	TTL port I_{IO} =+ 8mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage		2.4	-	
V_{OL}(2)(4)	Output low level voltage	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH}(3)(4)	Output high level voltage		V_{DD}–1.3	-	
V_{OL}(2)(4)	Output low level voltage	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(3)(4)	Output high level voltage		V_{DD}–0.4	-	

1. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
2. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 12* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 12* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Guaranteed by characterization.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 37* and *Table 50*, respectively.

Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 50. I/O AC characteristics(1)(2)

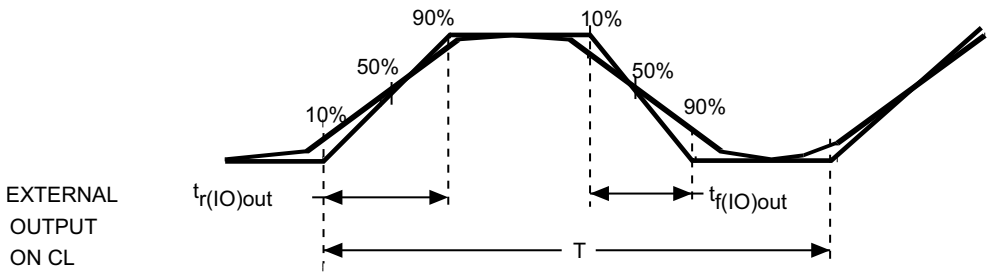
OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} > 2.70 V	-	-	4	MHz
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	2	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	8	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	4	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} = 1.8 V to 3.6 V	-	-	100	ns
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} > 2.70 V	-	-	25	MHz
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	12.5	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	50(4)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	20	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} >2.7 V	-	-	10	ns
			C_L = 50 pF, V_{DD} > 1.8 V	-	-	20	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	6	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	10	
10	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 40 pF, V_{DD} > 2.70 V	-	-	50(4)	MHz
			C_L = 40 pF, V_{DD} > 1.8 V	-	-	25	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	100(4)	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	50(4)	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 40 pF, V_{DD} > 2.70 V	-	-	6	ns
			C_L = 40 pF, V_{DD} > 1.8 V	-	-	10	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	4	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	6	

Table 50. I/O AC characteristics[1][2] (continued)

OSPEEDRy [1:0] bit value[1]	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	$F_{max(IO)out}$	Maximum frequency[3]	C_L = 30 pF, V_{DD} > 2.70 V	-	-	100[4]	MHz
			C_L = 30 pF, V_{DD} > 1.8 V	-	-	50[4]	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	180[4]	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	100[4]	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 30 pF, V_{DD} > 2.70 V	-	-	4	ns
			C_L = 30 pF, V_{DD} > 1.8 V	-	-	6	
			C_L = 10 pF, V_{DD} > 2.70 V	-	-	2.5	
			C_L = 10 pF, V_{DD} > 1.8 V	-	-	4	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller		10	-	-	ns

1. Guaranteed by characterization.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F4xx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in *Figure 37*.
4. For maximum frequencies above 50 MHz, the compensation cell should be used.

Figure 37. I/O AC characteristics definition



Maximum frequency is achieved if (t_r + t_f) ≤ (2/3)T and if the duty cycle is (45-55%) when loaded by CL specified in the table " *I/O AC characteristics*".

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I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 56* for the i²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 14*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}

Refer to *Section 5.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 56. I²S dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I²S main clock output	-	256 x 8K	256 x F_S(2)	MHz
f_{CK}	I²S clock frequency	Master data: 32 bits	-	64 x F_S	MHz
		Slave data: 32 bits	-	64 x F_S	
D_{CK}	I²S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	0	6	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	1	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	7.5	-	
$t_{su(SD\_SR)}$		Slave receiver	2	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	0	-	
$t_{h(SD\_SR)}$		Slave receiver	0	-	
$t_{v(SD\_ST)}$ $t_{h(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	27	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	20	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	2.5	-	

1. Guaranteed by characterization.
2. The maximum value of 256 x F_S is 42 MHz (APB1 maximum frequency).

Note: Refer to the I²S section of RM0090 reference manual for more details on the sampling frequency (F_S). f_{MCK}, f_{CK}, and D_{CK} values reflect only the digital peripheral behavior. The value of these parameters might be slightly impacted by the source clock accuracy. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of I2SDIV / (2 x I2SDIV + ODD) and a maximum value of (I2SDIV + ODD) / (2 x I2SDIV + ODD). F_S maximum value is supported for each mode/condition.

Table 79. Synchronous multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2T_{HCLK}$	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	0	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x= 0…2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	2	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	2	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16…25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x=16…25)	0	-	ns
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low	-	0	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	2	-	ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	4.5	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	ns
$t_{su(ADV-CLKH)}$	FSMC_A/D[15:0] valid data before FSMC_CLK high	6	-	ns
$t_{h(CLKH-ADV)}$	FSMC_A/D[15:0] valid data after FSMC_CLK high	0	-	ns
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	4	-	ns
$t_{h(CLKH-NWAIT)}$	FSMC_NWAIT valid after FSMC_CLK high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization.

Figure 74. SD default mode

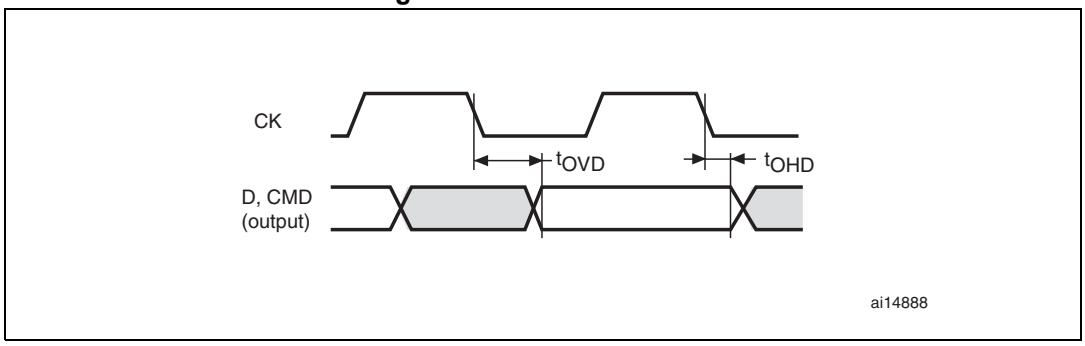

Table 88. Dynamic characteristics: SD / MMC characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode		0		48	MHz
	SDIO_CK/f_{PCLK2} frequency ratio		-	-	8/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 48 MHz	8.5	9	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 48 MHz	8.3	10	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	f_{PP} = 48 MHz	3	-	-	ns
t_{IH}	Input hold time HS	f_{PP} = 48 MHz	0	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	f_{PP} = 48 MHz	-	4.5	6	ns
t_{OH}	Output hold time HS	f_{PP} = 48 MHz	1	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	f_{PP} = 24 MHz	1.5	-	-	ns
t_{IHD}	Input hold time SD	f_{PP} = 24 MHz	0.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	f_{PP} = 24 MHz	-	4.5	7	ns
t_{OHD}	Output hold default time SD	f_{PP} = 24 MHz	0.5	-	-	

1. Guaranteed by characterization.

5.3.29 RTC characteristics

Table 89. RTC characteristics

Symbol	Parameter	Conditions	Min	Max
-	f_{PCLK1}/RTCCLK frequency ratio	Any read/write operation from/to an RTC register	4	-

Table 100. Document revision history (continued)

Date	Revision	Changes
04-Jun-2013	4 (continued)	Updated *Figure 6: Multi-AHB matrix*. Updated *Figure 7: Power supply supervisor interconnection with internal reset OFF* Changed 1.2 V to V_{12} in *Section : Regulator OFF* Updated LQFP176 pin 48. Updated *Section 1: Introduction*. Updated *Section 2: Description*. Updated operating voltage in *Table 2: STM32F415xx and STM32F417xx: features and peripheral counts*. Updated *Note 1*. Updated *Section 2.2.15: Power supply supervisor*. Updated *Section 2.2.16: Voltage regulator*. Updated *Figure 9: Regulator OFF*. Updated *Table 3: Regulator ON/OFF and internal reset ON/OFF availability*. Updated *Section 2.2.19: Low-power modes*. Updated *Section 2.2.20: VBAT operation*. Updated *Section 2.2.22: Inter-integrated circuit interface (I²C)* . Updated pin 48 in *Figure 15: STM32F41xxx LQFP176 pinout*. Updated *Table 6: Legend/abbreviations used in the pinout table*. Updated *Table 7: STM32F41xxx pin and ball definitions*. Updated *Table 14: General operating conditions*. Updated *Table 15: Limitations depending on the operating power supply range*. Updated *Section 5.3.7: Wakeup time from low-power mode*. Updated *Table 34: HSI oscillator characteristics*. Updated *Section 5.3.15: I/O current injection characteristics*. Updated *Table 48: I/O static characteristics*. Updated *Table 51: NRST pin characteristics*. Updated *Table 56: I^2C characteristics*. Updated *Figure 39: I^2C bus AC waveforms and measurement circuit*. Updated *Section 5.3.19: Communications interfaces*. Updated *Table 67: ADC characteristics*. Added *Table 70: Temperature sensor calibration values*. Added *Table 73: Internal reference voltage calibration values*. Updated *Section 5.3.26: FSMC characteristics*. Updated *Section 5.3.28: SD/SDIO MMC card host interface (SDIO) characteristics*. Updated *Table 23: Typical and maximum current consumptions in Stop mode*. Updated *Section : SPI interface characteristics* included *Table 55*. Updated *Section : I2S interface characteristics* included *Table 56*. Updated *Table 64: Dynamic characteristics: Eternity MAC signals for SMI*. Updated *Table 66: Dynamic characteristics: Ethernet MAC signals for MII*.

Table 100. Document revision history (continued)

Date	Revision	Changes
04-Jun-2013	4 (continued)	Updated *Table 64: Dynamic characteristics: Eternity MAC signals for SMI*. Updated *Table 66: Dynamic characteristics: Ethernet MAC signals for MII*. Updated *Table 79: Synchronous multiplexed NOR/PSRAM read timings*. Updated *Table 80: Synchronous multiplexed PSRAM write timings*. Updated *Table 81: Synchronous non-multiplexed NOR/PSRAM read timings*. Updated *Table 82: Synchronous non-multiplexed PSRAM write timings*. Updated *Section 5.3.27: Camera interface (DCMI) timing specifications* including *Table 87: DCMI characteristics* and addition of *Figure 72: DCMI timing diagram*. Updated *Section 5.3.28: SD/SDIO MMC card host interface (SDIO) characteristics* including *Table 88*. Updated *Chapter Figure 9.*