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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f415vgt6tr

- 8- to 14-bit parallel camera interface up to 54 Mbytes/s
- Cryptographic acceleration: hardware acceleration for AES 128, 192, 256, Triple DES, HASH (MD5, SHA-1), and HMAC
- True random number generator
- CRC calculation unit
- 96-bit unique ID
- RTC: subsecond accuracy, hardware calendar

Table 1. Device summary

Reference	Part number
STM32F415xx	STM32F415RG, STM32F415VG, STM32F415ZG, STM32F415OG
STM32F417xx	STM32F417VG, STM32F417IG, STM32F417ZG, STM32F417VE, STM32F417ZE, STM32F417IE

2.2.1 ARM® Cortex®-M4 core with FPU and embedded Flash and SRAM

The ARM Cortex-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M4 32-bit RISC processor with FPU features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F415xx and STM32F417xx family is compatible with all ARM tools and software.

Figure 5 shows the general block diagram of the STM32F41xxx family.

Note: Cortex-M4 with FPU is binary compatible with Cortex-M3.

2.2.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 with FPU processors. It balances the inherent performance advantage of the ARM Cortex-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 210 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 168 MHz.

2.2.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.2.4 Embedded Flash memory

The STM32F41xxx devices embed a Flash memory of 512 Kbytes or 1 Mbytes available for storing programs and data.

The DMA can be used with the main peripherals:

- SPI and I^2S
- I^2C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDIO
- Cryptographic acceleration
- Camera interface (DCMI)
- ADC.

2.2.9 Flexible static memory controller (FSMC)

The FSMC is embedded in the STM32F415xx and STM32F417xx family. It has four Chip Select outputs supporting the following modes: PCCard/Compact Flash, SRAM, PSRAM, NOR Flash and NAND Flash.

Functionality overview:

- Write FIFO
- Maximum FSMC_CLK frequency for synchronous accesses is 60 MHz.

LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

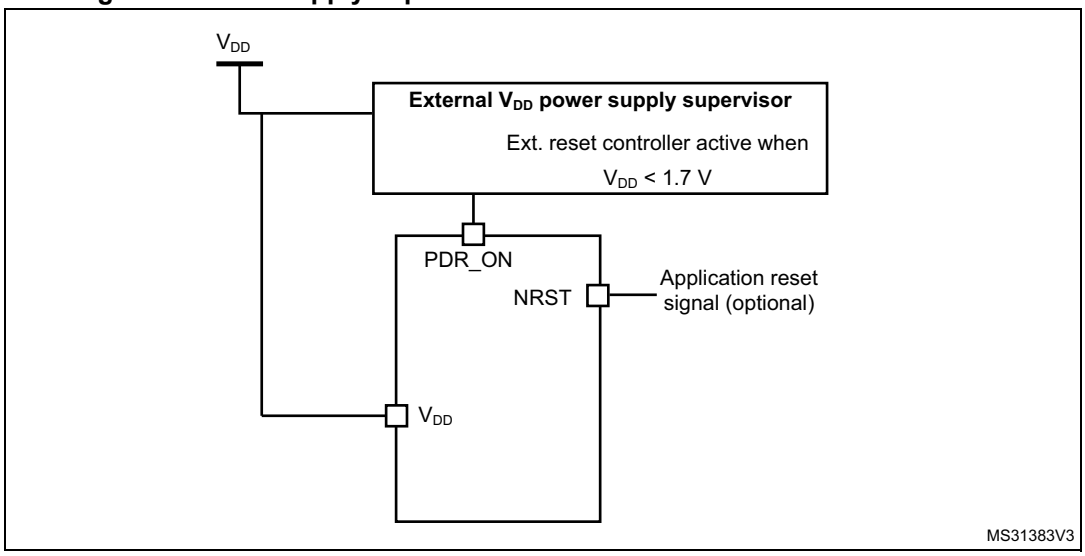
2.2.10 Nested vectored interrupt controller (NVIC)

The STM32F415xx and STM32F417xx embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 82 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

Figure 7. Power supply supervisor interconnection with internal reset OFF



1. PDR = 1.7 V for reduce temperature range; PDR = 1.8 V for all temperature range.

The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.8 V (see *Figure 7*). This supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range.

A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry is disabled
- The embedded programmable voltage detector (PVD) is disabled
- V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}

All packages, except for the LQFP64 and LQFP100, allow to disable the internal reset through the PDR_ON signal.

Table 10. STM32F41x register boundary addresses

Bus	Boundary address	Peripheral
	0xE00F FFFF - 0xFFFF FFFF	Reserved
Cortex-M4	0xE000 0000 - 0xE00F FFFF	Cortex-M4 internal peripherals
	0xA000 1000 - 0xDFFF FFFF	Reserved
AHB3	0xA000 0000 - 0xA000 0FFF	FSMC control register
	0x9000 0000 - 0x9FFF FFFF	FSMC bank 4
	0x8000 0000 - 0x8FFF FFFF	FSMC bank 3
	0x7000 0000 - 0x7FFF FFFF	FSMC bank 2
	0x6000 0000 - 0x6FFF FFFF	FSMC bank 1
	0x5006 0C00- 0x5FFF FFFF	Reserved
AHB2	0x5006 0800 - 0x5006 0BFF	RNG
	0x5006 0400 - 0x5006 07FF	HASH
	0x5006 0000 - 0x5006 03FF	CRYP
	0x5005 0400 - 0x5005 FFFF	Reserved
	0x5005 0000 - 0x5005 03FF	DCMI
	0x5004 0000- 0x5004 FFFF	Reserved
	0x5000 0000 - 0x5003 FFFF	USB OTG FS
	0x4008 0000- 0x4FFF FFFF	Reserved

floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 28: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

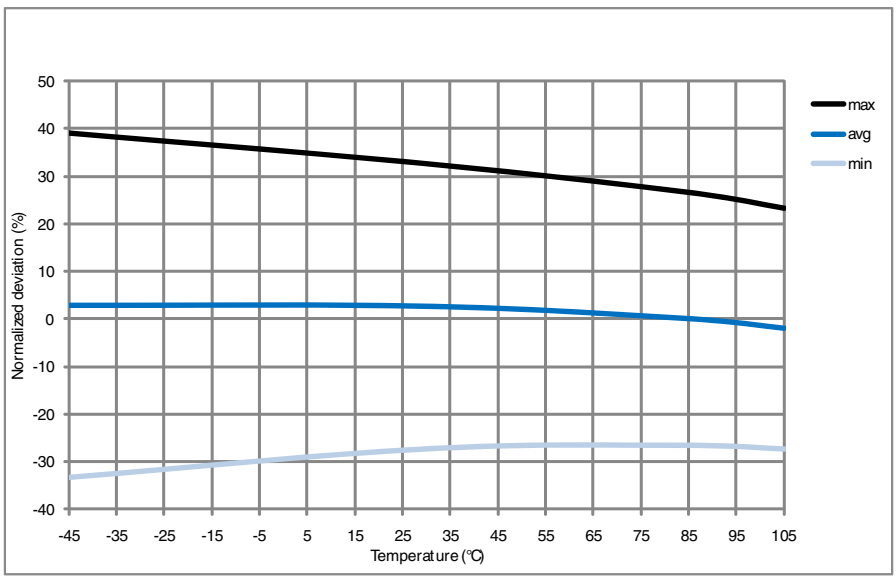
V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Figure 34. ACC_{LSI} versus temperature



5.3.10 PLL characteristics

The parameters given in *Table 36* and *Table 37* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 36. Main PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(1)	-	0.95(2)	1	2.10	MHz
f_{PLL_OUT}	PLL multiplier output clock	-	24	-	168	MHz
f_{PLL48_OUT}	48 MHz PLL multiplier output clock	-	-	48	75	MHz
f_{VCO_OUT}	PLL VCO output	-	100	-	432	MHz
t_{LOCK}	PLL lock time	VCO freq = 100 MHz	75	-	200	µs
		VCO freq = 432 MHz	100	-	300	

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC? code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 44. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				25/168 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP176 package, conforming to SAE J1752/3 EEMBC, code running from Flash with ART accelerator enabled	0.1 to 30 MHz	32	dBµV
			30 to 130 MHz	25	
			130 MHz to 1GHz	29	
			SAE EMI Level	4	-
		V_{DD} = 3.3 V, T_A = 25 °C, LQFP176 package, conforming to SAE J1752/3 EEMBC, code running from Flash with ART accelerator and PLL spread spectrum enabled	0.1 to 30 MHz	19	dBµV
			30 to 130 MHz	16	
			130 MHz to 1GHz	18	
			SAE EMI level	3.5	-

5.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 45. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000(2)	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD STM5.3.1	II	500	

1. Guaranteed by characterization.
2. On V_{BAT} pin, $V_{ESD(HBM)}$ is limited to 1000 V.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ±3mA. When using the PC13 to PC15 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 12*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 12*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 49* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*. All I/Os are CMOS and TTL compliant.

Table 49. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(2)	Output low level voltage	CMOS port I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage		V_{DD}–0.4	-	
V_{OL} (2)	Output low level voltage	TTL port I_{IO} =+ 8mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage		2.4	-	
V_{OL}(2)(4)	Output low level voltage	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH}(3)(4)	Output high level voltage		V_{DD}–1.3	-	
V_{OL}(2)(4)	Output low level voltage	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(3)(4)	Output high level voltage		V_{DD}–0.4	-	

1. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (e.g. to drive an LED).
2. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 12* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 12* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Guaranteed by characterization.

Table 55. SPI dynamic characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(SCKH)}$	SCK high and low time	Master mode, SPI presc = 2, 2.7V < V_{DD} < 3.6V	T_{PCLK}-0.5	T_{PCLK}	T_{PCLK}+0.5	ns
$t_{w(SCKL)}$		Master mode, SPI presc = 2, 1.7V < V_{DD} < 3.6V	T_{PCLK}-2	T_{PCLK}	T_{PCLK}+2	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4 x T_{PCLK}	-	-	
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2 x T_{PCLK}			
$t_{su(MI)}$	Data input setup time	Master mode	6.5	-	-	
$t_{su(SI)}$		Slave mode	2.5	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	2.5	-	-	
$t_{h(SI)}$		Slave mode	4	-	-	
$t_{a(SO)}$(2)	Data output access time	Slave mode, SPI presc = 2	0	-	4 x T_{PCLK}	
$t_{dis(SO)}$(3)	Data output disable time	Slave mode, SPI1, 2.7V < V_{DD} < 3.6V	0	-	7.5	
		Slave mode, SPI1/2/3 1.7V < V_{DD} < 3.6V	0	-	16.5	
$t_{v(SO)}$ $t_{h(SO)}$	Data output valid/hold time	Slave mode (after enable edge), SPI1, 2.7V < V_{DD} < 3.6V	-	11	13	
		Slave mode (after enable edge), SPI2/3, 2.7V < V_{DD} < 3.6V	-	12	16.5	
		Slave mode (after enable edge), SPI1, 1.7V < V_{DD} < 3.6V	-	15.5	19	
		Slave mode (after enable edge), SPI2/3, 1.7V < V_{DD} < 3.6V	-	18	20.5	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge), SPI1, 2.7V < V_{DD} < 3.6V	-	-	2.5	
		Master mode (after enable edge), SPI1/2/3, 1.7V < V_{DD} < 3.6V	-	-	4.5	
$t_{h(MO)}$	Data output hold time	Master mode (after enable edge)	0	-	-	

1. Guaranteed by characterization.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 57. Asynchronous multiplexed PSRAM/NOR write waveforms

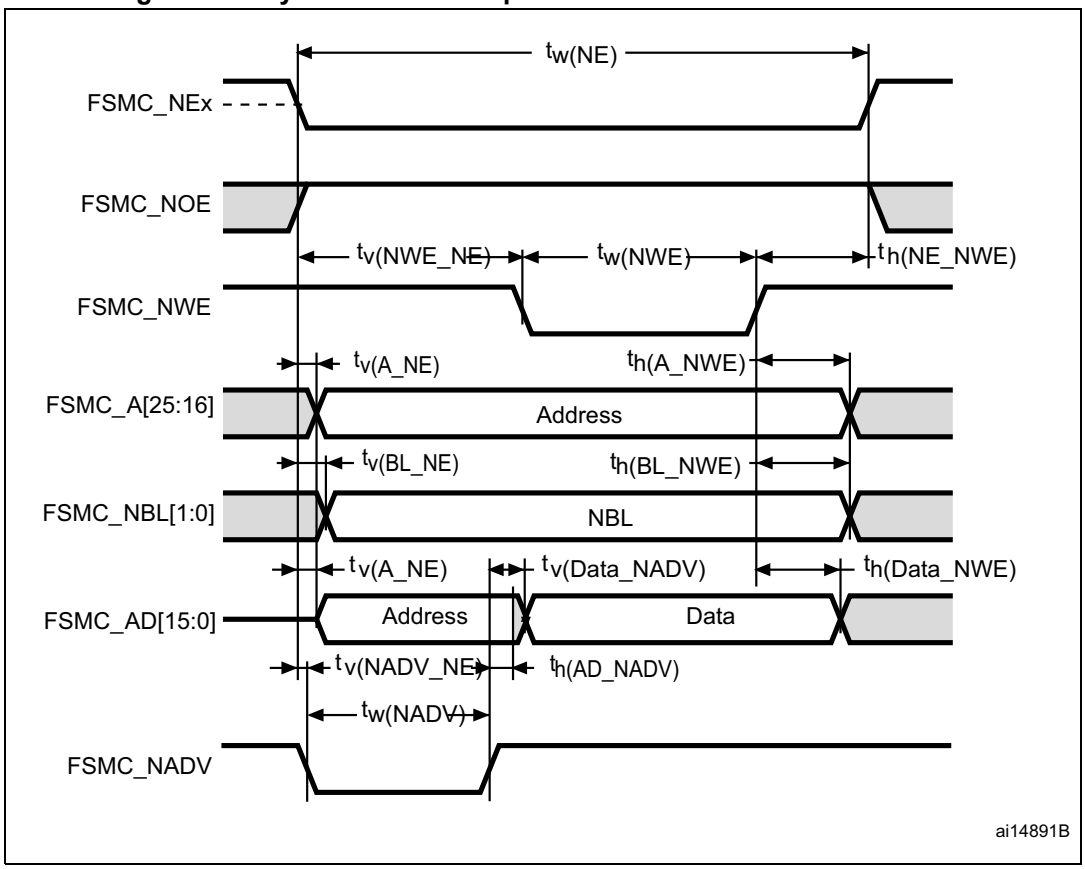


Table 78. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$4T_{HCLK}$–0.5	$4T_{HCLK}$+3	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	T_{HCLK}–0.5	T_{HCLK} -0.5	ns
$t_{w(NWE)}$	FSMC_NWE low tim e	$2T_{HCLK}$–0.5	$2T_{HCLK}$+3	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	T_{HCLK}	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	1	2	ns
$t_{w(NADV)}$	FSMC_NADV low time	T_{HCLK}– 2	T_{HCLK}+ 1	ns
$t_{h(AD\_NADV)}$	FSMC_AD(address) valid hold time after FSMC_NADV high)	T_{HCLK}–2	-	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	T_{HCLK}	-	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	T_{HCLK}–2	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	1.5	ns
$t_{v(Data\_NADV)}$	FSMC_NADV high to Data valid	-	T_{HCLK}–0.5	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	T_{HCLK}	-	ns

1. C_L = 30 pF.

Table 84. Switching characteristics for PC Card/CF read and write cycles in I/O space(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NIOWR)}$	FSMC_NIOWR low width	$8T_{HCLK}$ –1	-	ns
$t_{v(NIOWR-D)}$	FSMC_NIOWR low to FSMC_D[15:0] valid	-	$5T_{HCLK}$– 1	ns
$t_{h(NIOWR-D)}$	FSMC_NIOWR high to FSMC_D[15:0] invalid	$8T_{HCLK}$– 2	-	ns
$t_{d(NCE4\_1-NIOWR)}$	FSMC_NCE4_1 low to FSMC_NIOWR valid	-	$5T_{HCLK}$+ 2.5	ns
$t_{h(NCEx-NIOWR)}$	FSMC_NCEx high to FSMC_NIOWR invalid	$5T_{HCLK}$–1.5	-	ns
$t_{d(NIORD-NCEx)}$	FSMC_NCEx low to FSMC_NIORD valid	-	$5T_{HCLK}$+ 2	ns
$t_{h(NCEx-NIORD)}$	FSMC_NCEx high to FSMC_NIORD) valid	$5T_{HCLK}$– 1.5	-	ns
$t_{w(NIORD)}$	FSMC_NIORD low width	$8T_{HCLK}$–0.5	-	ns
$t_{su(D-NIORD)}$	FSMC_D[15:0] valid before FSMC_NIORD high	9	-	ns
$t_{d(NIORD-D)}$	FSMC_D[15:0] valid after FSMC_NIORD high	0	-	ns

1. C_L = 30 pF.
2. Guaranteed by characterization.

NAND controller waveforms and timings

Figure 68 through *Figure 71* represent synchronous waveforms, and *Table 85* and *Table 86* provide the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x01;
- COM.FSMC_WaitSetupTime = 0x03;
- COM.FSMC_HoldSetupTime = 0x02;
- COM.FSMC_HiZSetupTime = 0x01;
- ATT.FSMC_SetupTime = 0x01;
- ATT.FSMC_WaitSetupTime = 0x03;
- ATT.FSMC_HoldSetupTime = 0x02;
- ATT.FSMC_HiZSetupTime = 0x01;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 68. NAND controller waveforms for read access

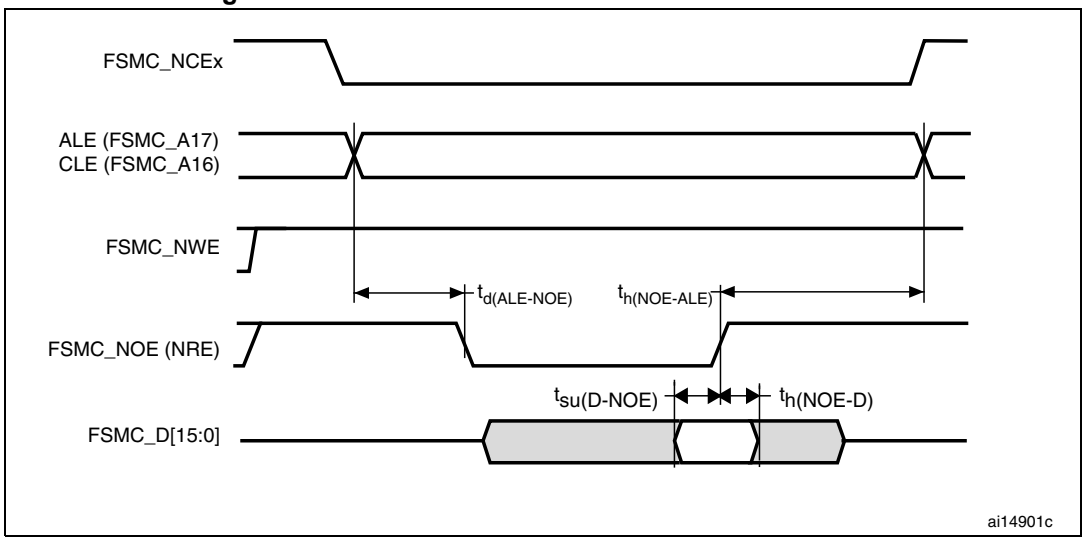
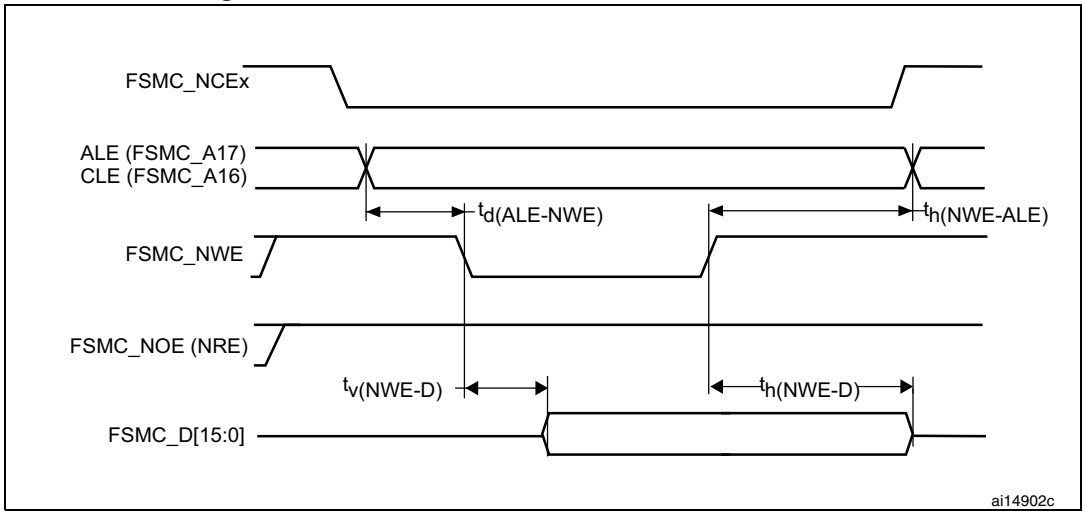


Figure 69. NAND controller waveforms for write access

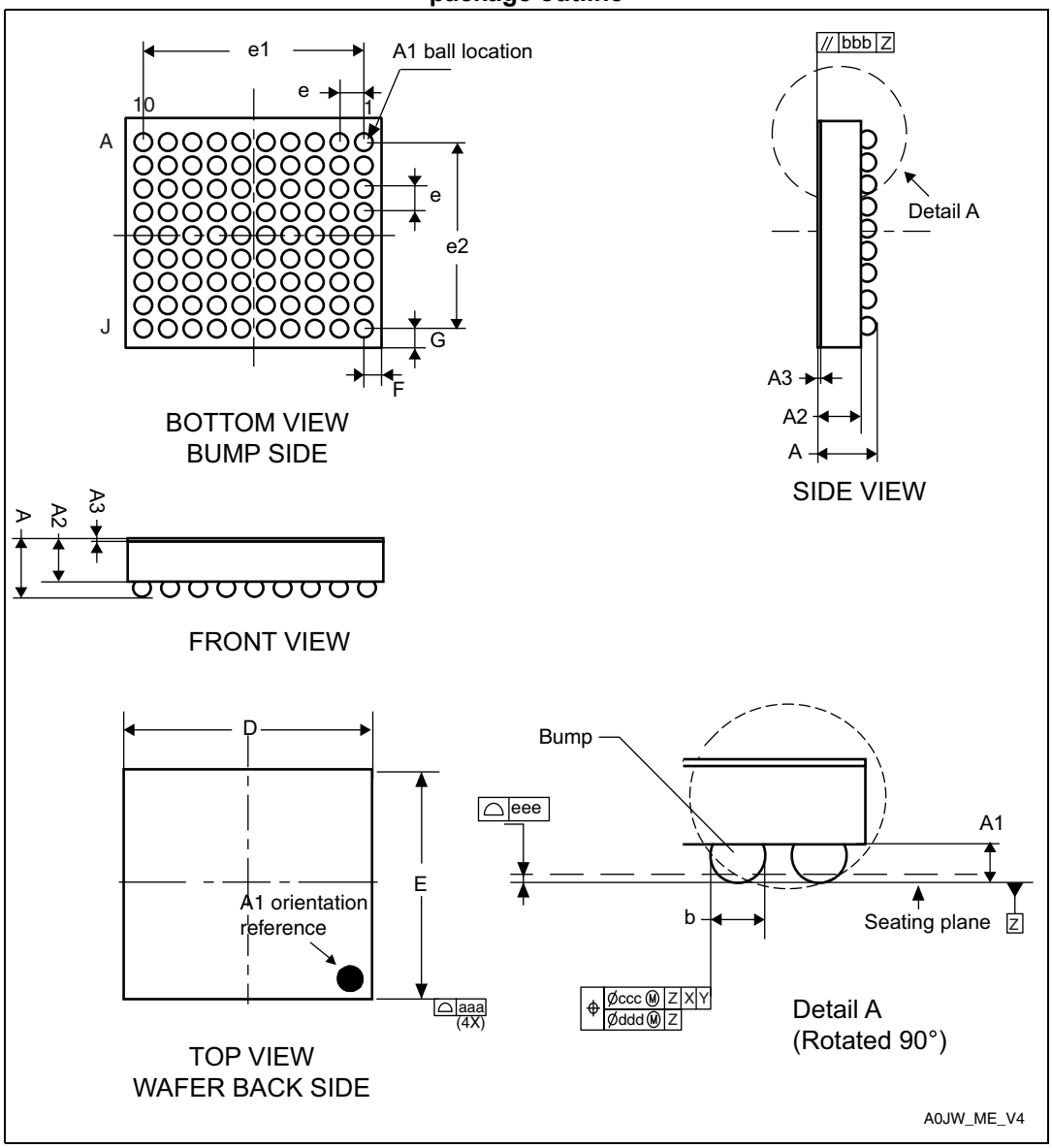


6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

6.1 WLCSP90 package information

Figure 75. WLCSP90 - 4.223 x 3.969 mm, 0.400 mm pitch wafer level chip scale package outline



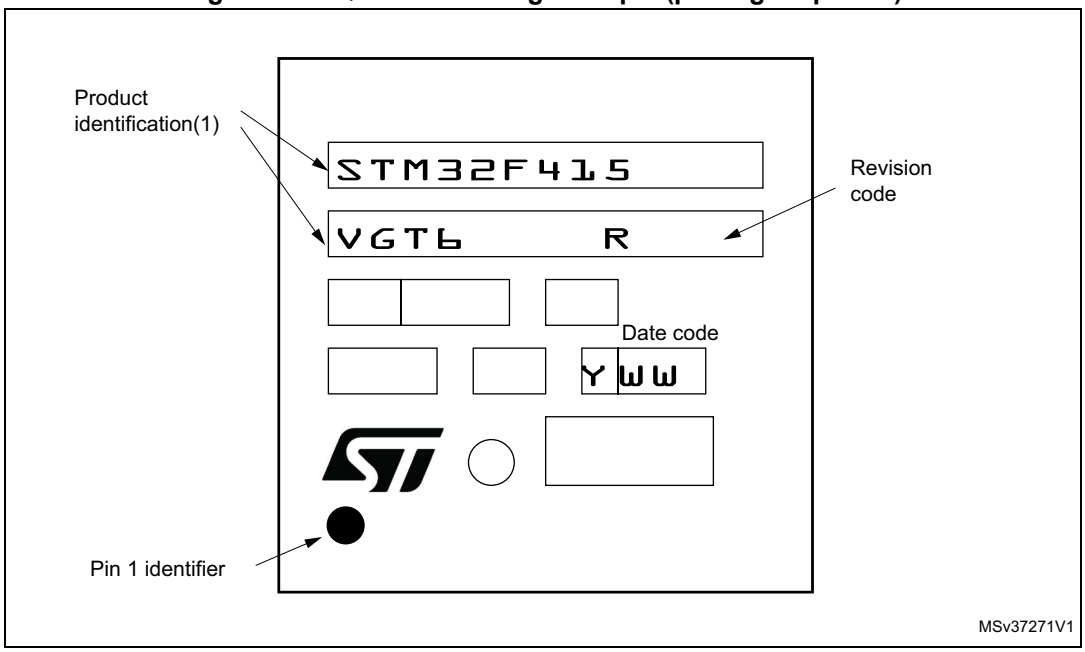
1. Drawing is not to scale.

Device marking for LFP100

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

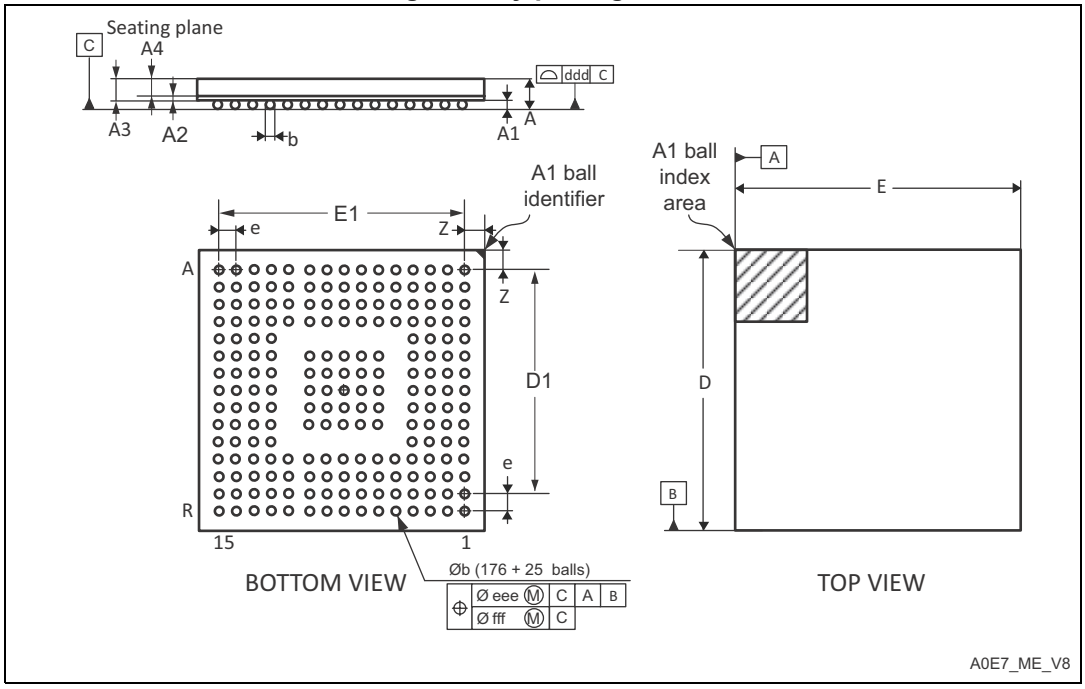
Figure 83. LQFP100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

6.5 UFBGA176+25 package information

Figure 87. UFBGA176+25 ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 95. UFBGA176+25 ball, 10 × 10 × 0.65 mm pitch, ultra thin fine pitch ball grid array mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.130	-	-	0.0051	-
A3	-	0.450	-	-	0.0177	-
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
Z	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

8 Revision history

Table 100. Document revision history

Date	Revision	Changes
15-Sep-2011	1	Initial release.
24-Jan-2012	2	Added WLCSP90 package on cover page. Renamed USART4 and USART5 into UART4 and UART5, respectively. Updated number of USB OTG HS and FS in *Table 2: STM32F415xx and STM32F417xx: features and peripheral counts*. Updated *Figure 3: Compatible board design between STM32F10xx/STM32F2/STM32F41xxx for LQFP144 package* and *Figure 4: Compatible board design between STM32F2 and STM32F41xxx for LQFP176 and BGA176 packages*, and removed note 1 and 2. Updated *Section 2.2.9: Flexible static memory controller (FSMC)*. Modified I/Os used to reprogram the Flash memory for CAN2 and USB OTG FS in *Section 2.2.13: Boot modes*. Updated note in *Section 2.2.14: Power supply schemes*. PDR_ON no more available on LQFP100 package. Updated *Section 2.2.16: Voltage regulator*. Updated condition to obtain a minimum supply voltage of 1.7 V in the whole document. Renamed USART4/5 to UART4/5 and added LIN and IrDA feature for UART4 and UART5 in *Table 5: USART feature comparison*. Removed support of I2C for OTG PHY in *Section 2.2.30: Universal serial bus on-the-go full-speed (OTG_FS)*. Added *Table 6: Legend/abbreviations used in the pinout table*. *Table 7: STM32F41xxx pin and ball definitions*: replaced V_{SS}_3, V_{SS}_4, and V_{SS}_8 by V_{SS}; reformatted *Table 7: STM32F41xxx pin and ball definitions* to better highlight I/O structure, and alternate functions versus additional functions; signal corresponding to LQFP100 pin 99 changed from PDR_ON to V_{SS}; EVENTOUT added in the list of alternate functions for all I/Os; ADC3_IN8 added as alternate function for PF10; FSMC_CLE and FSMC_ALE added as alternate functions for PD11 and PD12, respectively; PH10 alternate function TIM15_CH1_ETR renamed TIM5_CH1; updated PA4 and PA5 I/O structure to TTa. Removed OTG_HS_SCL, OTG_HS_SDA, OTG_FS_INTN in *Table 7: STM32F41xxx pin and ball definitions* and *Table 9: Alternate function mapping*. Changed TCM data RAM to CCM data RAM in *Figure 18: STM32F41xxx memory map*. Added I_{VDD} and I_{VSS} maximum values in *Table 12: Current characteristics*. Added *Note 1* related to f_{HCLK}, updated *Note 2* in *Table 14: General operating conditions*, and added maximum power dissipation values. Updated *Table 15: Limitations depending on the operating power supply range*.

Table 100. Document revision history (continued)

Date	Revision	Changes
04-Jun-2013	4 (continued)	Updated *Table 64: Dynamic characteristics: Eternity MAC signals for SMI*. Updated *Table 66: Dynamic characteristics: Ethernet MAC signals for MII*. Updated *Table 79: Synchronous multiplexed NOR/PSRAM read timings*. Updated *Table 80: Synchronous multiplexed PSRAM write timings*. Updated *Table 81: Synchronous non-multiplexed NOR/PSRAM read timings*. Updated *Table 82: Synchronous non-multiplexed PSRAM write timings*. Updated *Section 5.3.27: Camera interface (DCMI) timing specifications* including *Table 87: DCMI characteristics* and addition of *Figure 72: DCMI timing diagram*. Updated *Section 5.3.28: SD/SDIO MMC card host interface (SDIO) characteristics* including *Table 88*. Updated *Chapter Figure 9.*